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VPR-80
Service Manual

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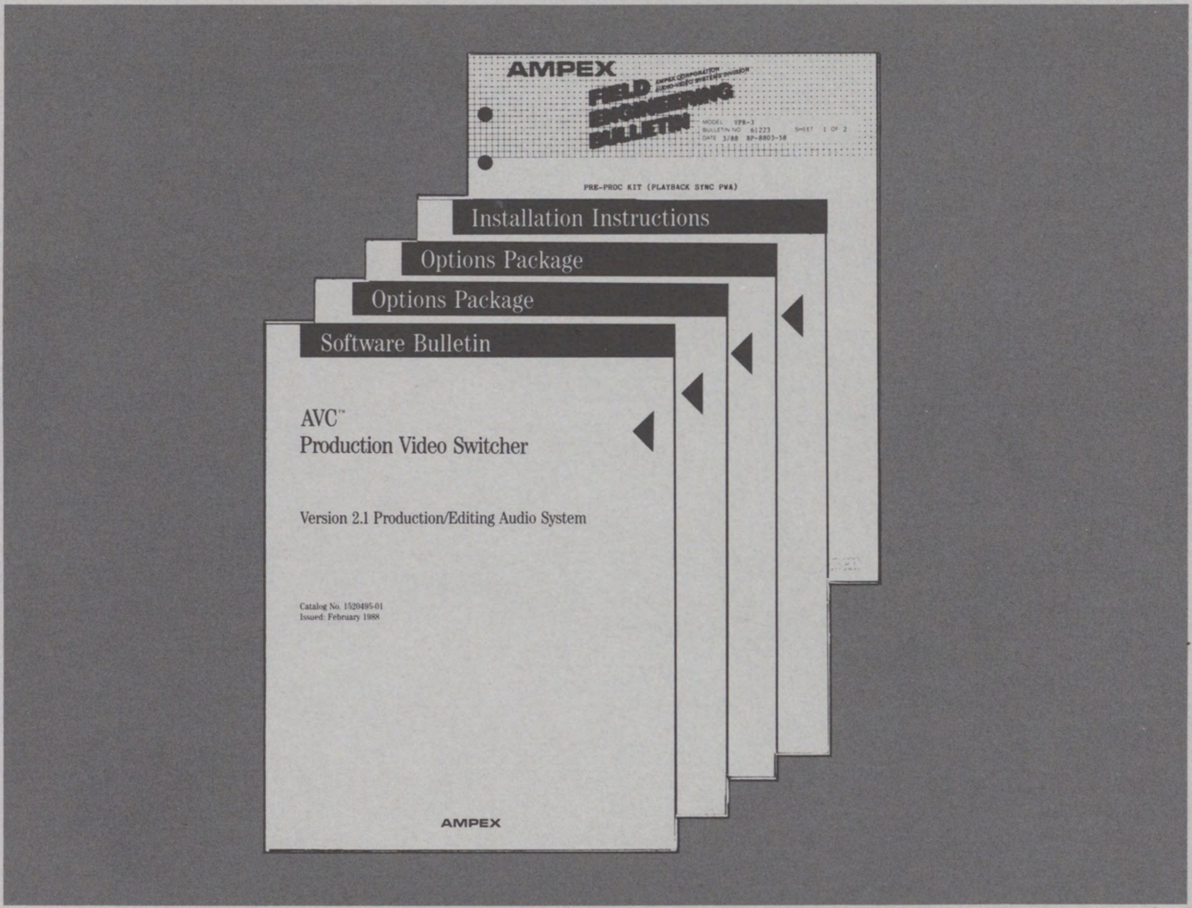
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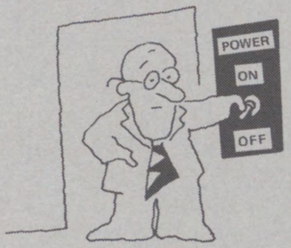
Safety and First Aid Suggestions

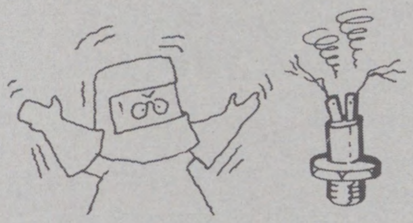
Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of the first aid related to electrical hazards.

In addition, the following safety practices must be followed:

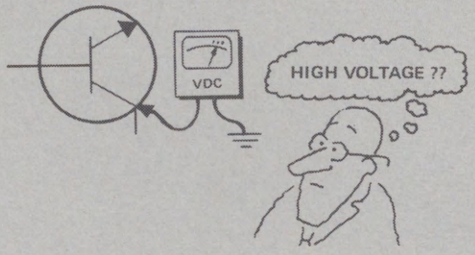


Do not attempt to adjust unprotected circuit controls or to dress leads with power **on.**

Always avoid placing parts of the body in series between ground and circuit points



To avoid burns, do not touch heavily loaded or overheated components without precaution.



Remember that some semiconductor cases and solid-state circuits carry high voltages.

Do not asssume that all danger of electrical shock is removed when power is **off.** Charged capacitors can retain dangerous voltages for a long time after power is turned off. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

Don't take chances. Be fully trained. Ampex equipment should be operated and maintained by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before rendering aid. Muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT TOUCH VICTIM OR HIS CLOTHING BEFORE POWER IS DISCONNECTED OR YOU CAN ALSO BECOME A SHOCK VICTIM.

If power cannot be turned off immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

Good Practices

In maintaining the equipment covered in this manual, please keep in mind the following, standard good practices:

When connecting any instrument (oscilloscope, waveform, monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminally internally.

When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.

When troubleshooting, remember that FETs and other metal-oxide semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.

When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.

When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

Warning

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case, the user, at his own expense, will be required to take whatever measures may be necessary to correct the interference.

Note

This system was tested using the shielded interconnect cables provided with the unit. Failure to use the cables provided may result in radio interference outside acceptable limits.

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VPR-80 Video Production Recorder

PART I
SECTION 1
GENERAL INFORMATION

1-1 PURPOSE AND SCOPE OF MANUAL

This manual provides maintenance information and instructions for the VPR-80 Video Production Recorder. It is part of the accessory VPR-80 Service Kit, and information and instructions herein are intended for use by trained service personnel only. Information covers all color video system configurations of the VPR-80: NTSC, PAL-M, and PAL/SECAM.

This manual is divided into two parts. Part I covers VPR-80 maintenance on a system basis, and also provides both physical and functional descriptions of VPR-80 subsystems. Modes of operation are explained, and functions of each switch and the significance of each indicator are tabulated. Detailed test and adjustment procedures are given which ensure interchangeability of Type C format video tapes. This is followed by information and instructions on the use of self-test features which verify VPR-80 performance and isolate faults to individual subsystems or PWAs.

Part II covers maintenance of individual subassemblies and printed wiring assemblies (PWAs). It also contains theory of operation discussions and illustrated test and adjustment procedures for each subsystem in the VPR-80, as well as instructions for the removal of major subassemblies so that they can be repaired and bench tested. Schematics, wiring diagrams, and parts lists which supplement this information are contained in the *VPR-80 Parts Lists and Schematics* manual.

Organization of this manual is diagrammed in Figure 1-1.

1-2 RELATED PUBLICATIONS

1-3 Installation and Operation Manual

Part of the miscellaneous parts kit furnished with every VPR-80, this manual provides information and instructions for the guidance of the VTR operator only insofar as that person is involved in the installation and operation of the VPR-80. Remote control and time-base corrector interfaces are documented in detail. Complete instructions for both manual and automated insert and assemble editing procedures are included. The *VPR-80 Service Manual* assumes the technician's familiarity with the contents of the *VPR-80 Installation and Operation* manual.

1-4 Parts Lists and Schematics Manual

This manual is part of the accessory VPR-80 General Service Kit. It contains complete parts lists, schematics, and parts location drawings for each of the

VPR-80 subsystems and PWAs. Drawing information enables the technician to physically and schematically locate components referenced in the *Service Manual*, while parts lists enable positive component identification for part replacement purposes. Contents of the *Parts Lists and Schematics* manual are periodically updated under an ongoing manual revision program which keeps the manual current with product enhancements.

1-5 Diagnostic Procedures

Section 9, Part II of this manual instructs the technician in the use of the diagnostic probe accessory to isolate a detected fault to an individual component (or group of components) within a subassembly or PWA. Section 9 assumes the technician's familiarity with the contents of the *Installation and Operation* manual and this *Service Manual*.

1-6 INTENDED USE OF EQUIPMENT

The VPR-80 is a one-inch, one-field-per-scan, helical video tape recorder with a 124-minute record/play time. The VPR-80 is compatible with all standard features specified in the SMPTE Type C and EBU Format C specification for 1-inch, helical scan video tape recordings. The VPR-80 can be used with 525-line/60-Hz or 625-line/50-Hz monochrome or NTSC/PAL/SECAM color systems.

1-7 CAPABILITIES

Major features and capabilities of the basic VPR-80 are as follows:

- Three audio channels, all capable of full bandwidth record and playback operations.
- Variable speed shuttle, providing up to 300 in/sec (762 cm/sec) speed in forward and reverse (30X normal).
- Variable speed play, from still to one and one-half play speed forward.
- Color framer, for minimizing horizontal picture shift during editing or switching.
- Autochroma, for automatically adjusting playback equalization control on a field-by-field basis.
- Tape timer, providing digital display with one-frame accuracy.
- Auto edit control with tape timer, providing complete automatic editing capability, including programmable entrance and exit edit points, as well as multi-VTR control and rehearsal features.
- Video meter, providing monitoring of off-tape rf level or incoming video level.
- Automatic scan tracking (AST*), enabling the video record/play head to be mechanically deflected. This ensures accurate tracking of recorded video

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* TM Ampex Corporation

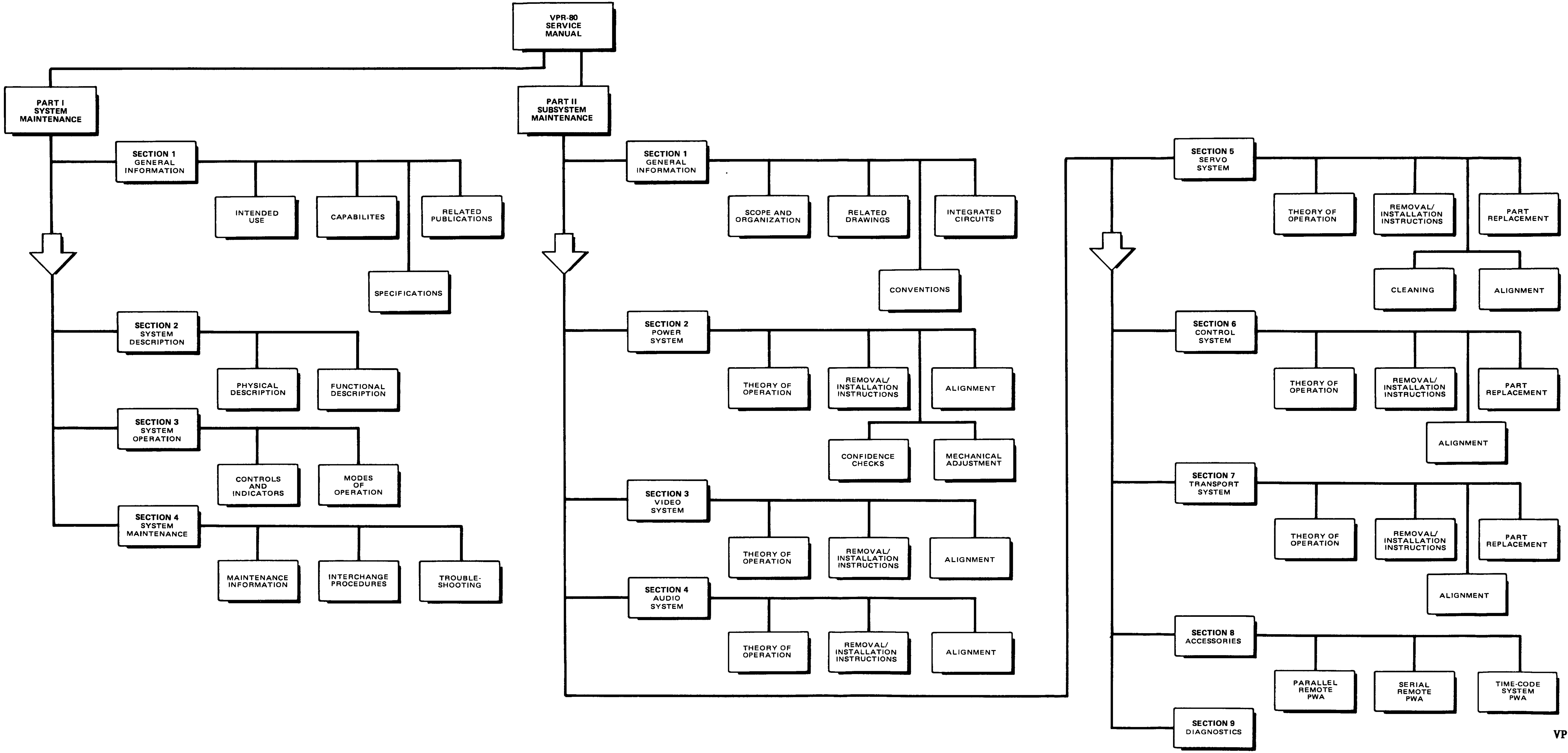

Figure 1-1.
VPR-80 Service Manual Organization

material, and, when used in conjunction with the Ampex TBC-6 Time-Base Corrector, provides still-mode and forward slow-motion playback without picture disturbances.

- Automatic fault detection with an interactive fault isolation program.
- Keypad for entering setup condition identifiers (i.e., video head optimization), edit entrance and exit points, and edit point trim values.

1-8 Additional Capabilities with Accessory Equipment

The VPR-80 is designed for compatibility with standard Ampex audio/video system options and accessories. When equipped with the parallel remote accessory, the VPR-80 can be controlled by external accessory items 1 through 3 listed below.

1. The RCO-2 Remote Changeover Unit allows the VPR-80 to be switched to any one of three remote control devices. The RCO-2 can be located up to 150 feet from the VTR and can also be remote controlled.

2. The SMC-100 Slow Motion Controller provides remote and expanded control of VTR transport functions. It also includes two manually controllable cue points used in conjunction with the SMC-100 front panel 60-second clock display.

3. The STC-100 Search to Cue accessory device can recall up to 99 auto cue points or 99 still recordings for quick access. The STC-100 also has the ability to store its entire memory on tape for recall by another STC-100 at another location.

4. The TBC-6 Digital Time-Base Corrector provides a broadcast quality video signal from the VPR-80 during normal, slow-motion, and still-frame playback and provides a viewable picture in shuttle modes. The TBC-6 includes features such as a one-line dropout compensator to replace missing video information with video from a previous correctly phased line, and a velocity compensator to reduce time-base errors on a line-by-line basis.

In addition to having compatibility with devices listed above, the VPR-80 can be equipped with an accessory serial control interface. The VPR-80 can, therefore, be integrated into an asynchronous data communication network such as the Ampex Computerized Editing System (ACE). The ACE edit controller communicates with on-line system components via SMPTE-proposed RS422-compatible lines. A typical editing system configuration is shown in Figure 1-2.

1-9 SPECIFICATIONS

Specifications for the VPR-80 are given in Table 1-1. Ampex reserves the right to make product and specification changes at any time without notice.

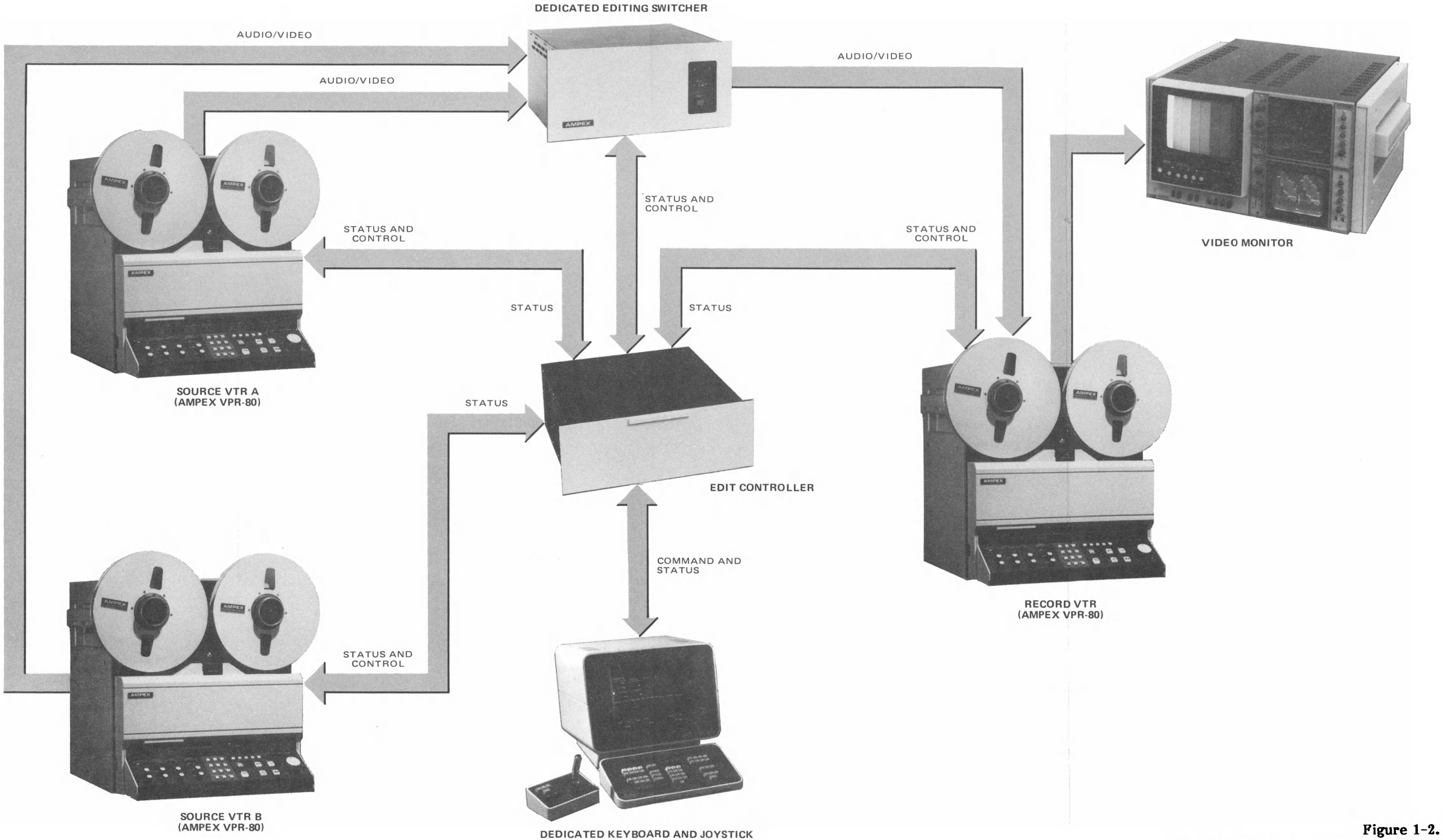

Figure 1-2.
Typical Editing System Configuration

Table 1-1. VPR-80 Specifications

Characteristics	Specifications	
	PAL/SECAM 625/50	NTSC/PAL-M 525/60
General		
Record Time	124 minutes nominal; 6000 ft of tape	124 minutes nominal, 6000 ft of tape
Shuttle Speed	300 in/s maximum	300 in/s maximum
Shuttle Time	less than 2-1/2 minutes for 60-minute tape	less than 2-1/2 minutes for 60-minute tape
Tape Timer Accuracy (control track updated)	±1 frame over full length of tape, with continuous control track	±1 frame over full length of tape, with continuous control track
Tape Speed	239.8 ±0.5 mm/s; 9.44 ±0.02 in/s	244 ±0.5 mm/s; 9.606 ±0.02 in/s
Video Writing Speed	842 in/s nominal 21.36 m/s nominal	1008 in/s nominal 25.60 m/s nominal
FM Carrier Frequencies	7.68 MHz blanking, 8.9 MHz peak white	7.9 MHz blanking, 10.0 MHz peak white
Audio Equalization (time constants)	15 µs	15 µs, 3180 µs
Lock-Up Time from Ready Mode	4 seconds	3 seconds
Signal Inputs		
Video Input (75Ω BNC)	0.5 to 2 Vp-p adjustable to unity	0.5 to 2 Vp-p adjustable to unity
Ref Video (75Ω BNC)		
Comp Video	0.5 to 2V	0.5 to 2V
Audio Line Inputs	−24 to +8 dBm nominal; +24 dBm	−24 to +8 dBm nominal; +24 dBm
Impedance	balanced; 50 KΩ (50 Hz to 15 kHz)	balanced; 50 KΩ (50 Hz to 15 kHz)
Microphone Input (channel internally selectable)	−60 dBm at 200 Ω −20 dBm maximum	−60 dBm at 200 Ω −20 dBm maximum
Signal Outputs		
Video Output (3) (75Ω BNC)	1.0 Vp-p	1.0 Vp-p
Audio Line Outputs	+8 dBm nominal; balanced	+8 dBm nominal; balanced
(Channels 1, 2, 3)	+24 dBm maximum	+24 dBm maximum
Impedance	less than 50Ω	less than 50Ω
Speaker and Head Phone Audio Monitor	0 dBm to drive 600Ω	0 dBm to drive 600Ω

(Continued next page)

Table 1-1. VPR-80 Specifications (Continued)

Characteristics	Specifications	
	PAL/SECAM 625/50	NTSC/PAL-M 525/60
Video and Sync		
Bandwidth	flat to 5.0 MHz ±1.0 dB −3 dB at 6.0 MHz	flat to 4.2 MHz ±1.0 dB −3 dB at 5.0 MHz
Signal-to-Noise (Rhode and Schwarz unweighted with bandpass filter, 50% APL) output through TBC	−43 dB p-p video to RMS noise on interchange basis	−46 dB p-p video to RMS noise on interchange basis
LF linearity	2% blanking to peak white (maximum)	2% blanking to peak white (maximum)
Differential Gain	4% blanking to peak white (maximum)	4% blanking to peak white (maximum)
Differential Phase (40 IEEE units of subcarrier through TBC)	4° at 4.43 MHz off-tape (maximum)	4° at 3.58 MHz off-tape (maximum)
Chrominance/ Luminance Delay	25 ns (maximum)	25 ns (maximum)
2T sin ^{2} Pulse and Bar	1% K-factor maximum	1% K-factor maximum
Moiré	−36 dB (4.43 MHz subcarrier)	−40 dB (3.58 MHz subcarrier)
Audio (Channels 1, 2, and 3)		
Frequency Response (100 nWb/m at 1 kHz reference level)	±1 dB 500 Hz to 12 kHz, ±2 dB 50 Hz to 15 kHz	±1 dB 500 Hz to 12 kHz, ±2 dB 50 Hz to 15 kHz
Signal-to-Noise (with respect to +8 dB above reference level)	−56 dB Audio 1 and 2, −54 dB for Audio 3	−56 dB Audio 1 and 2, −54 dB for Audio 3
Audio 3 wideband	−30 dB	-30 dB
Distortion (no predistortion)		
@100 nWb/m reference level (+8 dBm)	1% maximum	1% maximum
@ 251 nWb/m peak level (+16 dBm)	3% maximum	3% maximum
Depth of erasure (reference recording at 200 nWb/m at 1kHz)	-70 dB	-70 dB
Wow and Flutter	0.15% DIN weighted on own recording	0.12% RMS NAB unweighted on own recording

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Table 1-1. VPR-80 Specifications (Continued)

Characteristics	Specifications	
	PAL/SECAM 625/50	NTSC/PAL-M 525/60
Audio (Channels 1, 2, and 3) (Continued)		
Playback Crosstalk (Audio channel 1 and 2), 1 kHz referenced to +8 dBm or 100 nWb/m	-50 dB maximum	-50 dB maximum
Temperature and Humidity		
Temperature	0°C to 45°C	
Humidity	10% to 90% RH (noncondensing)	10% to 90% RH (noncondensing)
Power Input		
Power Line Frequency	50 to 60 Hz, single phase	50 to 60 Hz, single phase
Input Voltages	100/110/120/130 Vac, ±10% 200/220/240/260 Vac, ±10%	100/110/120/130 Vac, ±10% 200/220/240/260 Vac, ±10%
Input Current:	115 Vac, nominal 5.5A 230 Vac, nominal 2.5A	115 Vac, nominal 5.5A 230 Vac, nominal 2.5A
Physical Dimensions (Excluding Reels)		
Height:		
Tabletop (standard)	21.5 in. (546.1 mm)	21.5 in. (546.1 mm)
Rack Mount	21.0 in. (533.4 mm)	21.0 in. (533.4 mm)
Consolette	60.00 in. (1524 mm)	60.00 in. (1524 mm)
Pedestal	48.75 in. (1238 mm)	48.75 in. (1238 mm)
Width		
Tabletop (standard)	20.0 in. (508.2 mm)	20.0 in. (508.2 mm)
Rack Mount	19.0 in. (482.6 mm)	19.0 in. (482.6 mm)
Consolette	24.0 in. (610 mm)	24.0 in. (610 mm)
Pedestal	23.75 in. (603.3 mm)	23.75 in. (603.3 mm)
Depth:		
Tabletop (standard)	21.0 in. (533.4 mm)	21.0 in. (533.4 mm)
Rack Mount	21.0 in. (533.4 mm)	21.0 in. (533.4 mm)
Consolette	26.5 in. (673 mm)	26.5 in. (673 mm)
Pedestal	26.0 in. (660.4 mm)	26.0 in. (660.4 mm)
Weight:		
Tabletop (standard)	168 lb (73.6 kg)	168 lb (73.6 kg)
Rack Mount	159 lb (72.2 kg)	159 lb (72.2 kg)
Consolette	258 lb* (117.1 kg)	258 lb* (117.1 kg)
Pedestal	258 lb* (117.1 kg)	258 lb* (117.1 kg)

*Includes weight of time-base corrector, if installed.

PART I

SECTION 2

SYSTEM DESCRIPTION

2-1 GENERAL

This section provides detailed physical descriptions of each subassembly in the VPR-80, as well as functional descriptions of each of the major subsystems. Detailed descriptions and theory of operation discussions for each subassembly and PWA appear in Part II of this manual.

2-2 PHYSICAL DESCRIPTION

2-3 Configurations

The basic VPR-80 configuration is the tabletop model shown in the frontispiece. The VPR-80 can be rack-mounted, mounted on the consolette or pedestal accessories, or mounted in one of three console accessories.

2-4 Tabletop

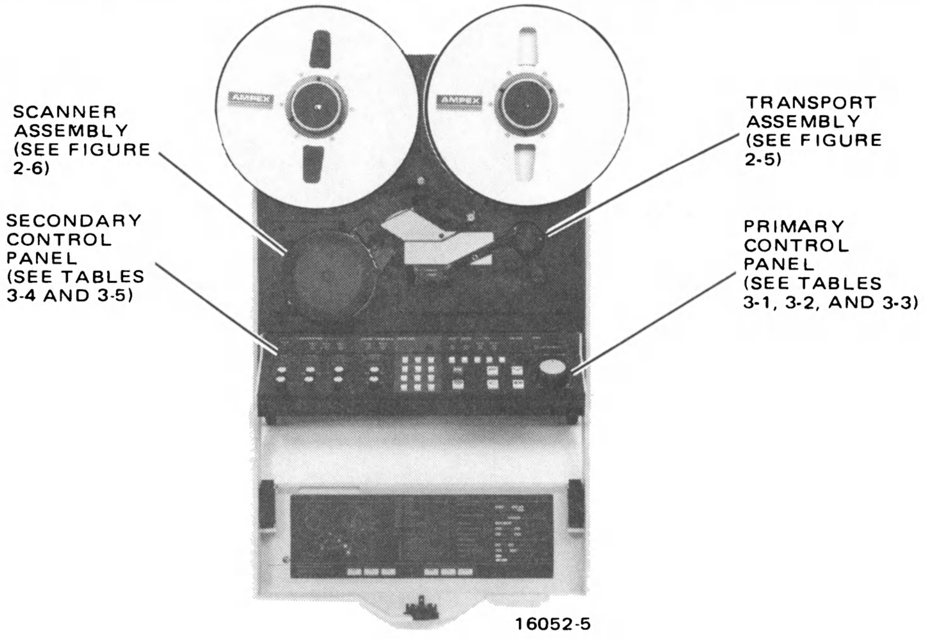
Front and rear views of the standard tabletop VPR-80 configuration are shown in Figure 2-1.

The standard tabletop VPR-80 can be placed on any flat, level surface capable of sustaining its basic weight of 168 lb (73.6 kg), plus the weight of tape, reels, and any internally mounted accessories. The four mounting feet of the cabinet provide approximately one inch of clearance between the bottom of the cabinet and the mounting surface. With 6000-ft (1800-m) capacity NAB tape reels installed, overall width is 23.75 in. (581.9 mm), overall height is 24.125 in. (612.8 mm), and depth is 21.0 in. (533.4 mm).

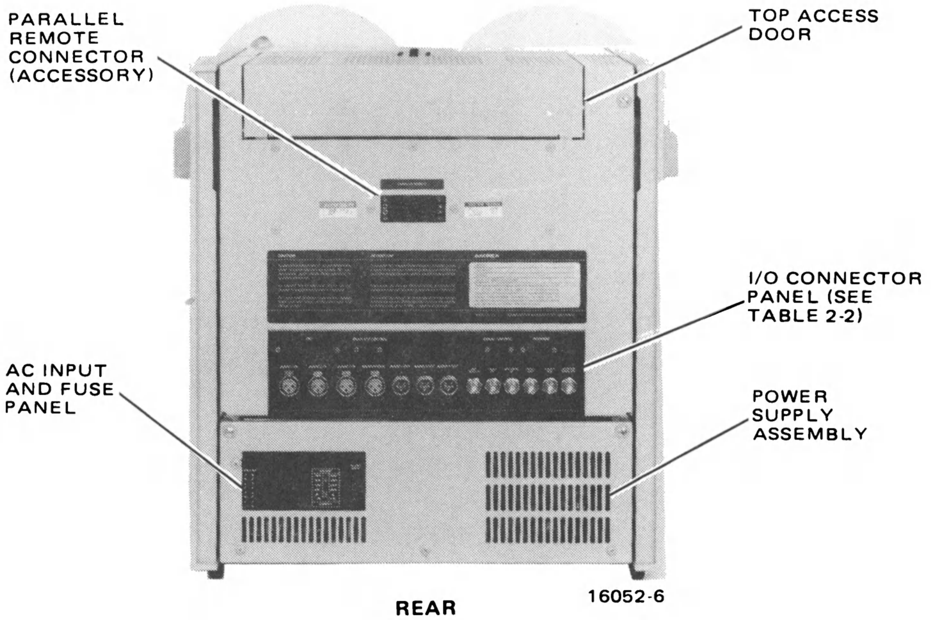
Access to tape transport components so that tape can be threaded is obtained by lowering the hinged transport front cover assembly. Doors on top of the VPR-80 cabinet provide access to edge-mounted controls on the Audio PWA and plug-in PWAs in the card cage. The entire rear door assembly, which includes the card cage, hinges open for access to audio electronics, motor drive amplifiers (MDAs), the rear of the transport assembly, and the card cage motherboard. Access to Control Panel PWAs, AST Driver PWA, tape speed control potentiometer, speaker, and other components beneath the primary control panel is obtained by pivoting the entire control panel assembly forward. Power and all I/O connections are made at the rear of the VPR-80 cabinet.

Clearances around the VPR-80 which must be provided for operational and maintenance access are covered in the *Installation and Operation* manual.

Instructions for gaining access to subassemblies and PWAs are given in Section 4, Part I of this manual. Detailed instructions on removal of subassemblies from the VPR-80 and disassembly (where applicable) are given in the appropriate sections of Part II.


SCANNER ASSEMBLY (SEE FIGURE 2-6)
SECONDARY CONTROL PANEL (SEE TABLES 3-4 AND 3-5)
TRANSPORT ASSEMBLY (SEE FIGURE 2-5)
PRIMARY CONTROL PANEL (SEE TABLES 3-1, 3-2, AND 3-3)
AMPEX
AMPEX
16052-5

FRONT


PARALLEL REMOTE CONNECTOR (ACCESSORY)
TOP ACCESS DOOR
I/O CONNECTOR PANEL (SEE TABLE 2-2)
AC INPUT AND FUSE PANEL
POWER SUPPLY ASSEMBLY
16052-6

REAR

Figure 2-1. VPR-80 Front and Rear Views

2-5 Rack-Mounted

No kit of adaptive parts is required for rack mounting the VPR-80. Only side panels and four mounting feet the VTR chassis must be removed; the VTR is then mounted with common hardware. Serviceability of the rack-mounted VPR-80 can be enhanced by installation of the rack-mount slide/turntable accessory. The turntable is mounted on slides in the rack, thus permitting the VTR to be moved outside the confines of the rack, and then pivoted so that all areas within the VTR are accessible.

2-6 Consolette

The VPR-80 consolette-mounted configuration is shown in Figure 2-2. The consolette accessory is mounted on casters and can therefore be easily moved from one studio location to another. In addition to the VPR-80, the consolette also accommodates the time-base corrector and video monitoring equipment, and thus cables between these three components need not be disconnected when the consolette is moved. Maintenance access to the consolette-mounted VPR-80 is facilitated by the consolette turntable which permits the VTR to be turned in place.

2-7 Pedestal-Mounted

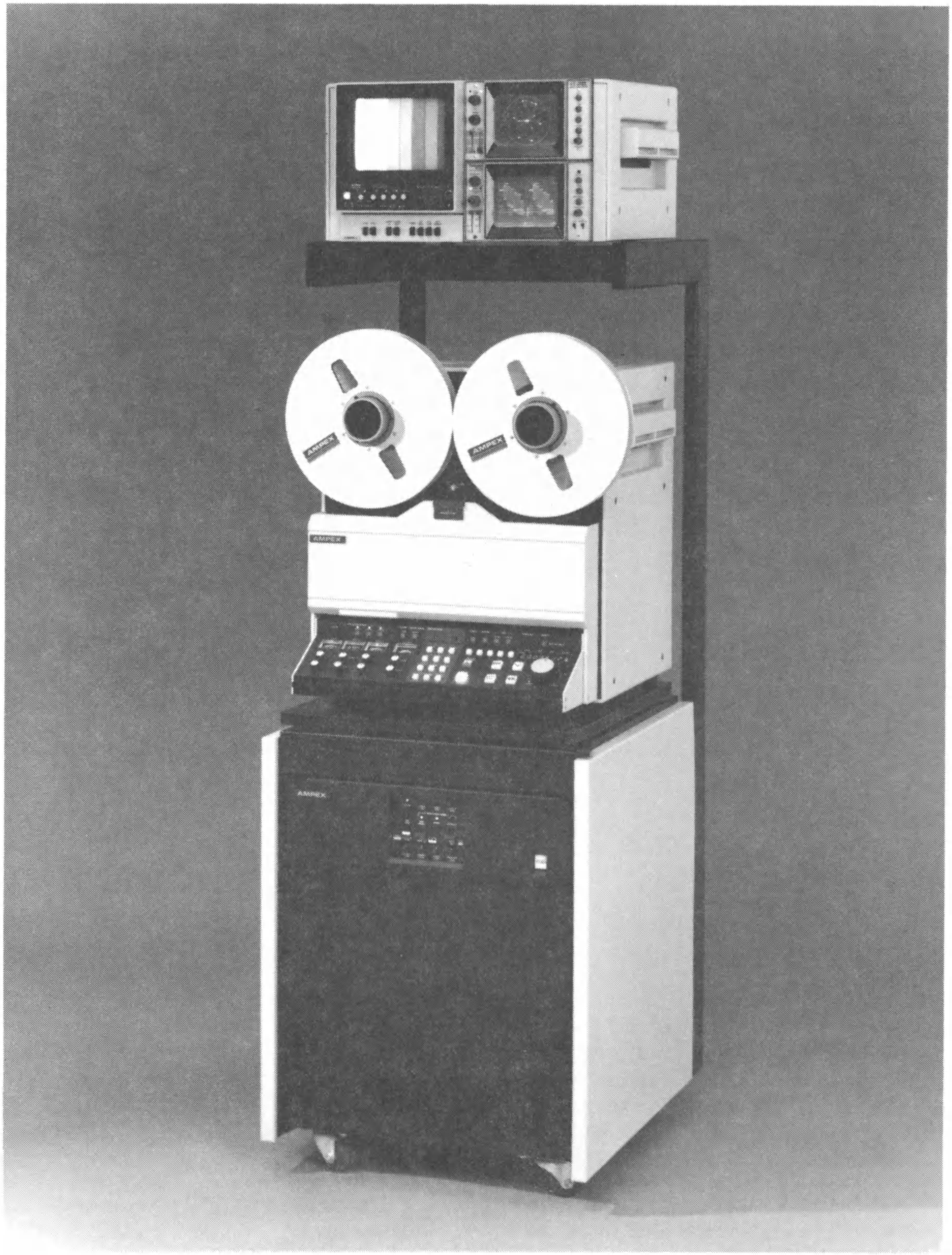
The VPR-80 pedestal-mounted configuration is shown in Figure 2-3. The pedestal accessory is also mounted on casters and provides mobility for the VPR-80 and time-base corrector. The pedestal-mounted VPR-80 and TBC can be quickly and conveniently moved as required within the studio environment.

2-8 Studio Consoles

Three studio console configurations are available, and provide either side car or overhead monitoring. All console configurations include two-channel monitor switching for time sharing of picture, waveform, vectorscope, and audio monitoring.

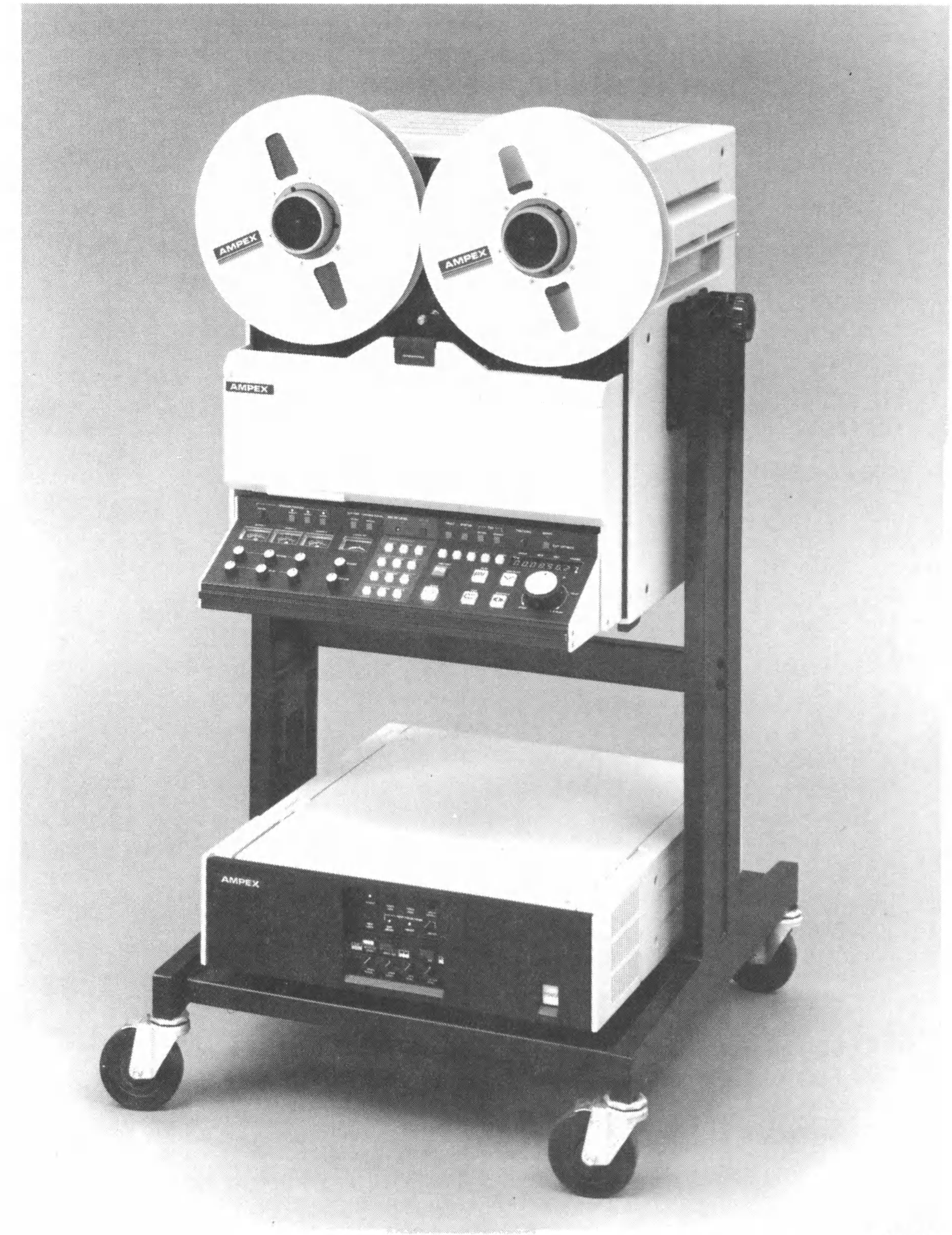
The side car console is shown in Figure 2-4. The VPR-80 and the TBC are mounted on the left-hand side, and video monitoring equipment is mounted in the side car on the right. The VPR-80 is mounted on a slide tray which permits the VPR-80 to be turned in place for maintenance access. Video monitoring equipment in the side car includes picture monitor, vectorscope, waveform monitor, and monitor switching panel. Storage space is provided in the bottom half of the console for other equipment. The side car console is mounted on casters for easy moves from one studio location to another.

The overhead bridge console, shown in Figure 2-5, provides all the features of the side car console, and in addition it contains a larger size (14-inch diagonal) picture monitor. The bridge also provides a dual-channel, high-fidelity audio monitoring system.



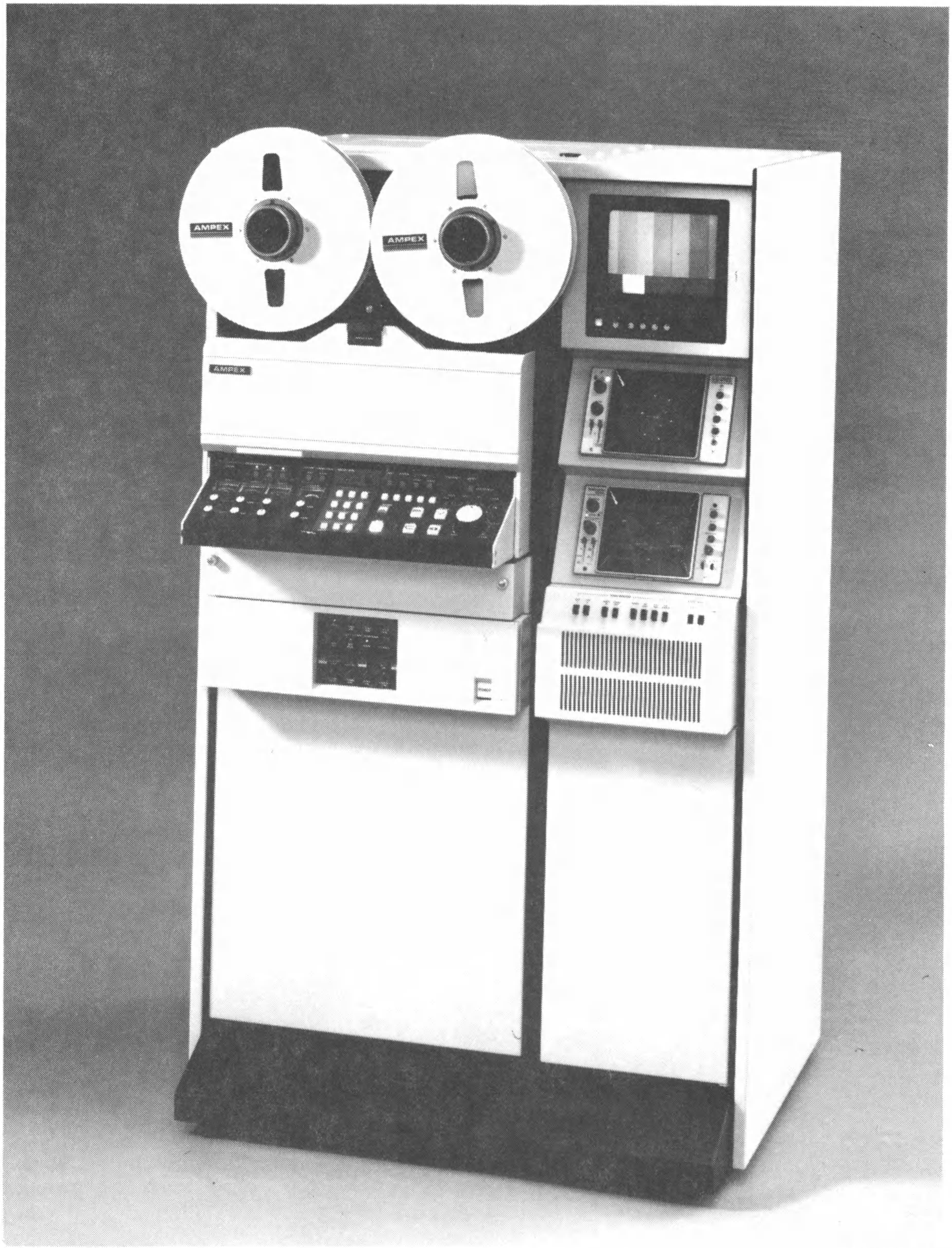
16255-19

Figure 2-2. VPR-80 in Consolette-Mounted Configuration



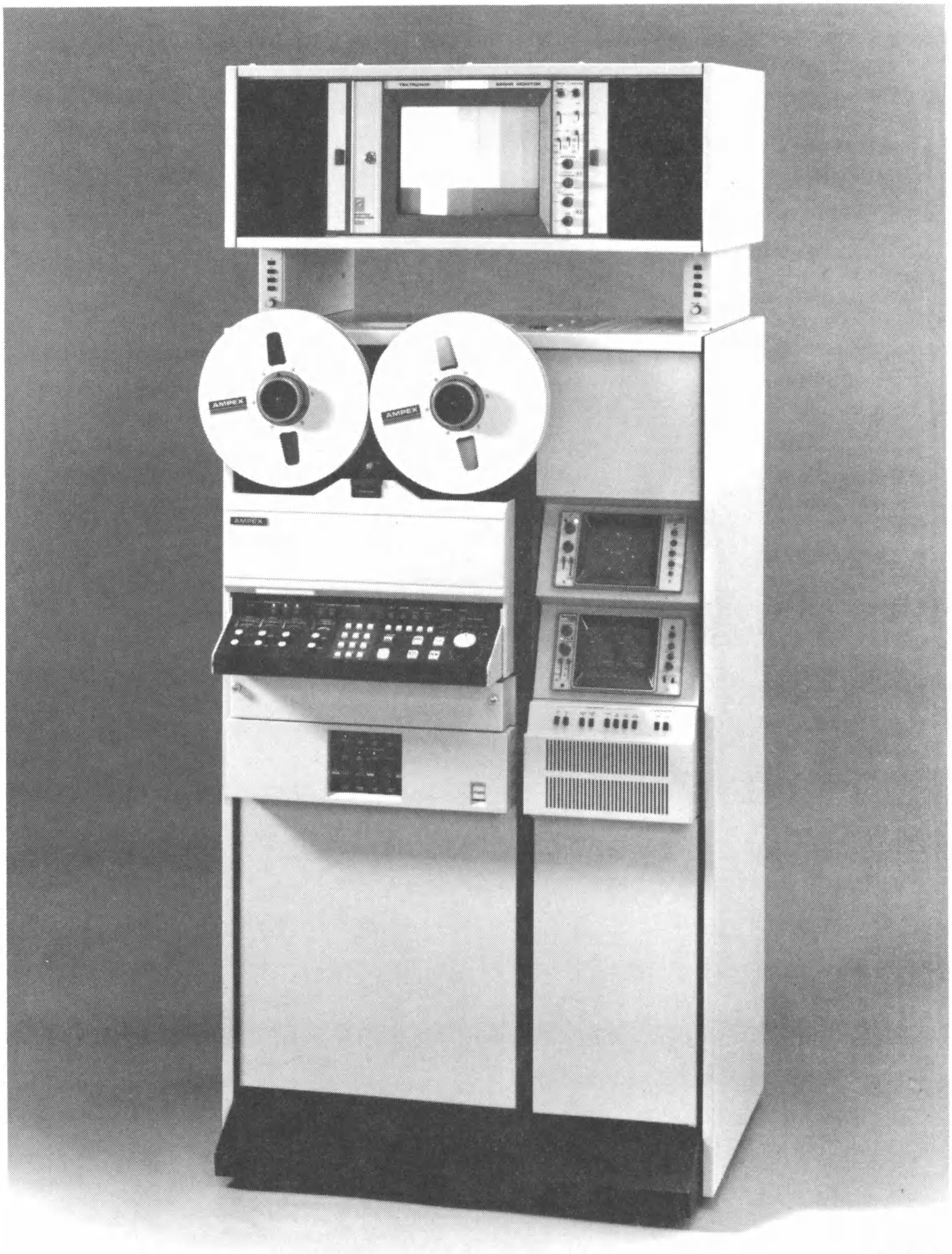
16255-24

Figure 2-3. VPR-80 in Pedestal-Mounted Configuration



16282-11

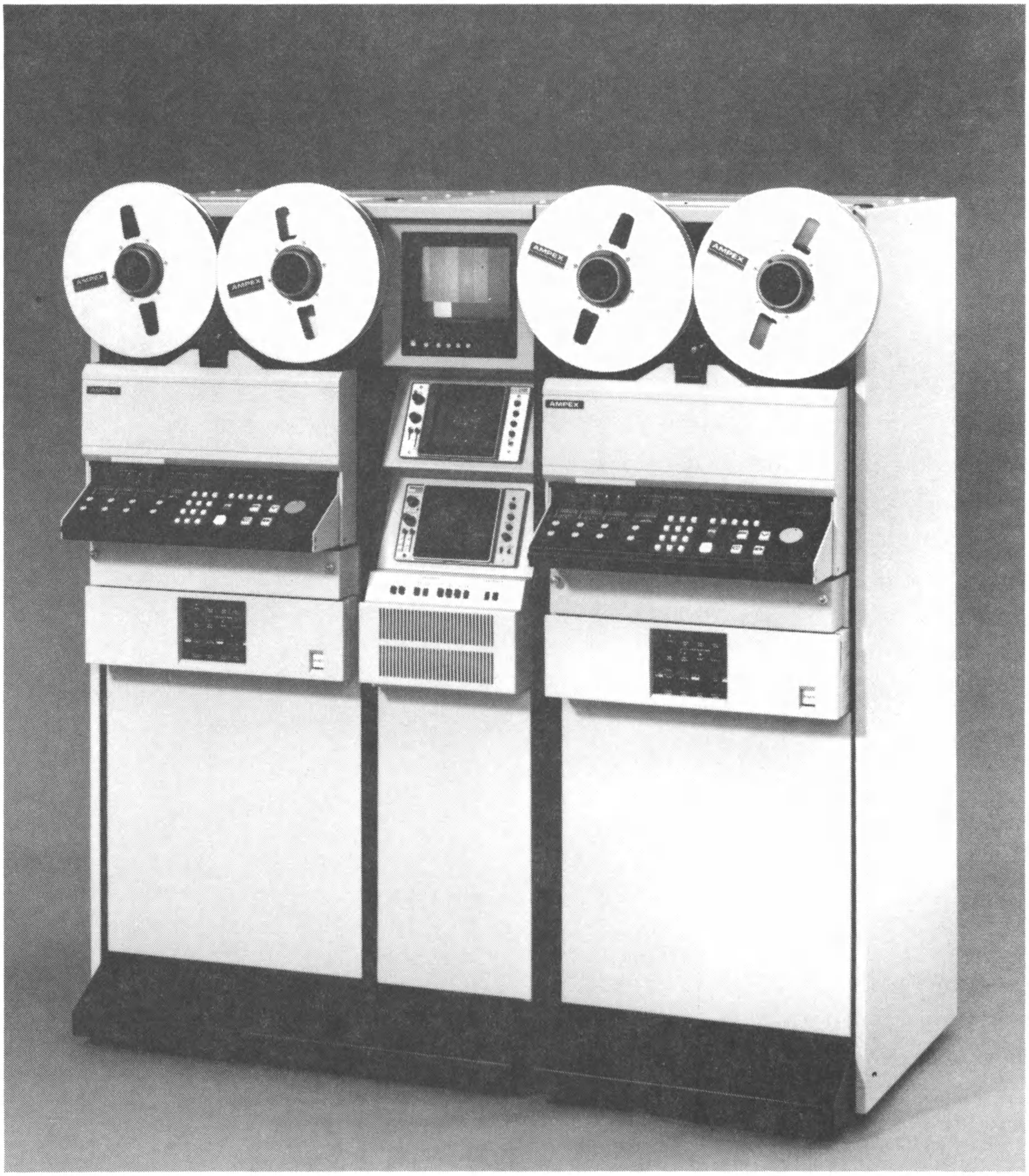
Figure 2-4. Side Car Console



16282-12

Figure 2-5. Overhead Bridge Console

The dual console, shown in Figure 2-6, consists of a side car console-mounted VPR-80/TBC and a second VPR-80/TBC in an integrated rack on the opposite side of the side car. All monitoring equipment in the side car can be quickly and conveniently switched from one system to the other.



16282-13

Figure 2-6. Dual Console

2-9 Power Supply

The power supply and regulator assembly is located on a separately removable tray in the bottom of the VPR-80 cabinet. It contains three output connectors for power distribution. A 36-pin connector supplies power via cable harness to the card cage motherboard. A 24-pin connector supplies power to the MDA assembly, and a 3-pin connector supplies power to the AST driver assembly. There are four individual power cables from the MDA assembly to the reel, capstan, and scanner motors.

Detailed instructions for removal of the power supply and regulator assembly from the VPR-80 are included in Section 2, Part II of this manual. After the power supply has been removed from the VPR-80, it can be electrically reconnected with the aid of one extension cable. Thus, output measurements can be made and detailed troubleshooting can be done with normal operating loads on the power supply.

A diagram of power distribution is also included in Section 2, Part II.

2-10 Card Cage Assembly

The card cage assembly consists of a motherboard assembly with six printed wiring assembly (PWA) connectors, mounting hardware, and a complement of five standard plus two optional (Serial Remote and Time-Code System) plug-in PWAs. Format and test controls and test points are located on the top edges of the PWAs. A hinged door on top of the VTR cabinet provides access to these PWAs. Table 2-1 shows PWA locations.

2-11 Audio System

The audio system consists of the Audio PWA, a loudspeaker (and headphone jack) for audio monitoring, three each line input and output connectors, and a microphone input connector. The Audio PWA is parallel to and directly in front of the card cage assembly. The Audio PWA contains all the record/playback electronics for the three audio channels and the control track. The loudspeaker is mounted beneath the control panel assembly, and the headphone jack is accessible through a cutout in the left-hand side of the control panel assembly.

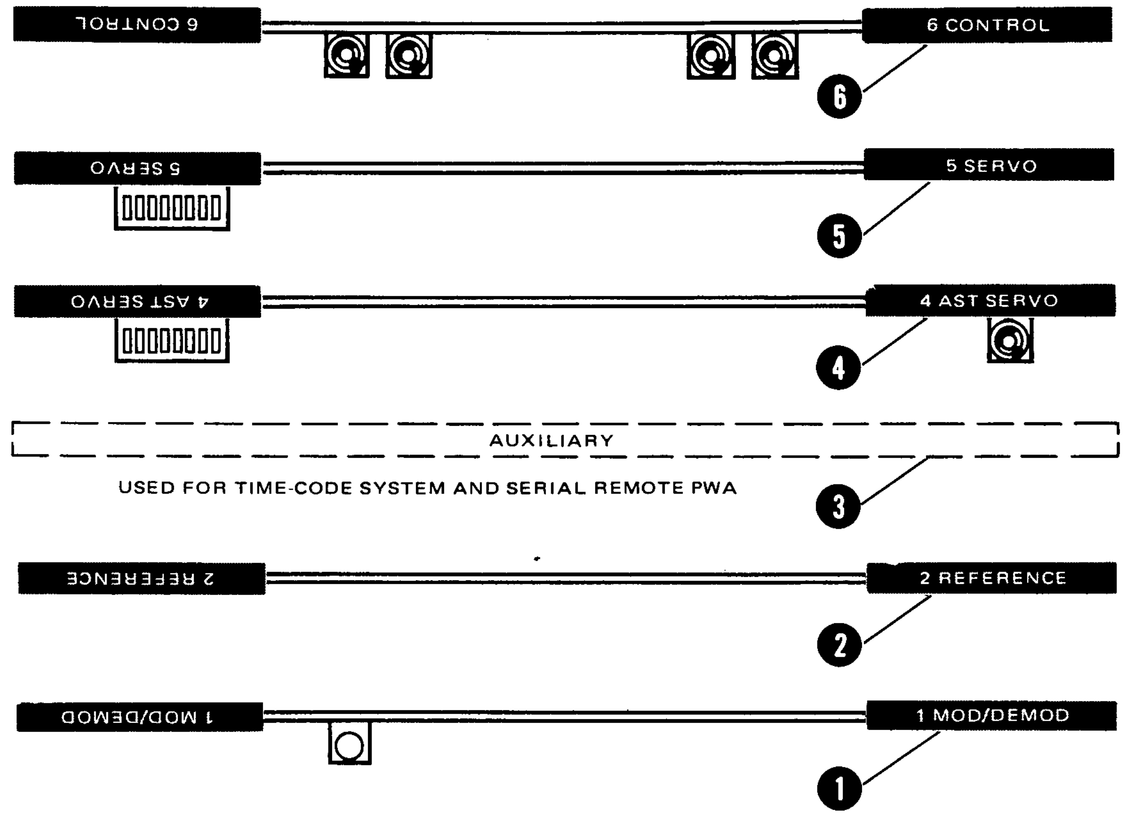
Detailed instructions for removal of the Audio PWA from the VPR-80 are included in Section 4, Part II of this manual.

2-12 Control Panel Assembly

The control panel assembly is composed of a primary and a secondary control panel. Controls and indicators used for record and playback operation and during editing procedures are located on the primary control panel. The panel is divided into three sections: input/output level controls and metering, mode enable controls, and transport mode controls. Controls and indicators used less frequently, such as during special operating circumstances or during adjustment procedures, are located on the secondary control panel directly above the primary controls.

Detailed instructions for removal of the control panel assembly from the VPR-80 are included in Section 6, Part II of this manual. Disassembly instructions for access to control panel PWAs and components mounted on the control panel are included.

Table 2-1. Card Cage Assembly PWA Locations



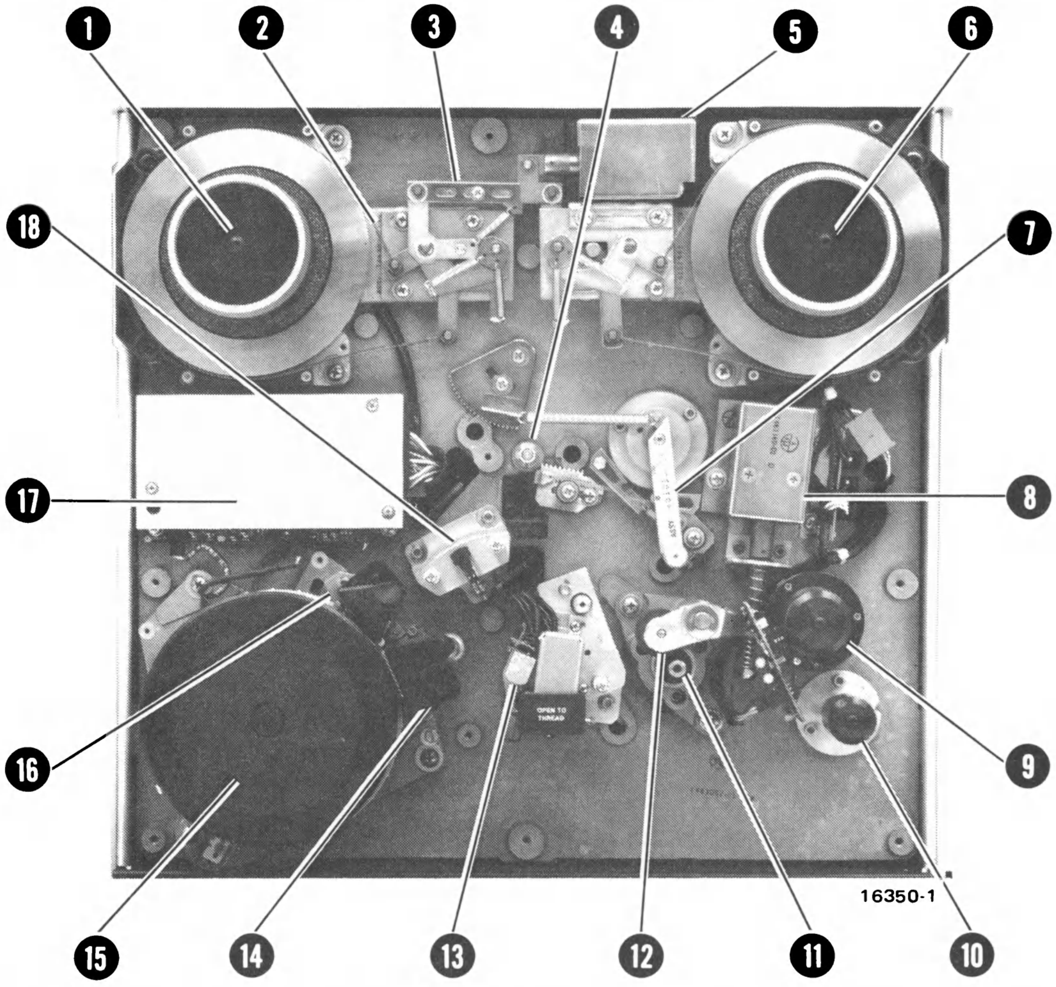
Index No.	Reference Designator	Printed Wiring Assembly (PWA)	Part Number
1	PWA 1	Mod/Demod (525)	1450206
1	PWA 1	Mod/Demod (625)	1450216
2	PWA 2	Reference (NTSC)	1450346
2	PWA 2	Reference (PAL-M)	1450363
2	PWA 2	Reference (PAL/SECAM)	1450356
3	PWA 3	(Reserved for Accessory PWAs)	
4	PWA 4	AST Servo	1450256
5	PWA 5	Servo	1465234
6	PWA 6	Control	1465505

2-13 Transport Assembly

The transport assembly consists of a top plate and all tape handling and head assemblies for the recorder. A hinged front cover provides access to the tape threading path and protects transport components.

2-14 Tape Handling Subassemblies

Subassemblies described below are shown in Figure 2-7.



1 Supply Turntable
2 Brake Band
3 Brake Linkage
4 Fixed Guide
5 Brake Solenoid
6 Takeup Turntable
7 Tension Arm
8 Pinch Roller Solenoid
9 Timer Idler
10 Idler
11 Capstan
12 Pinch Roller
13 Audio and CT Heads
14 Exit Guide
15 Scanner
16 Entrance Guide
17 Record Ampl. & Edit Erase PWA
18 Video Erase Head

Figure 2-7. Transport Assembly Components

2-15 **Reel Motors and Turntable Assemblies.** Dc motors are used to drive supply and takeup reels. Tape reels are secured with hold-downs on reel motor turntables. The VPR-80 is insensitive to differences in reel diameters: The transport handles 11.75-inch, 2-hour reels containing 6000 ft (1800m) of tape and spot reels containing 15 or 30 seconds of tape with equal smoothness. VPR-80 reel hubs are designed with a high peripheral mass, and servo gains are set to anticipate static and dynamic inertia values of that mass. The value of the mass is great enough so that additional inertia of the tape reels, large or small, is sensed only as a small difference in the anticipated mass. The result is smooth tape handling, regardless of reel diameter.

Detailed instructions for removal of reel motors and turntable assemblies from the VPR-80 are included in Section 7, Part II of this manual.

2-16 **Reel Brakes.** The parking brake assembly is composed of a solenoid, two sets of brake linkage, and two brake bands which bear on the supply and takeup reel turntables. Brake bands are lined with a rubberized cork material.

With power off, the solenoid plunger is extended, and two springs in each set of brake linkage are loaded. Loaded brake linkage springs thus cause brake bands to bear on reel turntables. When brakes are released, the solenoid plunger is withdrawn, simultaneously actuating both sets of brake linkage. The two pairs of springs are thus unloaded, releasing brake bands from turntables. Brake force on turntables is separately adjustable, as is brake timing and clearance of bands around the turntables. Detailed instructions for parking brake adjustments are given in Section 7, Part II of this manual.

2-17 **Tape Guides, Rollers, and Idlers.** Tape from the supply reel first passes over a rigidly mounted, small diameter guide which provides initial edge guiding. The tape then goes around the tension arm subassembly which alters tape travel direction and senses tape tension. The tape then passes over the longitudinal video erase head and around the scanner assembly. Entrance and exit guides (part of the scanner assembly) provide proper positioning of the tape at the entrance to and exit from the scanner guide band. After exiting the scanner, the tape passes by the longitudinal audio erase head and control track and audio record/playback heads. Guides, located on each longitudinal head subassembly, position tape against the heads. In addition, a hinged audio shield is used in conjunction with the control track and audio record/playback heads. The tape is held in contact with the capstan by the pinch roller which is engaged by a solenoid during play, record, and slow-motion modes of operation. The tape then passes around the timer idler and a rigidly mounted, large diameter roller which alters tape travel direction toward the takeup reel.

Detailed instructions for replacing rotating guide assembly bearings are given in Section 7, Part II of this manual.

2-18 **Capstan.** The capstan controls tape speed, and it is directly driven by a servoed dc motor. An optical tachometer supplies capstan speed information for the servo. During record operations, the capstan determines track spacing. During playback, the capstan ensures accurate alignment of recorded tracks to the video head. Timing information is taken from the control track.

Detailed instructions for removal of the capstan from the VPR-80 are included in Section 5, Part II of this manual.

2-19 **Tension Arm**. The tension arm assembly enables the servo system to maintain proper tape tension throughout the transport at all times. This is particularly visible at moments when mode commands require a change in tape speed and/or direction.

The tension arm assembly is essentially a spring-loaded bellcrank which is displaced in rotational position by changes in tape tension in the transport. A photopotentiometer in the arm assembly transmits position displacement information to the servo system. The servo system uses this feedback information, combined with capstan tach output, to govern speed (and direction) of the reel motors.

Detailed instructions for removal of the tension arm assembly from the VPR-80 are included in Section 5, Part II of this manual.

2-20 Tape Timer Idler

The tape timer idler is rotated by tape motion. A two-channel concentric tachometer disk is used to provide tape timing information. A tape-in-path (TIP) sensor is an integral part of the tape timer idler assembly. As long as the TIP sensor indicates that tape is threaded, normal operation is enabled, and the servo system microprocessor continuously computes tape pack diameter from reel tach information. This computation enables the near end-of-tape (EOT) point to be sensed at either end of the tape. Tape motion will automatically stop before tape runs off either end. (Operator may override this feature.) When the EOT point is reached, dynamic reel braking is initiated. If tape is completely run off the transport, the TIP sensor immediately causes the control system to place the VPR-80 in stop mode.

Detailed instructions for removal of the tape timer idler from the VPR-80 are included in Section 6, Part II of this manual.

2-21 Scanner Assembly

Major components of the scanner assembly are the servo-controlled dc motor, the stationary lower drum, the rotating upper drum, and entrance and exit tape guides. As shown in Figure 2-8, the scanner has positions for six heads in accordance with SMPTE/EBU Type C format specifications. The VPR-80 scanner contains four dummy heads and two active heads (edit erase and AST record/playback) spaced 120° apart. Heads are individually replaceable and can be quickly and easily optimized after replacement. The scanner also contains rotary transformers to transfer signals between rotary and stationary elements of the scanner assembly. Because the tape wrap around the scanner is less than 360°, there is a period of scanner rotation in which the video record/play head does not contact the tape, as shown in Figure 2-8. This is the vertical interval dropout period.

Scanner adjustments that do not require removal of the scanner from the VPR-80 are covered in Section 4, Part I.

Detailed instructions for removal of the scanner assembly from the VPR-80 are included in Section 5, Part II of this manual. Disassembly instructions for cleaning and replacement of components are also included.

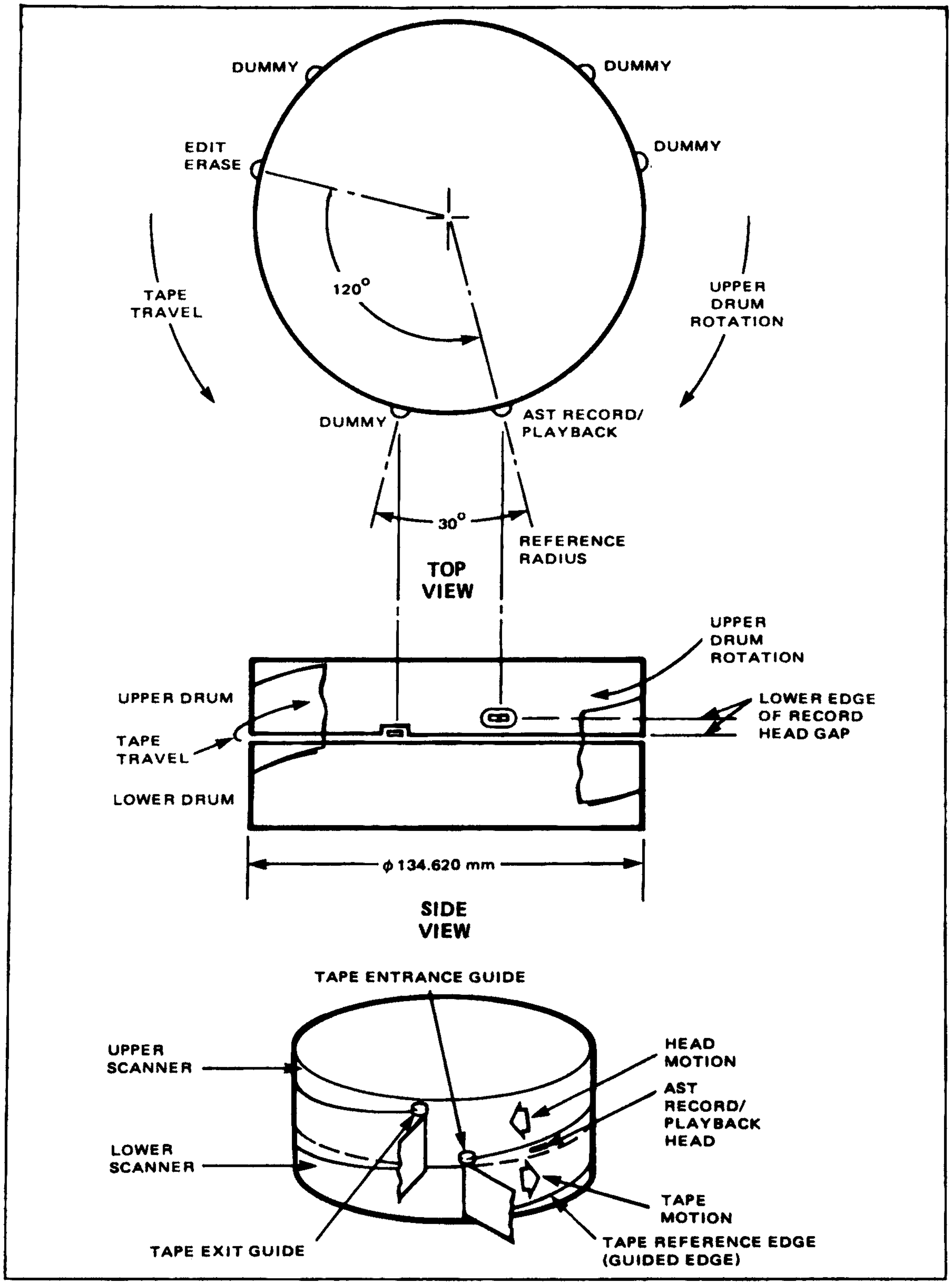


Figure 2-8. VPR-80 Scanner Assembly

2-22 Longitudinal Heads

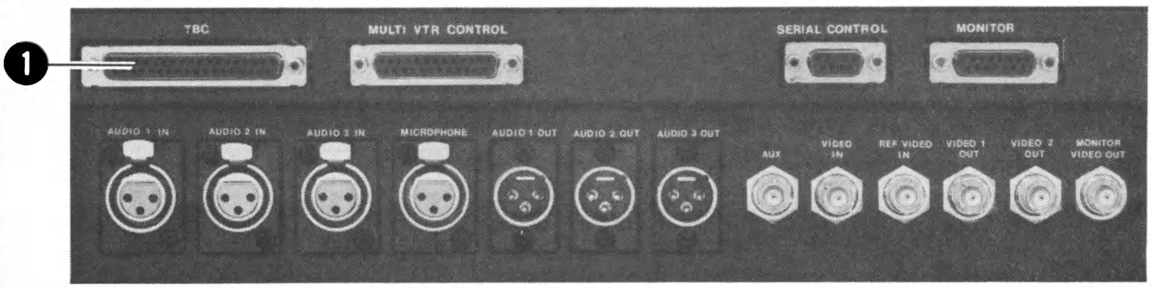
Two longitudinal head assemblies are mounted on the tape transport. The upper assembly is the video erase head assembly. The lower assembly is composed of two head stacks. The first stack consists of erase heads for each of the audio channels, and a head for control track erase. The second stack has record/playback heads for each of the audio channels and a record/playback head for the control track. Tape passes between this head stack and a hinged shield which must be opened in order to thread the tape.

Detailed instructions for removal and replacement of longitudinal head stacks are given in Section 4, Part II of this manual.

2-23 Input/Output Connections

All signal and power connections are made at the rear of the VPR-80 (refer to Figure 2-1). All I/O signal connections are made at the I/O connector panel with exception of the parallel remote control panel. If accessory parallel remote control capability is included in the VPR-80, the remote control cable is connected at the PARALLEL REMOTE connector on the upper rear panel of the VPR-80 cabinet. The primary power cord is connected at the ac input and fuse panel (also shown in Figure 2-1). Table 2-2 lists all connections made at the I/O connector panel. Further details, such as connector pin contact assignments, are given in the *VPR-80 Installation and Operation* manual.

Table 2-2. Input/Output Connections

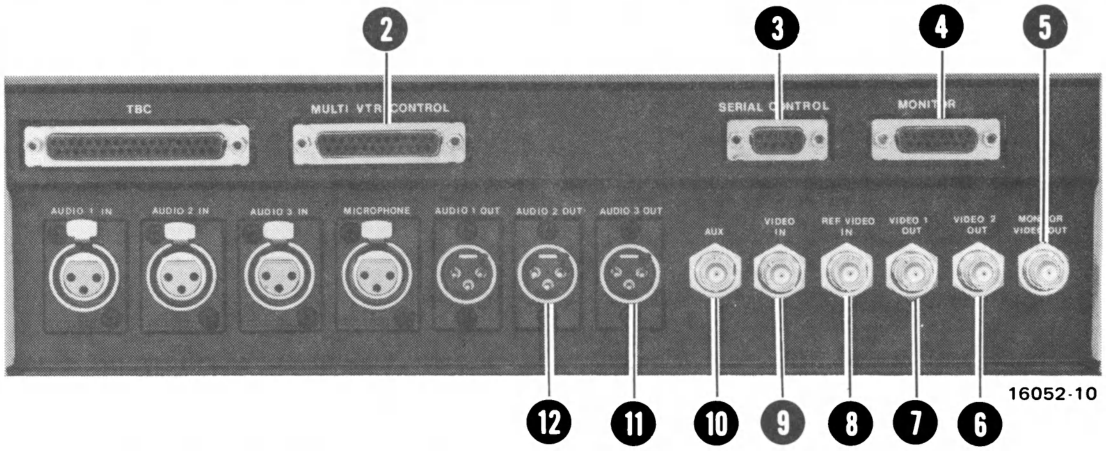


Index No.	Reference Designator	Name	Type	Description
*	J1 (Motherboard)	PARALLEL REMOTE	Burndy 75-pin	Connector for parallel remote control panel.
1	J2 (Motherboard)	TBC	AMP, or equiv., D Series, 37-pin	Time-base corrector (TBC) accessory interface connector.

*Not shown (PARALLEL REMOTE connector is located on upper rear panel of VTR cabinet).

(Continued next page)

Table 2-2. Input/Output Connections



Index No.	Reference Designator	Name	Type	Description
2	J3 (Motherboard)	MULTI VTR CONTROL	AMP, or equiv. D Series, 25-pin	Connector for sending play commands when VTR is used as editor in multiple machine automatic edits, and for receiving play commands when VTR is used as an editing source in multiple machine automatic edits. Also used for multi-VTR search. Also contains 14 pins for simple remote control connections.
3	J4 (Motherboard)	SERIAL CONTROL	AMP, or equiv., D Series, 9-pin	Provides RS-422A-compatible connection to serial control bus of a microprocessor-based videotape editing system (accessory).
4	J5 (Motherboard)	MONITOR	AMP, or equiv., D Series, 15-pin	Provides monitor access to four signals: rf envelope, control track, AST error, and frame reference.
5	J13	MONITOR VIDEO OUT	Insulated (75Ω) BNC	Output from video amplifier.
6	J12	VIDEO 2 OUT	Insulated (75Ω) BNC	Output from video amplifier.
7	J11	VIDEO 1 OUT	Insulated (75Ω) BNC	Output from video amplifier.

(Continued next page)

Table 2-2. Input/Output Connections (Continued)

Index No.	Reference Designator	Name	Type	Description
8	J10	REF VIDEO IN	Insulated (75Ω) BNC (terminated)	External video reference input.
9	J9	VIDEO IN	Insulated (75Ω) BNC (terminated)	Video input. Accepts 0.5 to 2.0 Vp-p (1.0 Vp-p nominal).
10	J8	AUX	Insulated (75Ω) BNC	Auxiliary video input for user auxiliary video input.
11	J7	AUDIO 3 OUT	XLR	Audio channel 3 line output (less than 50Ω impedance).
12	J6	AUDIO 2 OUT	XLR	Audio channel 2 line output (less than 50Ω impedance).
13	J5	AUDIO 1 OUT	XLR	Audio channel 1 line output (less than 50Ω impedance).
14	J4	MICROPHONE	XLR	Microphone input (200Ω impedance). In VPR-80 as-delivered configuration, microphone input is disconnected. Refer to Section 4, Part II for instructions on connecting microphone input.
15	J3	AUDIO 3 IN	XLR	Audio channel 3 line input (50KΩ impedance).
16	J2	AUDIO 2 IN	XLR	Audio channel 2 line input (50KΩ impedance).
17	J1	AUDIO 1 IN	XLR	Audio channel 1 line input (50KΩ impedance).

2-24 FUNCTIONAL DESCRIPTION

The VPR-80 provides one-inch, helical scan, direct color video recordings in accordance with SMPTE/EBU Type C format, which is nonsegmented. That is, one rotation of the scanner records one field of television video. Type C format parameters include:

- Placement and orientation of record tracks on tape
- Scanner, transport, and guiding geometry required to produce record tracks
- Electronic specifications, including parameters for audio, video, and control track signals

A section of magnetic tape with Type C format recording is shown in Figure 2-9. The drawing shows locations of helical (angled) tracks and longitudinal tracks. Longitudinal tracks (those parallel with the edge of the tape) are recorded by the stationary audio and control track head stack. Helical video tracks are recorded by heads on the rotating scanner in the upper portion of the scanner assembly. Sync track and EBU audio channel 4 track are not included. Track layout is essentially the same between NTSC and PAL/SECAM video standards. For specific format details (dimensions, parameters, etc.), refer to SMPTE publications C98.18, C98.19, C98.20, and RP86, or to EBU Format C Technical Information, sheet 7.

As shown in the simplified block diagram (see Figure 2-10), most of the principal electronic subsystems of the VPR-80 are interconnected via system data and address bus lines. The 8-bit system data bus and the system address/control bus provide the principal communication paths between control panels and control and timing logic, audio electronics, video mod/demod circuitry, reference timing circuitry, servo control logic, and accessory PWAs.

The VPR-80 employs two microprocessors: one on the Control PWA and one on the Servo PWA. Both are Motorola Type MC6802. Capabilities and operating characteristics of the MC6802 and its associated family of chips are well documented by the manufacturer. Refer to the MC6800-family product literature for this information.

The Control PWA contains the primary microprocessor with associated 32K x 8 capacity read-only memory (ROM) for storage of operational, diagnostic, and housekeeping routines. The control subsystem also contains tape timer and time display circuitry. The principal interface between the VTR operator and the control subsystem is at the control panel. Most of this communication is through the system bus. A few variable analog controls such as tape speed control (shuttle potentiometer) are routed directly from the control panel to the Control PWA.

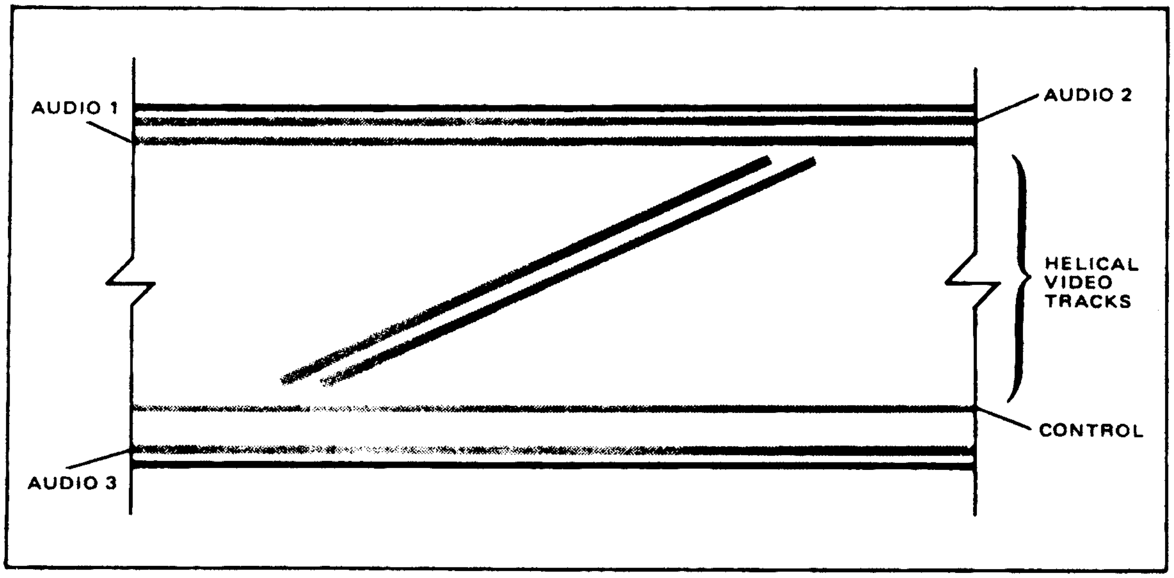


Figure 2-9. SMPTE/EBU Type C Helical Scan Recording Format (without Options)

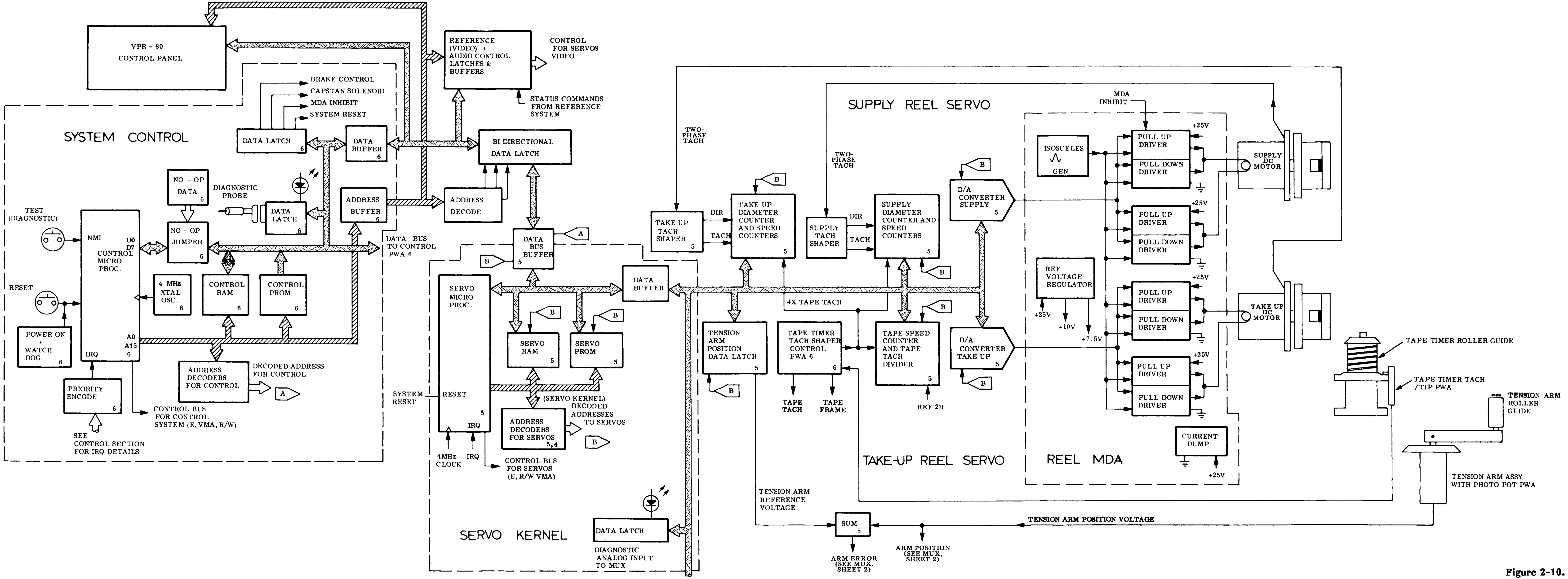


Figure 2-10. VPR-80 Simplified Block Diagram (Sheet 1 of 2)

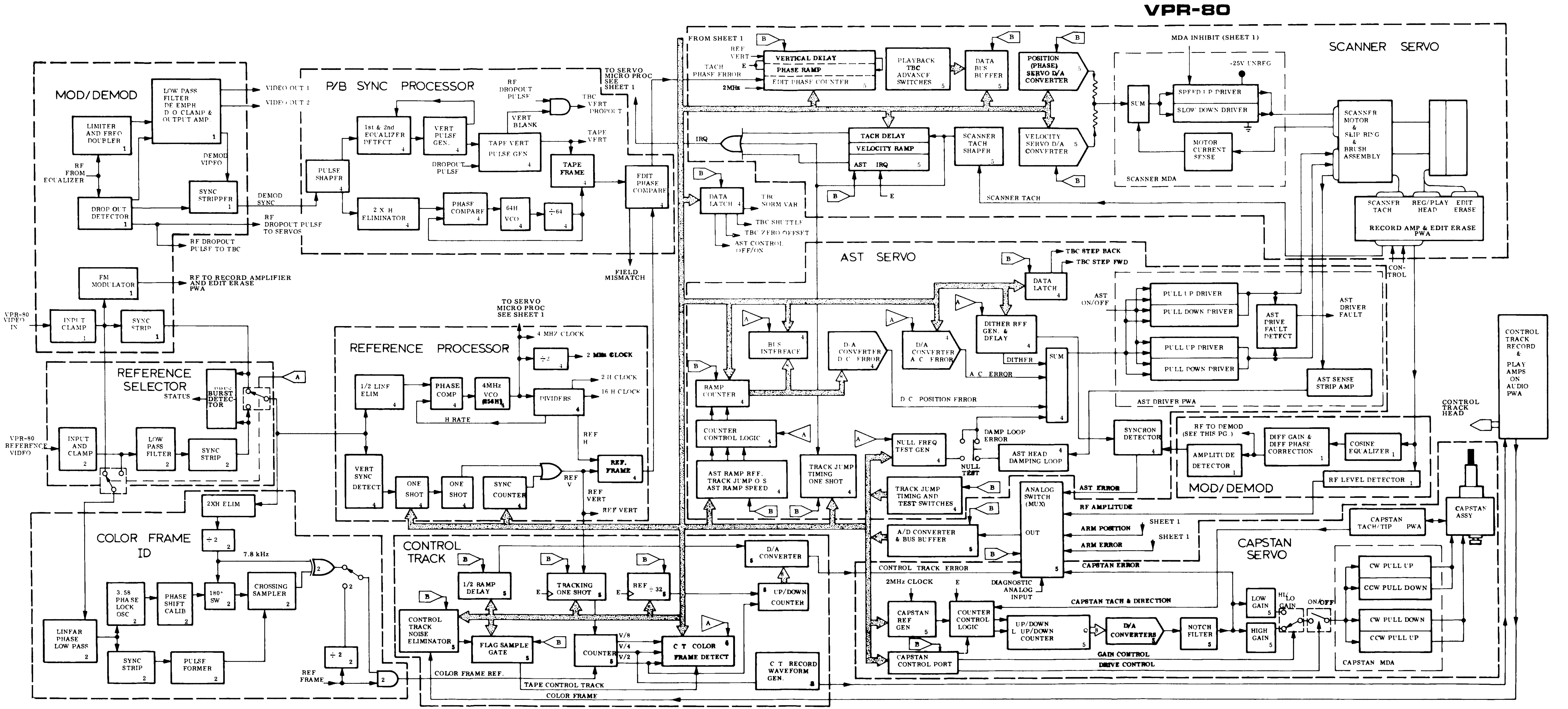


Figure 2-10.
VPR-80 Simplified Block Diagram
(Sheet 2 of 2)

The primary microprocessor services manually entered commands from the control panel. Mode change commands, requiring an immediate response in tape speed and direction, are implemented by a second microprocessor in the servo subsystem. The second microprocessor (on the Servo PWA) communicates with the analog domain of the servo subsystem through D/A and A/D converters. The control subsystem includes keyboard logic, remote control interfacing, and the tape timer system. Digital control and status information is communicated via bidirectional data, address, and control buses which link the control panel to reference, video, audio, and servo subsystems. Each subsystem on the system bus lines contains interfacing ports to latch command information and encode status and response data.

The system bus is composed of 8 data lines, address lines, and a number of control lines derived from decoded addresses. The system bus is the primary communication path for information exchange between major VPR-80 subsystems. There are, however, a number of direct paths among PWAs. These are principally analog adjustments entered at the control panel, such as record and play levels, shuttle speed, and rf equalization, which are applied directly to the PWA involved.

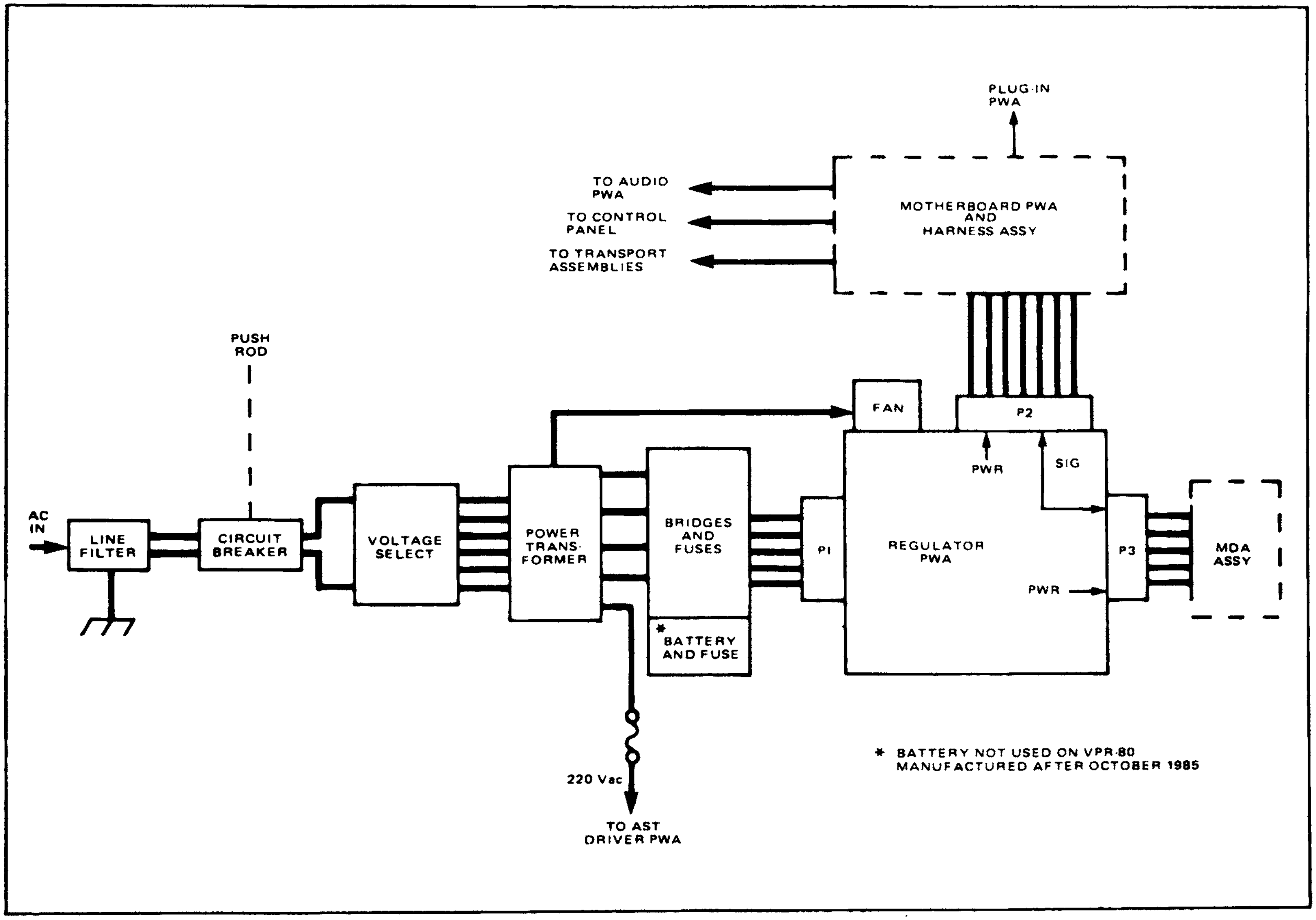
For explanation and illustration purposes, the VPR-80 is divided into six major subsystems: power, video, audio, servo, control, and transport. Each subsystem is briefly described in the following paragraphs, and is treated in detail with more complex diagrams in Part II.

2-25 Power System

The VPR-80 power system is shown in Figure 2-11. It is composed of a conventional linear power supply and regulator assembly. The power supply accepts primary power from 100 to 260 Vac. Power transformer primary windings are connected in parallel for 100- to 130-volt operation, and in series for 200- to 260-volt operation. Two jumper plugs are used for selecting appropriate input voltage windings within the ranges of 100 to 130 Vac or 200 to 260 Vac. Instructions for installation of the line voltage select jumper plugs are placarded on the ac input and fuse panel at the rear of the VPR-80 cabinet. Both sides of the ac input are isolated by a circuit breaker which acts as a power on/off switch.

The power supply furnishes five secondary outputs: 220 Vac, +11 Vdc, +10.5 Vdc, and ±25 Vdc. The 220 Vac output is routed directly to the AST Driver PWA, and dc outputs are routed to the Voltage Regulator PWA. As shown in Figure 2-12, the +10.5 Vdc output is supplied to the Capstan/Scanner motor drive amplifier (MDA) and is the input to the +5-volt regulated logic supply. The +11 Vdc output is used by local control system lamps, and supplies power requirements of remote control systems which may be included in the VTR configuration. The ±25 Vdc outputs are supplied to both reel motors and to the ±15-Vdc regulators. Unregulated +25 Vdc is furnished to the Reel and Capstan/Scanner MDAs.

Battery backup for protection of the contents of dynamic RAM storage is also part of the power system on VPR-80s manufactured prior to October 1985. The battery is located on the power supply chassis, and the battery charger is located on the Voltage Regulator PWA. On VPR-80s manufactured ofter October 1985 the battery



* BATTERY NOT USED ON VPR-80
MANUFACTURED AFTER OCTOBER 1985

Figure 2-11. Power System Simplified Block Diagram

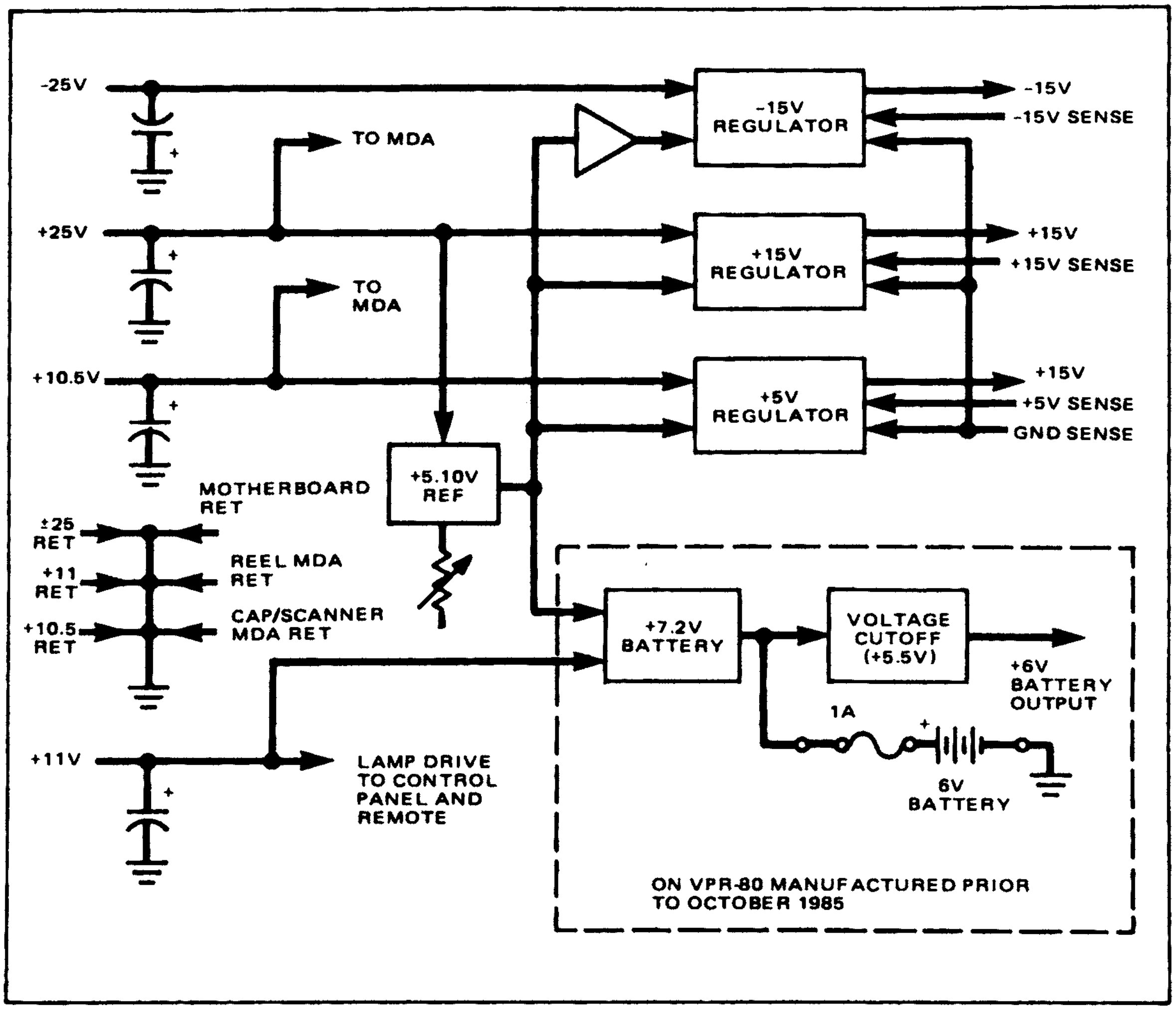


Figure 2-12. Voltage Regulator PWA Simplified Block Diagram

is not included and the battery charger has been removed from the Voltage Regulator PWA. The +11 Vdc supply powers the battery charger. Additional regulators on individual PWAs provide isolation and more precise regulation, where required.

The power system is described in detail in Section 2, Part II of this manual.

2-26 Video System

The video system is composed of the Mod/Demod PWA, Reference PWA, Record Amplifier and Edit Erase PWA, and Preamplifier PWA. A simplification of the video system is included in Figure 2-10.

There are two configurations of the video Mod/Demod PWA: one for NTSC and PAL-M video standards (525/60), and one for PAL/SECAM standards (625/50). The video Mod/Demod PWA contains all video input circuitry, level control, modulator circuitry, playback equalizers, and demodulator circuitry, and it produces a demod output. The video system communicates indirectly with the Control PWA. It gets most of its direct controls from the Reference PWA which acts as interpreter. Analog control levels to the Mod/Demod PWA, including record level, rf level, rf metering, and rf equalization, are received directly from the control panel.

The Reference PWA has three configurations: one for 525/60 NTSC, one for 525/60 PAL-M, and one for 625/50 PAL/SECAM standards. The Reference PWA contains video circuitry related to machine referencing. This function is shared by the servo subsystem. The Reference PWA receives the video input signal and the reference video signal, and it has the circuitry which does the switch selection of video or reference input. It does color frame referencing as well as provide a selected composite sync to the servo system. The Reference PWA receives its commands and provides its feedback information to the control system via system bus lines. It also provides discrete command signals from the control system to the Mod/Demod PWA, and any particular feedback information from the Mod/Demod PWA back to the control system.

The Reference PWA also contains demod output video processing which can be used directly by a video monitor. This video processing consists of playback phase-lock oscillator and sync reinsertion circuitry to provide sync through what is normally the dropout region. It therefore produces a signal that a typical video monitor will receive and lock to. This circuitry is not a color corrector, and the video monitor should not be expected to produce true colors. The video monitor should be a fast time constant monitor. If an accessory Time-Code System PWA is included in the configuration, video output from that circuitry will come through the Reference PWA, and from there go to the video monitor.

Theory of operation information and detailed video signal system alignment procedures appear in Section 3, Part II, of this manual.

2-27 Audio System

The three-channel audio system is composed of the Audio PWA, audio record/play head stack assembly, audio monitoring facilities, and interface connector components. Functions of the Audio PWA include control track signal processing, generation of ramped bias for audio and control track heads, and generation of ramped erase frequencies for audio, full-width video, and control track erase heads. Figure 2-13 is a simplified block diagram of the audio system.

The audio system has direct routing to the input/output connector panel where the microphone and three line inputs are inserted and the three audio line outputs are provided. It also has direct communication to the control panel where all analog audio adjustments are made. These include record and play levels, meter drives, and speaker controls. Digital timing and control of the audio system are applied through the bidirectional system bus. The Audio PWA is a transformerless system. It has direct input and output lines. The Audio PWA also contains the analog portion of the control track record and play circuitry. The three audio channels can be applied separately or in any combination to the internal speaker (or a headset) for monitoring.

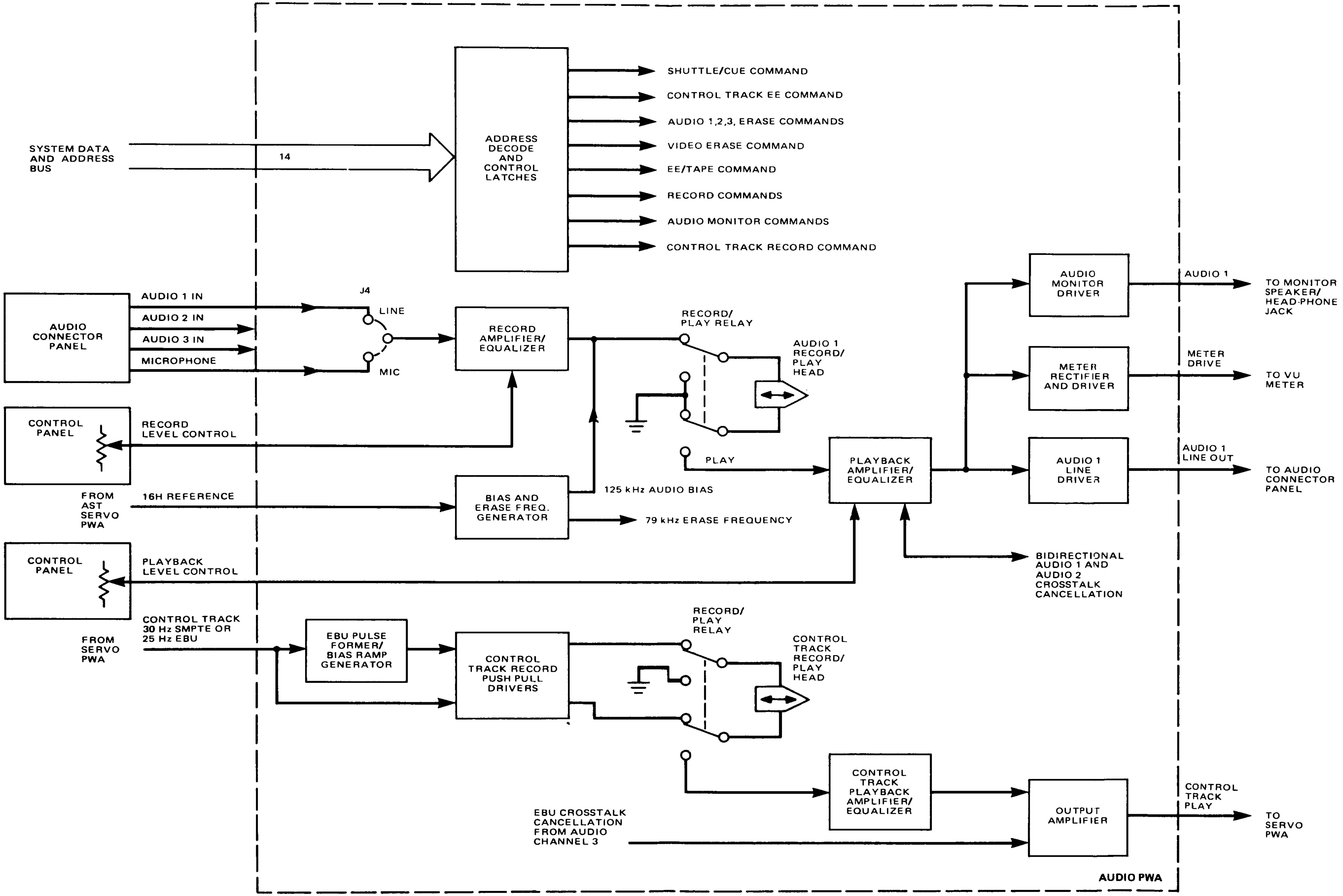

SHUTTLE/CUE COMMAND
CONTROL TRACK EE COMMAND
AUDIO 1,2,3, ERASE COMMANDS
VIDEO ERASE COMMAND
EE/TAPE COMMAND
RECORD COMMANDS
AUDIO MONITOR COMMANDS
CONTROL TRACK RECORD COMMAND
SYSTEM DATA AND ADDRESS BUS
14
ADDRESS DECODE AND CONTROL LATCHES
AUDIO CONNECTOR PANEL
AUDIO 1 IN
AUDIO 2 IN
AUDIO 3 IN
MICROPHONE
J4
LINE
MIC
RECORD AMPLIFIER/ EQUALIZER
RECORD/ PLAY RELAY
AUDIO 1 RECORD/ PLAY HEAD
CONTROL PANEL
RECORD LEVEL CONTROL
PLAY
FROM AST SERVO PWA
16H REFERENCE
BIAS AND ERASE FREQ. GENERATOR
125 kHz AUDIO BIAS
79 kHz ERASE FREQUENCY
PLAYBACK AMPLIFIER/ EQUALIZER
AUDIO MONITOR DRIVER
METER RECTIFIER AND DRIVER
AUDIO 1 LINE DRIVER
AUDIO 1
TO MONITOR SPEAKER/ HEAD-PHONE JACK
METER DRIVE
TO VU METER
AUDIO 1 LINE OUT
TO AUDIO CONNECTOR PANEL
BIDIRECTIONAL AUDIO 1 AND AUDIO 2 CROSSTALK CANCELLATION
CONTROL PANEL
PLAYBACK LEVEL CONTROL
FROM SERVO PWA
CONTROL TRACK 30 Hz SMPTE OR 25 Hz EBU
EBU PULSE FORMER/ BIAS RAMP GENERATOR
CONTROL TRACK RECORD PUSH PULL DRIVERS
RECORD/ PLAY RELAY
CONTROL TRACK RECORD/ PLAY HEAD
CONTROL TRACK PLAYBACK AMPLIFIER/ EQUALIZER
OUTPUT AMPLIFIER
EBU CROSSTALK CANCELLATION FROM AUDIO CHANNEL 3
CONTROL TRACK PLAY
TO SERVO PWA
AUDIO PWA

Figure 2-13. Audio System Simplified Block Diagram

As shown in Figure 2-13, audio inputs to be recorded are routed from the I/O connector panel to the Audio PWA. The signal is amplified by a front-panel-controlled amplifier and then applied to a record driver/equalizer circuit which boosts the high-frequency components. For the SMPTE standard only, frequencies below 50 Hz are also boosted. The equalized signal is fed through a bias filter and combined with a ramped 125-kHz bias signal before being routed to the audio record/play head stack assembly. For monitoring purposes, the record signal is also routed to the VU meter, audio monitor circuitry, and line output connector.

Transformer action within the audio head stack assembly causes bidirectional crosstalk between audio channels 1 and 2. To remedy the crosstalk that occurs when one channel is recording while another channel is playing back, audio from the channel in record is inserted 180° out of phase into the channel playing back to provide crosstalk cancellation.

In play mode, audio from the record/play head assembly is routed to the Audio PWA. The signal is preamplified and fed to a playback equalizer. Equalizer gain decreases with increasing frequencies to provide a flat playback response. The SMPTE standard Audio PWA also rolls off frequencies below 50 Hz to compensate for the boost provided in record mode. The equalized signal is amplified by a front-panel-controlled amplifier and then fed to the output line driver amplifiers which feed the line output connector. For monitoring purposes, the playback signal is also routed to the VU meter and audio monitoring circuitry.

The audio mixer mixes audio channels in any combination for application to the internal monitor speaker (or connector for an external headset). Signals routed to the monitor correspond to the VTR mode of operation (i.e., tape or E-E).

Audio bias and erase circuitry accepts a 16X horizontal (16H) reference frequency from the AST Servo PWA and provides 79-kHz bias for the recording of the control track signal, and erasure frequency for the full-width video erase head, control track erase head, and audio erase heads. The circuitry also provides 125-kHz bias for audio recording. Erase and bias frequencies are ramped on and off to prevent recording any pops or clicks.

SMPTE control track recording consists of saturated square waves that alternate in polarity at a field rate with an extra pair of transitions added on alternate frames to identify the color frame. The EBU control track recording consists of a series of alternate polarity pulses with an extra pulse provided to identify the PAL eight-field sequence.

Crosstalk cancellation circuitry is used in insert edit mode because of the close proximity of the audio channel 3 head winding to the control track head winding, and the low-level EBU control track signal level on tape (channel 3 audio in record mode while playing back the control track). Channel 3 audio is added 180° out of phase to the playback control track signal to provide cancellation.

Audio system theory of operation is given in Section 4, Part II of this manual. That section also includes detailed audio signal-system performance verification and alignment procedures.

2-28 Servo System

The servo system is made up of the Servo PWA, AST Servo PWA, and AST Driver PWA. The tension arm assembly, the scanner, and the capstan assembly are also included in the servo system. A simplified block diagram of the servo system is included in Figure 2-10.

The Servo PWA includes an NMOS, 8-bit microprocessor which interprets commands from the primary microprocessor, controls the servo system accordingly, and returns servo status information back to the primary microprocessor. The servo microprocessor kernel is composed of the microprocessor, 16K bytes of read-only memory (ROM), and 1024 bytes of RAM storage.

The AST Servo PWA contains reference oscillators, counters, dividers, and reference phases essential to VTR operation. The AST Servo PWA is locked to information from the Reference PWA. The servo system includes scanner servo, capstan servo, reel motor servos, and AST servo, as well as playback sync processing, phase-lock oscillators, and all responsibility for time-base corrector interfacing. The servo system is a low-power system, providing low-level signals out which are then amplified by the AST Driver PWA and four motor drive amplifiers (MDAs).

Whereas the primary microprocessor communicates with all the other PWAs on the system bus, the servo microprocessor is slaved to and communicates only with the primary microprocessor. The primary microprocessor issues commands such as "start the scanner" to the servo microprocessor. The Servo PWA makes decisions as to what conditions must be satisfied in order to accept and execute any particular command. The servo microprocessor then decides what the frequencies are, what the speed is, what the phase is, etc., and whether the tach is actually turning. The servo microprocessor then reports the status of the servo system to the primary microprocessor. Status bits indicate that the scanner is running and coming up to speed, that the scanner is running at lock speed, or that the scanner is not running and why.

Theory of operation information and detailed servo system alignment procedures are given in Section 5, Part II of this manual.

2-29 Control System

The control system is composed of the Control PWA and the control panel assembly which includes Primary and Secondary Control Panel PWAs. Parallel and/or serial remote control capabilities are included at the user's option. A simplified block diagram of the Control PWA is shown in Figure 2-14.

The primary microprocessor is located on the Control PWA. The kernel consists of the 8-bit, NMOS microprocessor, 32K bytes of read-only memory, and 1024 bytes of random access memory (RAM). PROM storage holds instruction sets involved in the initialization, background, and foreground routines, and RAM storage is used to hold variables such as tape time and edit entrance and exit points.

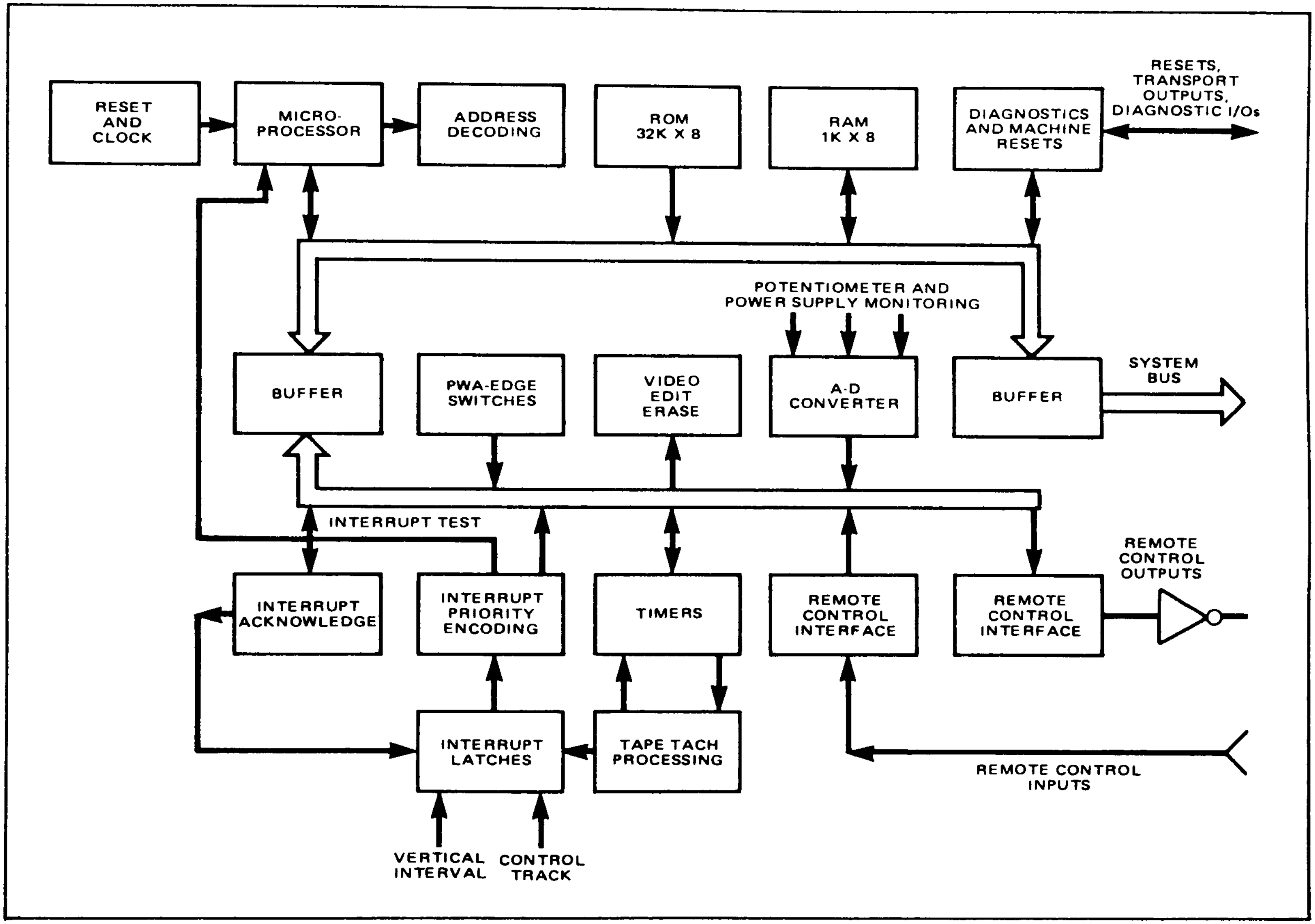


Figure 2-14. Control PWA Simplified Block Diagram

When power is applied to the VPR-80, the primary microprocessor immediately performs the initialization routine. The initialization routine first tests the CPU kernel. It then tests the system bus and each of the subsystems of the VPR-80. If no faults are detected, it then completes the initialization routine as diagrammed in Figure 2-15. The VTR then enters stop mode, standby condition. The microprocessor is in a housekeeping status which will be terminated when the first mode change command is initiated by the VTR operator at the control panel. The next command entered at the control panel could be depression of the READY switch. This command starts the scanner motor. When the scanner motor reaches lock speed, the ready condition of stop mode is achieved. If, for example, the next command is depression of the PLAY switch, the microprocessor begins the background routine in which the subset of instructions which implements the transition to play mode is employed. If play mode and edit commands are combined, the background routine can be interrupted by any of the eight foreground routines charted in Table 2-3. Each of the foreground routines first acknowledges its interrupt and then executes the routine. When finished, it returns to the interrupt service routine: if there are no more interrupts, it then returns to the background routine (Figure 2-16).

The control system is discussed in detail in Section 6, Part II of this manual.

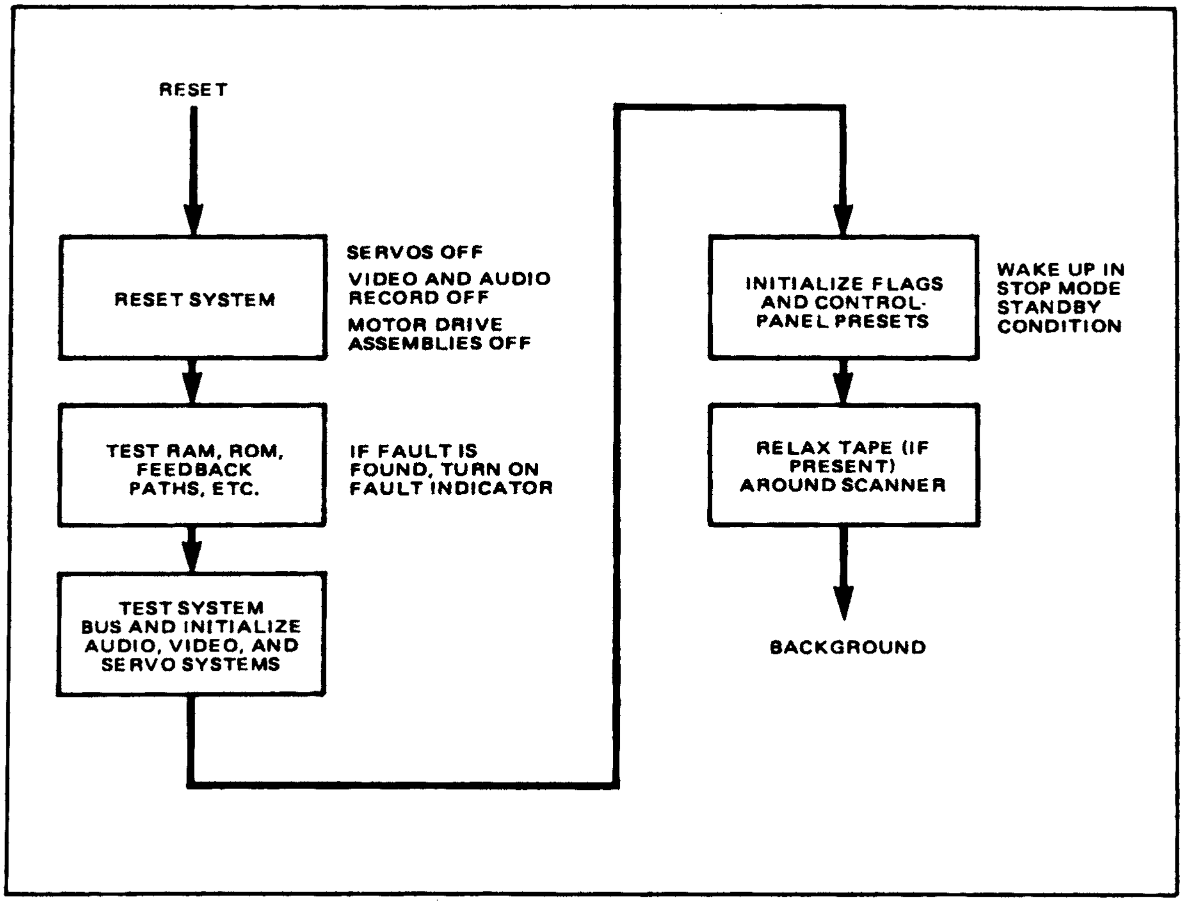
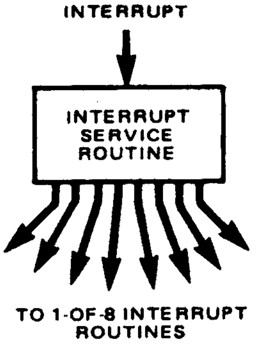

RESET
RESET SYSTEM
SERVOS OFF
VIDEO AND AUDIO RECORD OFF
MOTOR DRIVE ASSEMBLIES OFF
TEST RAM, ROM, FEEDBACK PATHS, ETC.
IF FAULT IS FOUND, TURN ON FAULT INDICATOR
TEST SYSTEM BUS AND INITIALIZE AUDIO, VIDEO, AND SERVO SYSTEMS
INITIALIZE FLAGS AND CONTROL-PANEL PRESETS
WAKE UP IN STOP MODE STANDBY CONDITION
RELAX TAPE (IF PRESENT) AROUND SCANNER
BACKGROUND

Figure 2-15. Control System—Initialization Routine

Table 2-3. Control System—Foreground Routines (Interrupts)



Priority	Interrupt	Routine
0	Vertical	Sample inputs, editing decisions, read elapsed time meter, output data.
1	Tach Frame	Increments or decrements tape time binary counters.
2	Delta D	A change in direction; adjusts count direction in tape timer.
3	Control Track	Adjusts count in tape tach timer for control track phasing.
4	Video Edit	Provides fine timing for video record and erase switching.
5	Audio Edit Erase	Provides fine timing for audio edit erase switching.
6	Audio Edit Record Off	Provides fine timing for switching audio edit record off at the exit point.
7	Audio Edit Record On	Provides fine timing for switching audio edit record on at the entrance point.

2-30 Transport System

The transport system is made up of the Capstan/Scanner Motor Drive Amplifier (MDA), the Reel MDA, and the supply and takeup reel motor and turntable assemblies.

The capstan motor and scanner motor are powered by the Capstan/Scanner MDA PWA. This PWA contains two separate servo-controlled amplifiers used to drive the motors. Supply and takeup reel motors are powered by the Reel MDA PWA. This PWA also contains two separate servo-controlled switching amplifiers, each of which is capable of driving a reel motor in either direction at variable speed.

Figure 2-17 is a simplified block diagram of the Capstan MDA. The Capstan MDA is a position-servo-controlled analog amplifier under control of a dc error signal

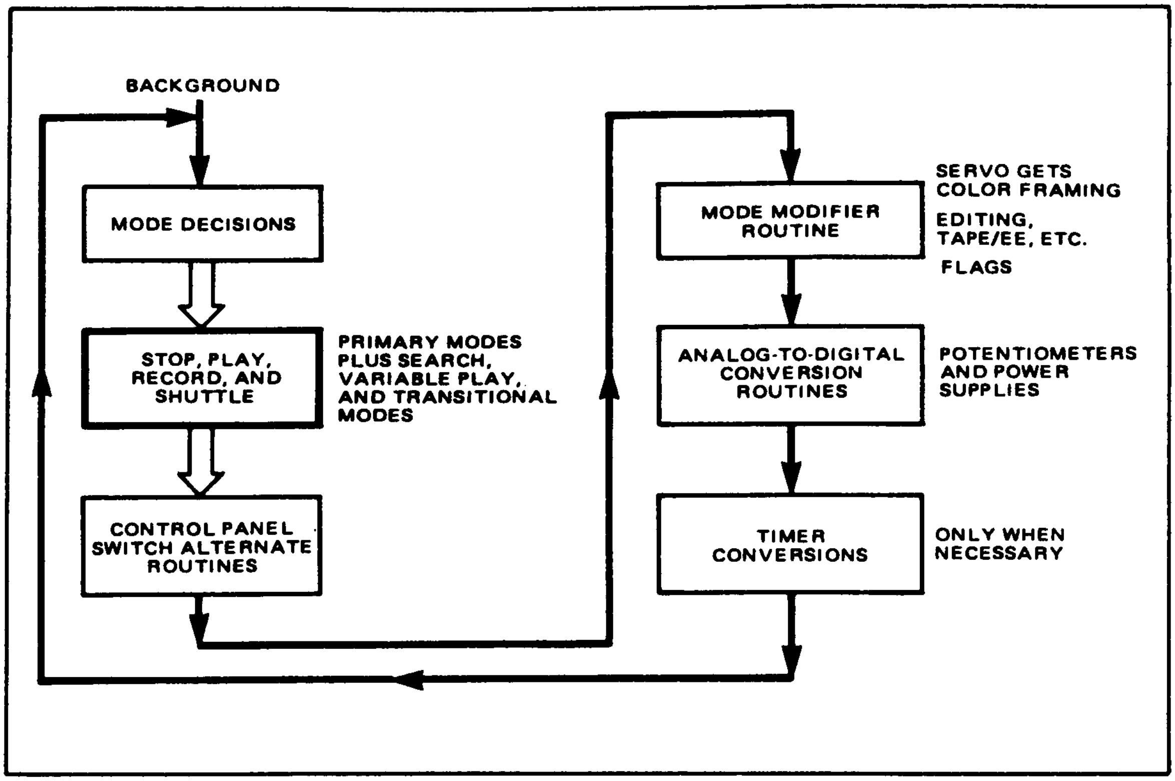

BACKGROUND
MODE DECISIONS
STOP, PLAY, RECORD, AND SHUTTLE
PRIMARY MODES PLUS SEARCH, VARIABLE PLAY, AND TRANSITIONAL MODES
CONTROL PANEL SWITCH ALTERNATE ROUTINES
MODE MODIFIER ROUTINE
SERVO GETS COLOR FRAMING
EDITING, TAPE/EE, ETC.
FLAGS
ANALOG-TO-DIGITAL CONVERSION ROUTINES
POTENTIOMETERS AND POWER SUPPLIES
TIMER CONVERSIONS
ONLY WHEN NECESSARY

Figure 2-16. Control System—Background Routine

supplied by the capstan servo. Although the amplifier is capable of driving the dc capstan motor in either direction, the motor drives tape forward only at speeds from 0 to 1.5X normal play speed. The motor is quickly stopped when the capstan servo momentarily generates an error signal. Error signal polarity causes the MDA to provide reverse drive current to the capstan motor.

Figure 2-18 is a simplified block diagram of the Scanner MDA, which is a servo-controlled analog power amplifier that is under control of a dc position-error signal developed on the Servo PWA. This error signal is a result of comparing the scanner tach signal with the reference vertical signal. The MDA drives the scanner dc motor in one direction only at either 3600 rpm (60-Hz line standard) or 3000 rpm (50-Hz line standard). Dynamic braking is used to stop the motor.

Figure 2-19 is a simplified block diagram of the Reel MDA. The Reel MDA contains two servo-controlled switching amplifiers, each under control of a dc differential error signal supplied from the Servo PWA. The dc error signal is combined with a 46.5-kHz triangular waveform to produce a pulse-width-modulated (PWM) waveform. Symmetry of the waveform changes as a function of the dc error signals. The PWM signal is applied to current switching FET transistors to control motor direction, torque, and to affect dynamic braking.

Detailed descriptions of the Scanner, Capstan, and Reel MDAs and the Reel MDA alignment procedure are given in Section 7, Part II of this manual.

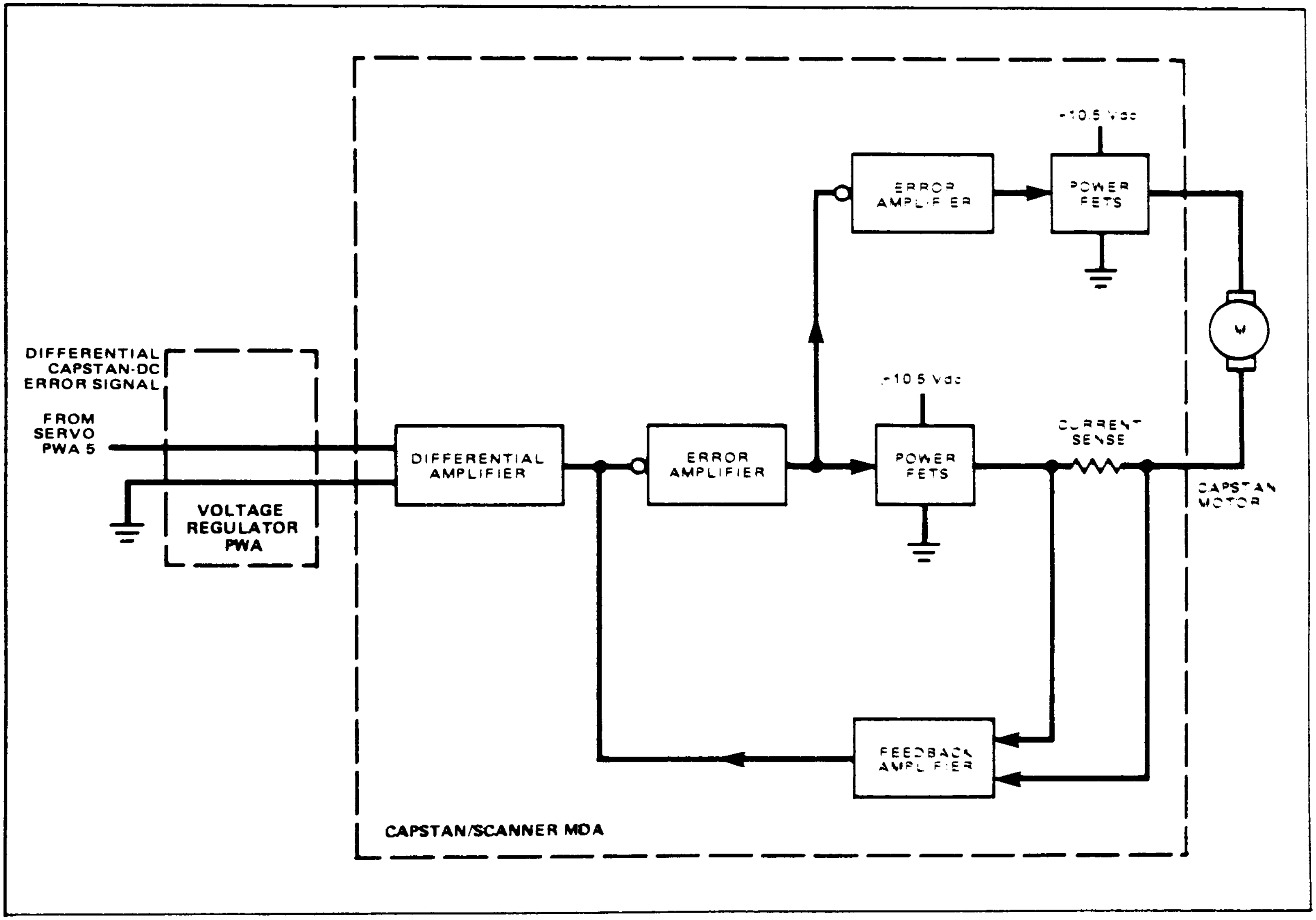


Figure 2-17. Capstan MDA Simplified Block Diagram

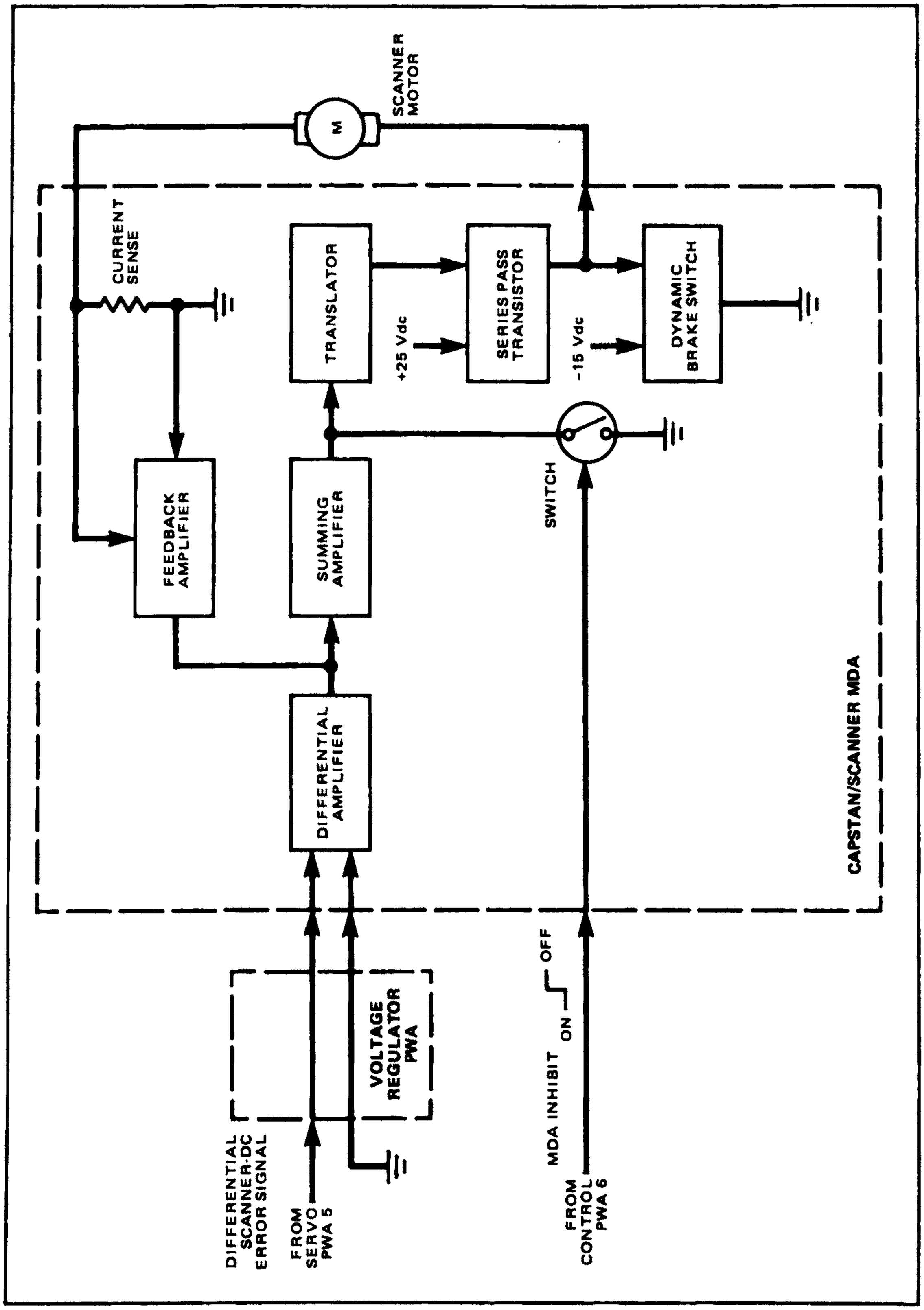


Figure 2-18. Scanner MDA Simplified Block Diagram

2-31 Accessories

There are three PWAs available as optional accessories for the VPR-80:

Parallel Remote PWA
Serial Remote PWA
Time-Code System PWA

The Serial Remote PWA and Time-Code System PWA are installed piggyback in the auxiliary Card Cage slot (slot 5), and the Parallel Remote PWA is installed piggyback on the Control PWA.

2-32 Parallel Remote PWA

The Parallel Remote PWA is provided in kit form (Ampex P/N 1450019) for installation piggyback on the Control PWA. Parts provided in the kit are listed in Table 2-4. The Parallel Remote PWA provides the interface between an external, remotely located control panel and the Control PWA in the VPR-80. Parallel control inputs and parallel output lines to the remote indicators are routed through the PARALLEL REMOTE connector (J1) at the rear of the VPR-80 cabinet. Parallel I/O lines between the Parallel Remote and Control PWAs are contained in a PWA-edge-to-PWA-edge connector which acts as a jumper plug between the two adjacent PWAs.

Table 2-4. Parallel Remote Kit

Ampex P/N	Description	Quantity
1450-466	PWA, Parallel Remote	1
1450783-AA	Cable Assy, 0.9 inch, 50 Position	1
1450783-AB	Cable Assy, 20 inch, 50 Position	1
1451112	Label, Parallel Remote	1
1809587	Instructions, Installation	1
070-452	Fuse, Plug-in, Fast Blow, 0.5A 125V	2
070-453	Fuse, Plug-in, Fast Blow, 2A 125V	1
166-227	Connector Part, Contact, Pin, 18-16 AWG	75
166-299	Connector Part, Body, Plug, Rect., 75 Position	1
473-895	Screw, Decorative, #6-32 x 0.375 Lg.	7

2-33 Serial Remote PWA

The Serial Remote PWA is provided in kit form (Ampex P/N 1450023) and enables the VPR-80 to be incorporated in a serial communications network such as the

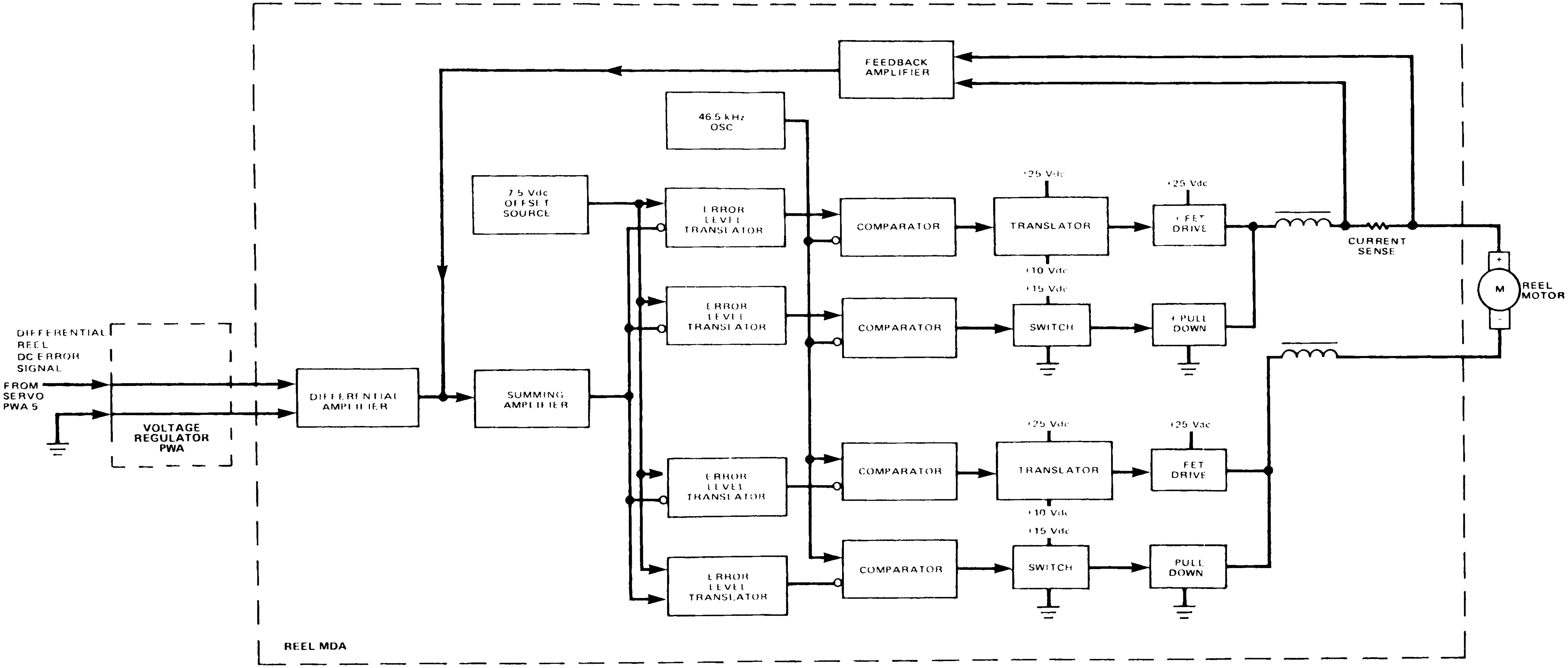


Figure 2-19.
Reel MDA Simplified Block Diagram

Ampex computerized Editing (ACE) system. With serial communication capability the VPR-80 can be controlled by any device which conforms to the electrical and mechanical characteristics described in "Proposed American Standard PH22.207M: Electrical and Mechanical characteristics for Digital Control Interface." In the discussion on the Serial Remote PWA such a device is referred to as the Bus Controller. Protocol is specified in "Proposed SMPTE Recommended Practice RP 113: Supervisory Protocol for Digital Control Interface."

2-34 Time-Code System PWA

The Time-Code System (TCS) PWA generates longitudinal time code in accordance with either of the following television industry standards:

> SMPTE Proposed Recommended Practice RP 93-1980, "Requirements for Recording American National Standard Time and Control Code on 1-in. Types B and C Helical Scan Video Tape Recorders"
>
> EBU Technical Bulletin 3097-E, "EBU time-and-control codes for television tape recordings (625-line television systems)"

Time code (TC) is a digital signal containing 80 bits per television frame, and is recorded in bi-phase mark (Manchester I) code format on the audio channel 3 longitudinal track. The code uniquely defines, or addresses, every frame on the tape in hours, minutes, seconds, and frames. The signal originated from a time-code generator (TCG) and can be distributed to other VTRs and editing devices.

PART I

SECTION 3

SYSTEM OPERATION

3-1 GENERAL

This section provides descriptions of all controls and indicators and a general summary of modes of operation. Detailed operating instructions are spelled out in the *VPR 80 Installation and Operation* manual.

3-2 CONTROLS AND INDICATORS

Controls and indicators used for record and playback operation and during editing procedures are located on the primary control panel. Controls and indicators used less frequently, such as during special operating circumstances or during adjustment procedures, are located on the secondary control panel directly above the primary controls. Controls and indicators used for maintenance purposes only are located on top edges of the Audio PWA and PWAs in the card cage. Access to these controls and indicators is gained by opening the top access door of the VPR-80 cabinet.

3-3 Primary Control Panel

Operating controls and indicators, located on the primary control panel, are described in Tables 3-1, 3-2, and 3-3.

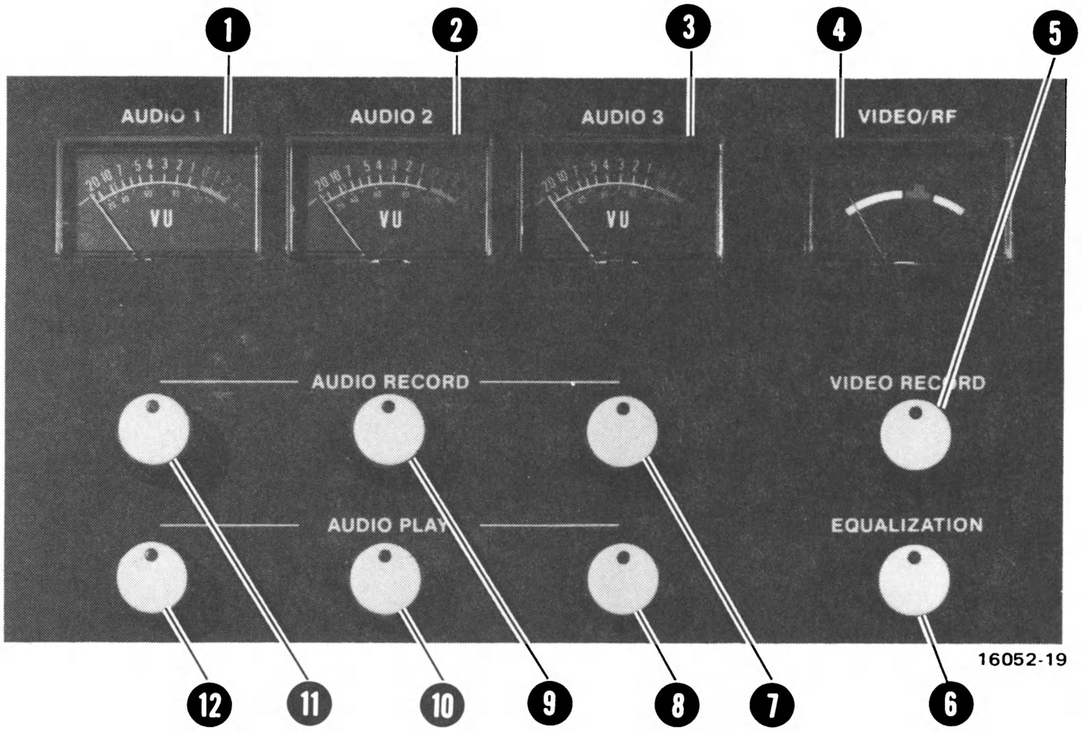
3-4 Secondary Control Panel

Secondary operating controls and indicators are described in Tables 3-4 and 3-5.

3-5 PWA Edge Controls and Indicators

PWA edge-mounted controls and indicators in the card cage are described in Table 3-6. PWA edge-mounted controls on the Audio PWA are explained in Section 4, Part II of this manual.

Table 3-1. Primary Control Panel (Input/Output Level Controls and Metering)



Index No.	Description	Function
1	AUDIO 1 meter	Indicates audio channel 1 signal amplitude. Zero VU is normal operating level (+8 dBm, balanced output).
2	AUDIO 2 meter	Indicates audio channel 2 signal amplitude.
3	AUDIO 3 meter	Indicates audio channel 3 signal amplitude.
4	VIDEO/RF meter	When in play or variable play mode, displays rf level. In record mode, indicates demodulator output video level which in EE corresponds to video record level. In other modes, indicates off-tape rf if EE indicator is off, or demodulator output video level which corresponds to video record level if EE indicator is on.
5	VIDEO RECORD control	Provides adjustment of video input from zero (full ccw) to twice input amplitude (full cw). Center (detent) position is used for unity gain setting when input level is 1.0 Vp-p..

(Continued next page)

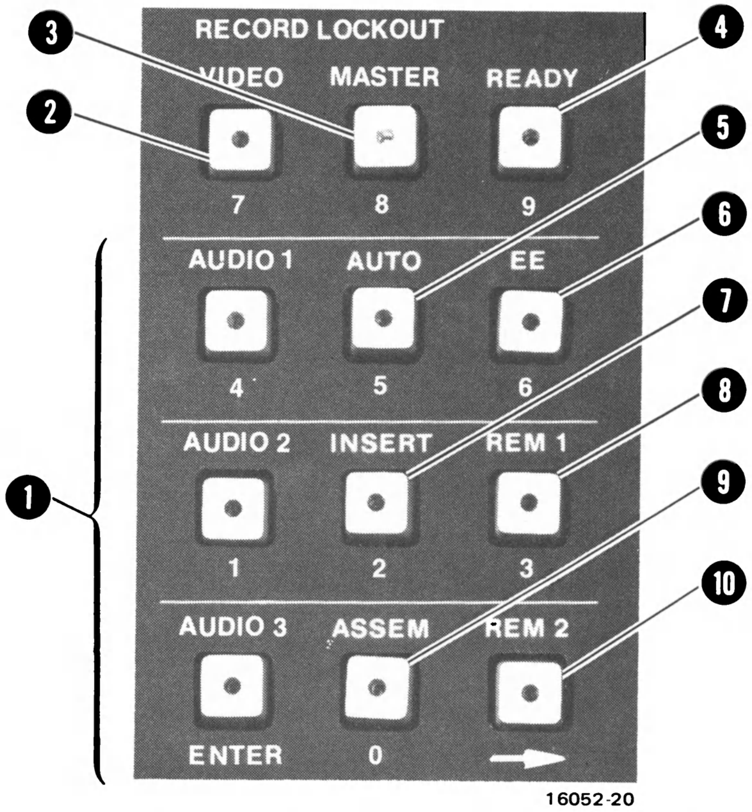
Table 3-1. Primary Control Panel (Input/Output Level Controls and Metering) (Continued)

Index No.	Description	Function
6	EQUALIZATION control	When CHROMA EQUAL/MANUAL indicator (on secondary control panel) is off, playback frequency response is automatically adjusted in order to keep constant chroma amplitude. Detent position is unity, and adjustment range of this control is limited to a very narrow band on either side of the detent. When CHROMA EQUAL/MANUAL indicator is on, this control provides manual equalization adjustment to video frequency response in playback.
7	AUDIO (3) RECORD control	Provides adjustment of audio channel 3 record level. Center (detent) position is used for unity gain setting.
8	AUDIO (3) PLAY control	Provides adjustment of audio channel 3 playback level. Center (detent) position is used for unity gain setting.
9	AUDIO (2) RECORD control	Provides adjustment of audio channel 2 record level. Center (detent) position is used for unity gain setting.
10	AUDIO (2) PLAY control	Provides adjustment of audio channel 2 playback level. Center (detent) position is used for unity gain setting.
11	AUDIO (1) RECORD control	Provides adjustment of audio channel 1 record level. Center (detent) position is used for unity gain setting.
12	AUDIO (1) PLAY control	Provides adjustment of audio channel 1 playback level. Center (detent) position is used for unity gain setting.

Table 3-2. Primary Control Panel (Record Lockout and Mode Enable Controls)

Note

All switches listed in Table 3-2 are alternate action.



Index No.	Description	Function
1	AUDIO 1-3 RECORD LOCKOUT switch/indicators (3)	Enabled when in insert edit mode (INSERT indicator lighted). When individual switch is pressed and indicator is lighted, recording of that audio channel is inhibited. Record capability is interlocked through MASTER RECORD LOCKOUT switch.

Note

When in insert edit mode, individual channels can be enabled or locked out, but when in assemble edit or normal record mode, all channels are either enabled or locked out.

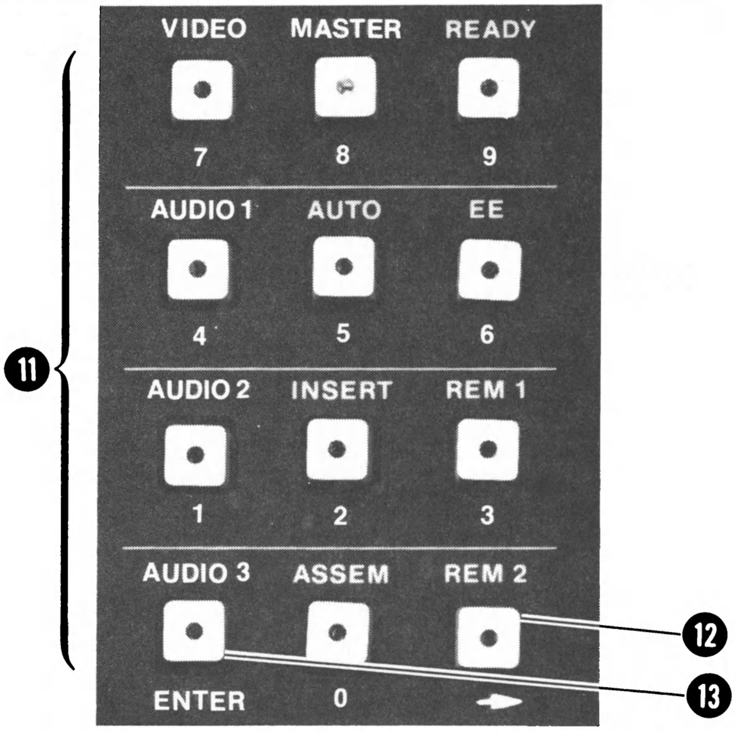
(Continued next page)

Table 3-2. Primary Control Panel (Record Lockout and Mode Enable Controls) (Continued)

Index No.	Description	Function
2	VIDEO RECORD LOCKOUT switch/indicator	Video recording inhibited when indicator is lighted. Record capability is interlocked through MASTER RECORD LOCKOUT switch. (Refer to note above.)
3	MASTER RECORD LOCKOUT switch/indicator	This switch is enabled when RECORD switch is first pressed and held down. When indicator is lighted, all record functions are inhibited.
4	READY switch/indicator	Controls VTR condition when in stop mode. When indicator is not lighted, VTR is in standby condition (all motors off). Pressing READY commands VTR to come up to ready condition (scanner motor starts and comes up to lock speed). VTR is always in standbuy condition when power is initially applied.
5	AUTO switch/indicator	When this switch is pressed and indicator is lighted, auto edit mode is enabled (see paragraphs 3-23 through 3-27).
6	EE switch/indicator	Active in stop and shuttle modes. When indicator is lighted, input signals are routed through record and play electronics to the outputs but are not actually recorded on tape. Tape is not under tension in stop mode. When indicator is not lighted, tape is tensioned, and off-tape audio and video appear at outputs.
7	INSERT switch/indicator	When indicator is lighted, insert editing is enabled (video and audio channels are edited separately or in any combination, control track is not recorded).
8	REM 1 switch/indicator	Enables parallel, serial, or simple remote control capability. When REM 1 indicator is not lighted, control of VTR is exercised at local control panel assembly. Pressing REM 1 transfers control of VTR to selected remote control accessory; however, STOP mode switch on primary control panel remains enabled. Selection of remote control input source is made by remote 1 setup procedure.
9	ASSEM switch/indicator	When indicator is lighted, assemble editing is enabled (video and all audio channels are edited simultaneously and control track is recorded).
10	REM 2 switch/indicator	Enables or inhibits auto edit (multi-VTR) mode. When two or more VTRs are interconnected via the multi-VTR cable, depressing REM 2 on source VTR enables record VTR to remotely control cue and play modes of source VTR(s)

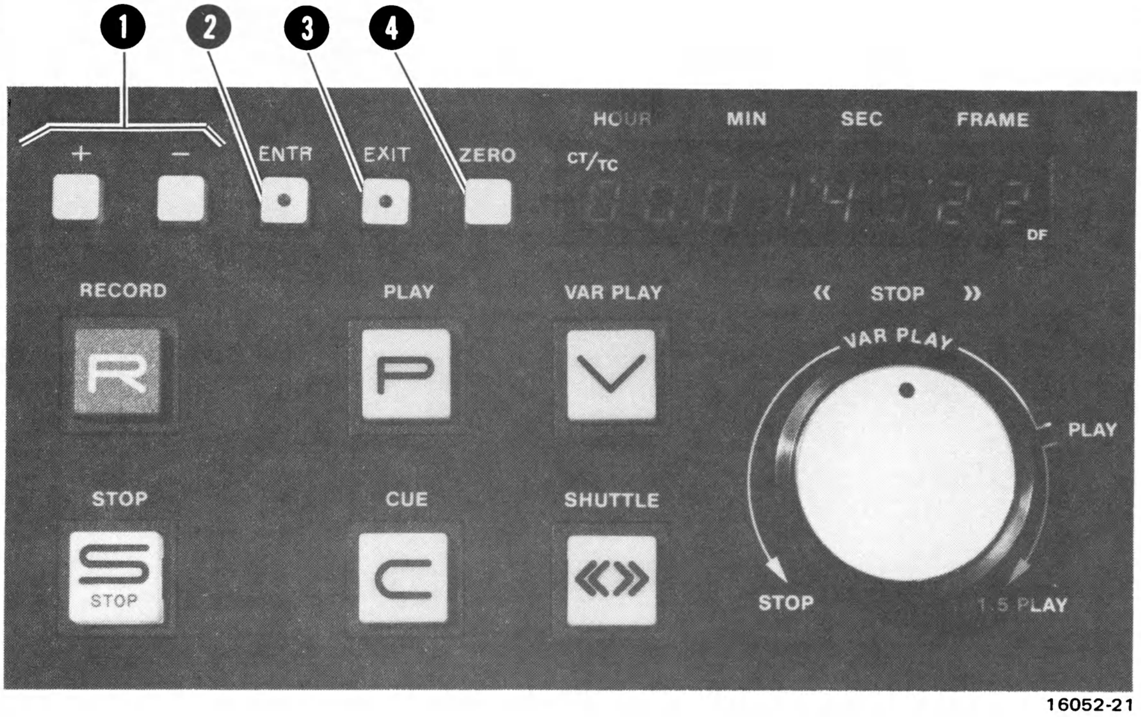
(Continued next page)

Table 3-2. Primary Control Panel (Record Lockout and Mode Enable Controls) (Continued)



<table>
<tr><th>Index No.</th><th>Description</th><th>Function</th></tr>
<tr><td colspan="3">**Note**
Keypad functions (placarded in yellow or green) are enabled only when either SET UP, ENTR, or EXIT indicator (see Tables 3-3 and 3-5) is lighted.</td></tr>
<tr><td>11</td><td>Numeric 0-9 switches (10)</td><td>Used to enter setup condition identifiers (i.e., video head optimization) edit entrance and exit points, and edit point trim values. Entries are shown on numeric display. Numeric entry is not recognized by VPR-80 until ENTER is pressed. There is a 5-second timeout on all keypad entries. If ENTER (below) is not pressed within 5 seconds after last entry, entire keypad entry and display are erased.</td></tr>
<tr><td>12</td><td>Backspace switch</td><td>Each depression of this switch shifts to the right the displayed number last entered with keypad numeric switches. Used to correct errors in keypad entry.</td></tr>
<tr><td>13</td><td>ENTER switch</td><td>Loads and validates keypad entries made with numeric switches. VPR-80 does not recognize keypad entry until ENTER is pressed. This switch must be pressed within 5 seconds after last entry. Otherwise, entire keypad entry and display are erased.</td></tr>
</table>

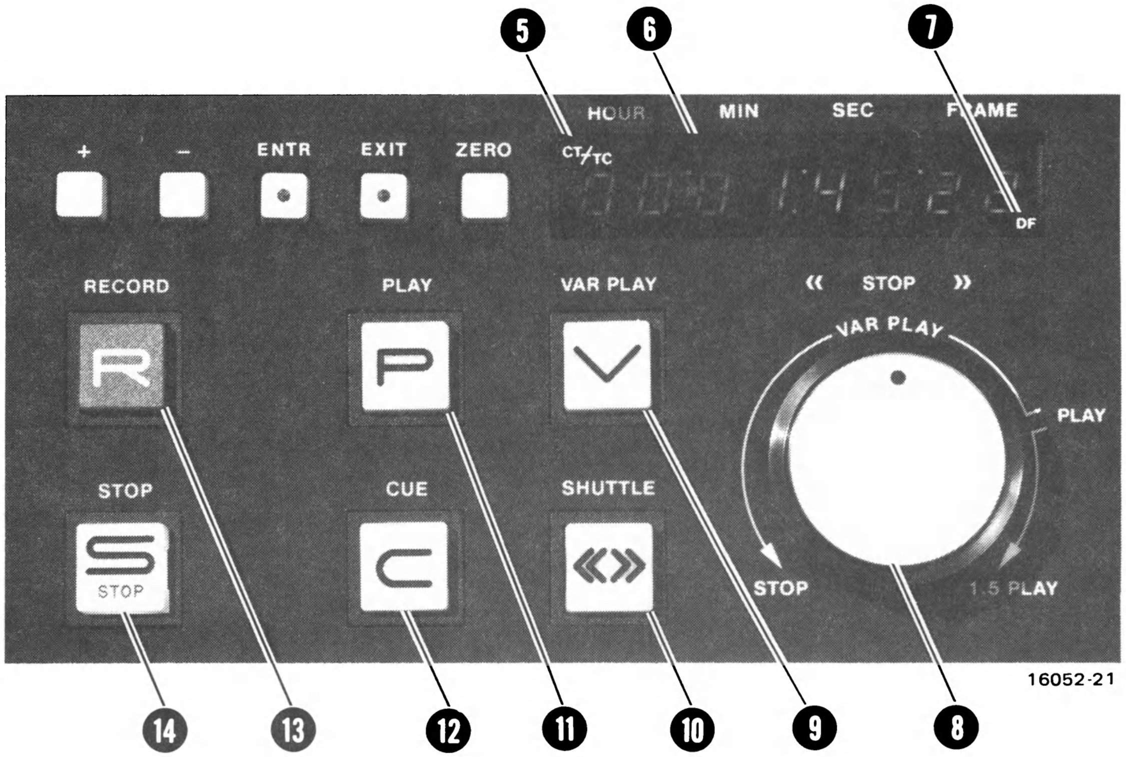
Table 3-3. Primary Control Panel (Transport Mode Controls)



Index No.	Description	Function
1	± switches (2)	Enabled when ENTR or EXIT indicators are lighted. Pressing (+) or (−) switch determines whether frame trim count entered with keypad numeric switches will be added to or subtracted from edit entrance or exit point. Frame trim count is shown on numeric display. Entrance or exit points are not adjusted by frame trim count until ENTER switch (refer to Table 3-2) is pressed. When both (+) and (−) switches are pressed at the same time, duration of edit interval is displayed.
2	ENTR switch/indicator	This is an alternate action switch. When indicator is lighted, keypad is enabled, and edit entrance point is displayed. Edit entrance point can then be set, changed, or trimmed.
3	EXIT switch/ indicator	This is an alternate action switch. When indicator is lighted keypad is enabled, and edit exit point is displayed. Edit exit point can then be set, changed, or trimmed.
4	ZERO switch	Zeros tape timer.

(Continued next page)

Table 3-3. Primary Control Panel (Transport Mode Controls) (Continued)



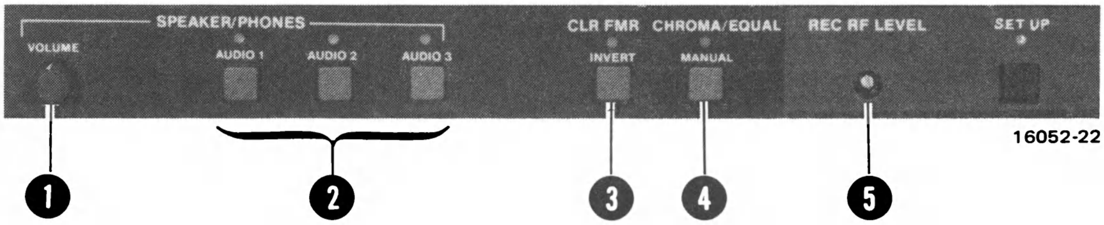
Index No.	Description	Function
5	CT//TC indicator	This indicator flashes if control track not present. When time code is displayed, this indicator flashes if time code is not valid.
6	Numeric display	Displays current tape time in hours, minutes, seconds, and frames, time-code time, or time-code user information, as determined by display input selection setup. Also displays fault and nonstandard condition indications when commanded by FAULT and SYSTEM switches on secondary control panel (see Table 3-5). Also displays setup codes, duration of edit interval when (+) and (−) switches are both pressed, keypad entries, and contents of entrance or exit register.
7	DF indicator	When lighted, indicates that drop frame time is displayed. If output of time code is displayed, indicates that time code off tape is drop frame. If output of tape timer is displayed, indicates that DROP FRAME switch on Control PWA is in DF position. Not applicable to PAL/SECAM systems.

(Continued next page)

Table 3-3. Primary Control Panel (Transport Mode Controls) (Continued)

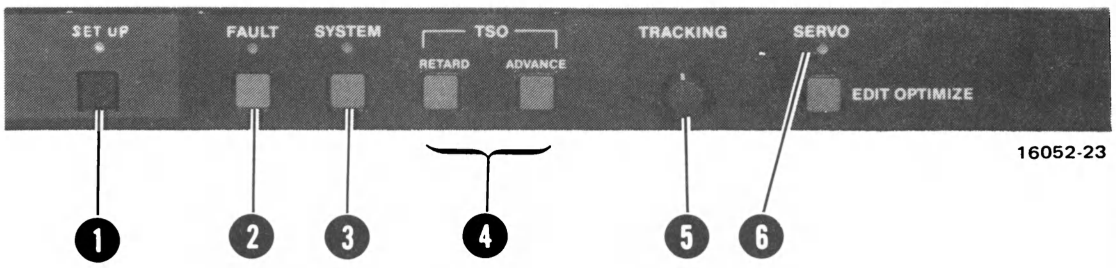
Index No.	Description	Function
8	Tape speed control	When activated by SHUTTLE switch, provides variable speed shuttle up to 300 in/s (762 cm/s) forward or reverse. When activated by VAR PLAY switch, provides variable speed play from stop to 1.5X play speed forward. When knob is rotated to normal play speed position, indicated by PLAY on the scale, PLAY switch/indicator lights.
9	VAR PLAY switch/indicator	When pressed, indicator lights, and tape speed control is enabled to provide variable speed playback. When switch is pressed twice in succession, tape motion stops and indicator flashes, indicating pause mode. Pressing switch again restarts tape motion at speed commanded by tape speed control.
10	SHUTTLE switch/indicator	When pressed, indicator lights, and tape speed control is enabled to provide shuttling of tape in either direction. Tape will not shuttle off end of tape in either direction. Pressing this switch twice in succession commands transport to unthread (see paragraph 3-19). Indicator flashes during unthreading.
11	PLAY switch/indicator	Initiates playback mode of operation. Lights when active. Indicator will also light during playback portions of edit record operations. Also lights when tape is moving at normal play speed when in variable play mode. If in auto edit mode (AUTO indicator is lighted), pressing this switch twice in succession initiates review mode. PLAY indicator flashes during review operation (see paragraph 3-26).
12	CUE switch/indicator	When switch is pressed, cues tape to entrance point with preroll. If EXIT is pressed first (EXIT indicator lighted), pressing CUE cues tape to exit point with preroll. If CUE is pressed twice in succession, tape is cued without preroll and CUE indicator flashes.
13	RECORD switch/indicator	When pressed simultaneously with PLAY, initiates record mode of operation. Lighted when active. PLAY indicator remains on until recording starts.
14	STOP switch/indicator	Pressing this switch initiates stop mode of operation which overrides all other mode commands. Indicator is lighted when active. When in remote operation, pressing this switch will terminate remote control mode.
Not shown	PWR switch	Primary power switch is located above right-hand end of the secondary control panel. It is a slide switch: pushed in for power on, pulled out for power off.

Table 3-4. Secondary Control Panel (Left-Hand Side)



Index No.	Description	Function
1	SPEAKER/ PHONES VOLUME control	Controls speaker (or headphone) volume when monitoring audio channels.
2	AUDIO 1–3 switch/indicators (3)	Enables or inhibits monitoring of audio channels 1, 2, and 3. Indicator lighted for enabled channels(s). Any combination of audio channels can be monitored simultaneously.
3	CLR FMR/INVERT switch/indicator	INVERT switch is enabled when CLR FRAME switch on Control PWA is ON. See Table 3-6. INVERT switch selects color framer playback phase by enabling operator to choose odd or even frame referencing. When CLR FMR indicator is off, playback color frame matches color frame reference. When INVERT is pressed, indicator lights, indicating that playback color frame is inverted from the reference. IF CLR FRAME switch on Control PWA is OFF, pressing INVERT causes CLR FMR indicator to flash once momentarily.
4	CHROMA EQUAL/MANUAL switch/indicator	When switch is pressed and indicator is lighted, EQUALIZATION control on primary control panel is enabled. When indicator is off, chroma burst is automatically adjusted, and EQUALIZATION control is limited to a very narrow range.
5	REC RF LEVEL (VHO) control	This screwdriver adjustment is used when in VHO setup mode. Provides control of rf level during record mode (video head optimization); monitored at RF LEVEL/VIDEO meter on primary control panel. Adjustment should not be altered unless in VHO setup mode.
Not shown	HOURS (Head Hour) meter	A digital counter which indicates cumulative number of hours that scanner has been on with tape tension. Meter is located above CLR FMR indicator. Counter steps every six minutes. Maximum indication is 99999.9 hours.

Table 3-5. Secondary Control Panel (Right-Hand Side)



Index No.	Description	Function
1	SET UP switch/indicator	Enabled only when in local stop mode. Switch enables operator to select special operating modes. When indicator is lighted, keypad is enabled. (Refer to Table 3-2).
2	FAULT switch/indicator	If self-test logic detects a fault in the system, FAULT indicator will blink momentarily or continuously, depending upon nature of the fault. Fault can be identified by pressing FAULT which causes a numerical indication of the fault to be displayed. A total of four fault indications can be held for display. See Table 4-9.
3	SYSTEM switch/indicator	SYSTEM indicator will light when a nonstandard condition exists in the VTR. SYSTEM indicator will blink momentarily or continuously, depending upon nature of the condition. Condition can be identified by pressing SYSTEM switch which causes a numerical indication to be displayed. A total of four nonstandard condition indications can be held for display. See Table 4-8.
4	TSO RETARD and ADVANCE switches	Tape speed override (momentary contact) switches enabled in play mode only. Depressing RETARD provides a 7% decrease in tape speed, and depressing ADVANCE provides a 7% increase.
5	TRACKING control	This control–enabled only in play mode and inhibited when either AST or editor is on–provides adjustment of capstan servo to align center of tape rf track with video head. Center detent is unity position in which tracking is preset to a reference vertical phase.
6	SERVO indicator	When lighted, indicates that a servo is unlocked (i.e., started, but not up to speed). Also lighted when in edit optimize mode.

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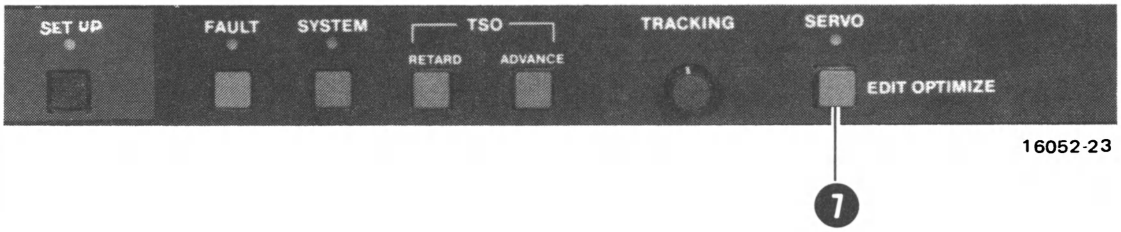
Table 3-5. Secondary Control Panel (Right-Hand Side) (Continued)



Index No.	Description	Function
7	EDIT OPTIMIZE switch	Enabled only when in edit play mode (PLAY and INSERT or ASSEM indicators lighted). When switch is pressed, SERVO indicator lights, indicating edit optimization is taking place. Edit optimization is needed only when performing interchange edits (on a tape recorded by a diffferent VTR). During edit optimization, VPR-80 automatically tracks to tape and rephases scanner tach to timing of video signal on tape. If VPR-80 is unable to rephase scanner tach to tape, SYSTEM indicator is lighted. Refer to index 3.

Table 3-6. Card Cage PWA Edge-Mounted Controls and Indicators

Index No.	Reference Designation	Control	Function
1	6R8		(This pot has no function.)
2	6DS1	BUS indicator (red)	When lighted, indicates bus communication fault.
3	6DS2	CPU indicator (green)	When blinking at 1-Hz rate, indicates that CPU activity is proceeding normally. If indicator is off or on steadily, indicates fault in CPU kernel.
4	6S1	SYSTEM RESET switch (momentary contact)	Asserts reset to CPU and resets control logic to initial condition.

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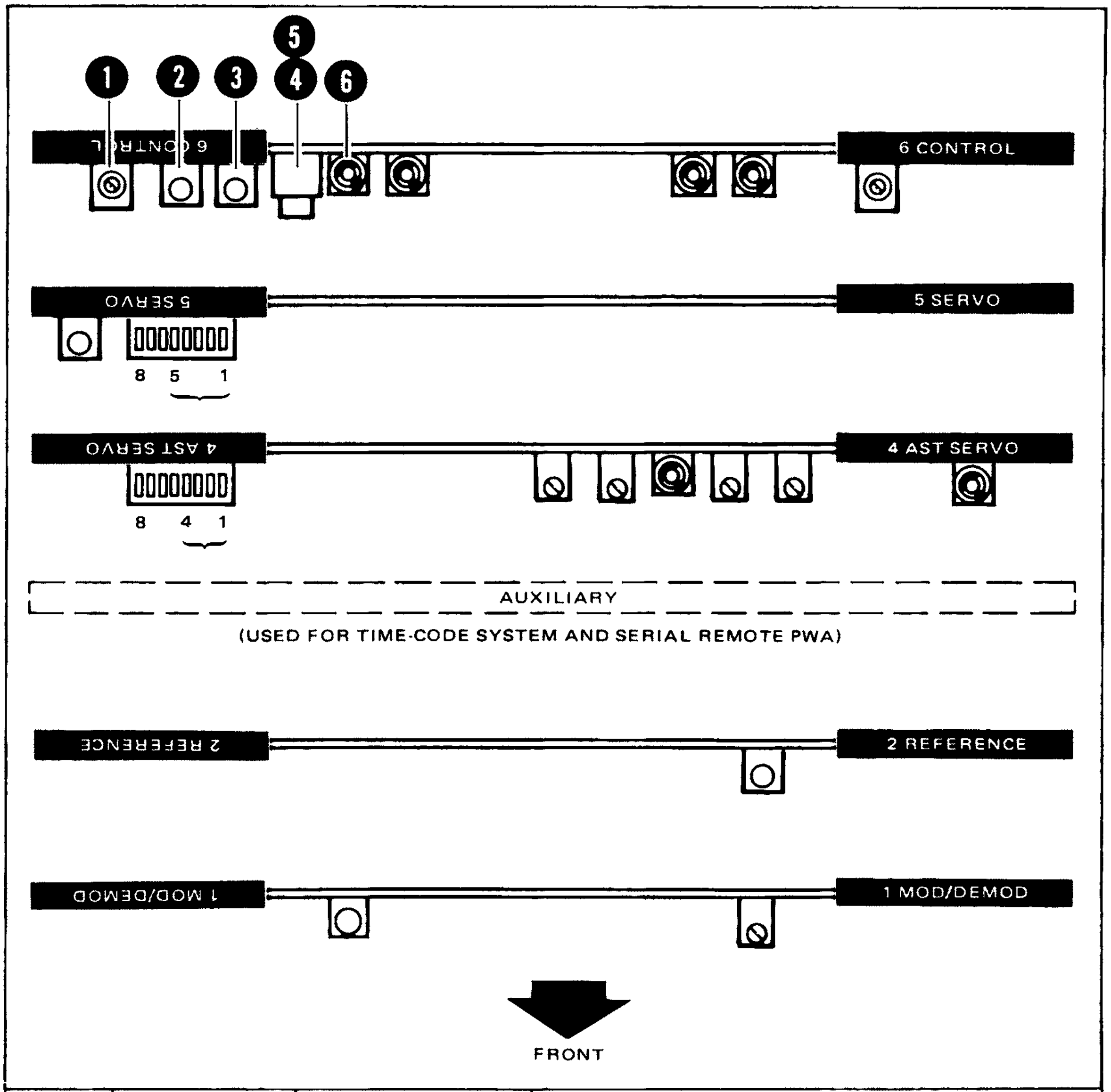
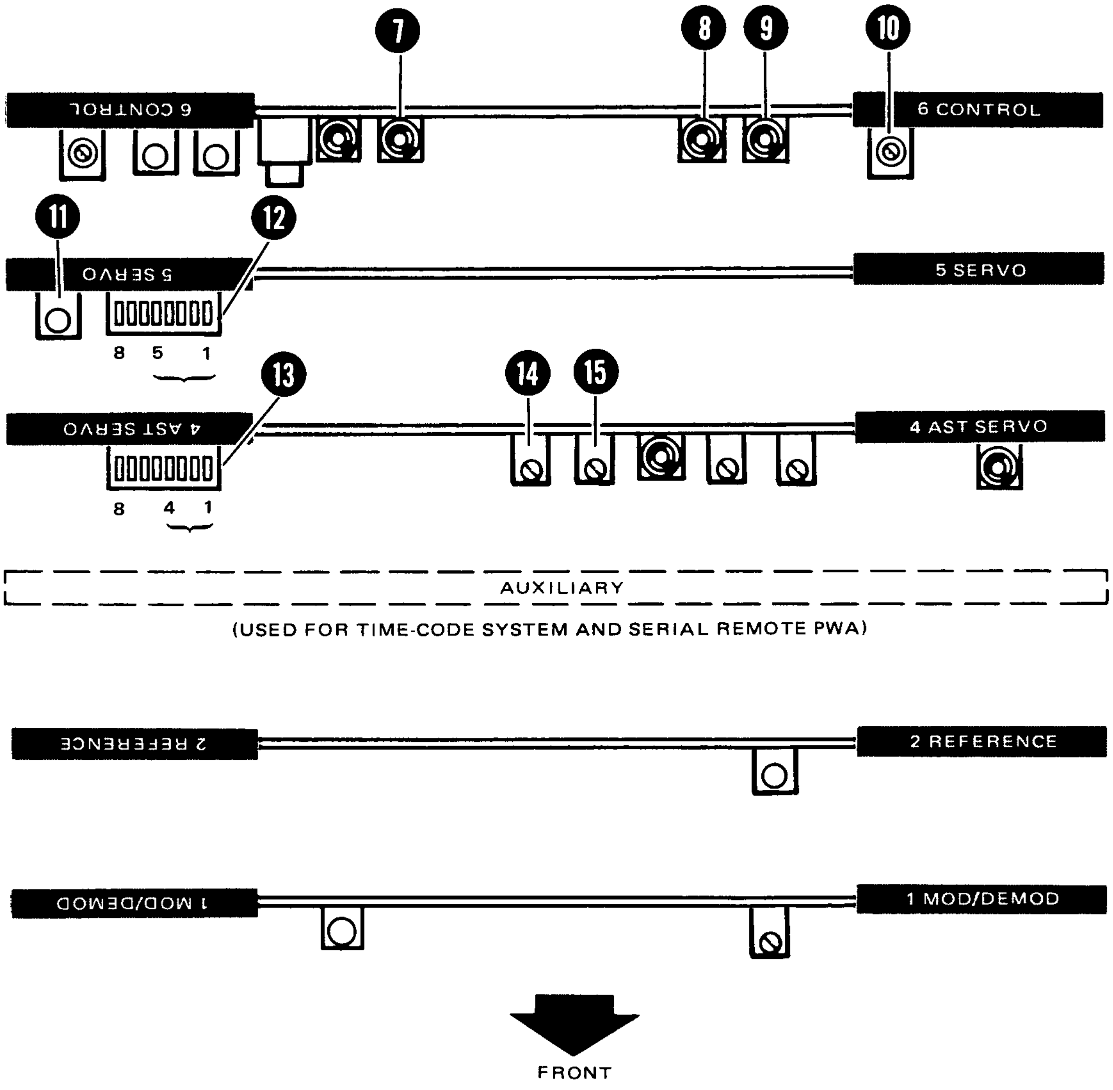
Table 3-6. Card Cage PWA Edge-Mounted Controls and Indicators (Continued)



Index No.	Reference Designation	Control	Function
5	6S2	TEST switch (momentary contact)	Asserts non-maskable interrupt to CPU.
6	6S3	CLR FRAME switch (2 positions: on-off)	Provides on/off control of color framer during play mode. (Normal-invert control is located on the secondary control panel. See Table 3-4.)

(Continued next page)

Table 3-6. Card Cage PWA Edge-Mounted Controls and Indicators (Continued)



Index No.	Reference Designation	Control	Function
7	6S4	DROP FRAME switch (2 positions: DF-FF)	PAL/SECAM systems: not applicable. This switch not activated in PAL or SECAM systems. NTSC/PAL-M systems: Allows use of tape timer as real-time readout when set to DF (frop frame) position.

(Continued next page)

Table 3-6. Card Cage PWA Edge-Mounted Controls and Indicators (Continued)

Index No.	Reference Designation	Control	Function
8	6S5	REF SELECT switch (3 positions: REF-AUTO-INPUT)	When in REF position, timing reference is from external source only. When in AUTO position, automatically selects either video input timing or external timing reference. When in INPUT position, timing reference is from video input only.
9	6S6	PREROLL SEL switch (3 positions: 1 SEC, VARIABLE, 5/7)	When in 1 SEC position, VTR cues to entrance (or exit) point minus 1 second. When in VARIABLE position, enables preroll time which has been set by keypad entry. When in the 5/7 position, preroll point is set 5 seconds ahead of entrance (or exit) point for NTSC systems (7 seconds for PAL, PAL-M , or SECAM systems). When VPR-80 is in preview, auto edit, or edit review modes, tape will cue to selected preroll point.
10	6R109	Remote Shuttle Speed Potentiometer	Adjusts analog value of remote shuttle pot at input to A/D converter.
11	5DS1	CPU indicator (green)	When blinking at 1-Hz rate, indicates that CPU activity is proceeding normally. If indicator is off or on steadily, indicates fault in CPU kernel.
12	5S1	SCANNER PHASE switch	An 8-section DIP switch; S1-1 is LSB: closed position is active. Sections 1 through 5 are set to provide offset timing required by particular TBC used. Five-bit word represents TBC lead time in 1/2H steps.
13	4S1	TRACK JUMP TIMING switch	An 8-section DIP switch: closed position is active. Sections 1 through 5 are binary weighted (S1-1 is LSB), and are set to provide symmetrical jump track timing. Also used in frequency null, damping phase and gain, and jump track gain adjustments. See Section 5, Part II.
14	4R84	DAMP PHASE potentiometer	Provides adjustment of AST damping phase. Interactive with DAMP GAIN pot 4R85 (index 15). See Section 5, Part II.
15	4R85	DAMP GAIN potentiometer	Provides adjustment of AST damping gain. Interactive with DAMP PHASE pot 4R84 (index 14). See Section 5, Part II.

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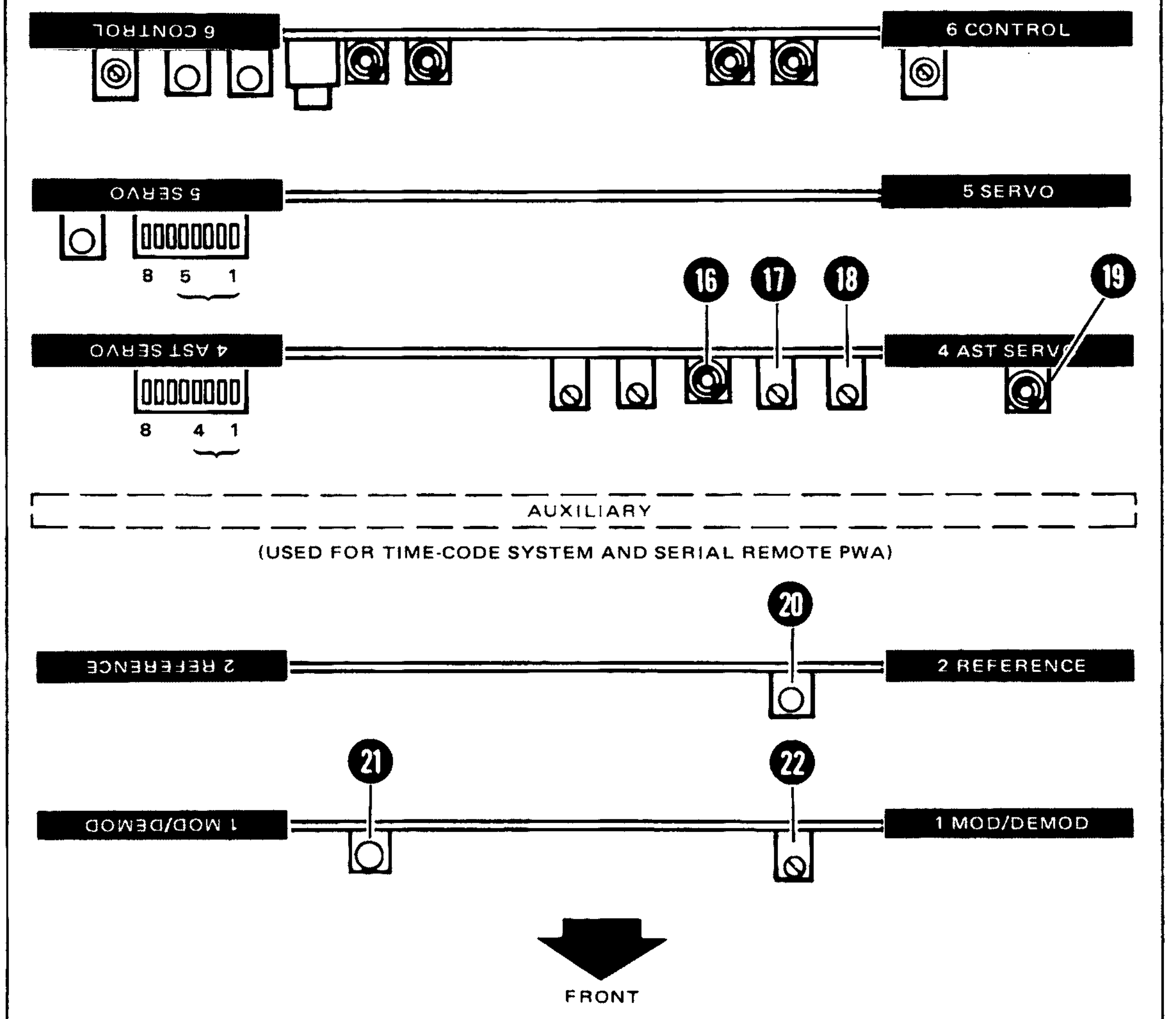
Table 3-6. Card Cage PWA Edge-Mounted Controls and Indicators (Continued)



Index No.	Reference Designation	Control	Function
16	4S2	NULL TEST switch (momentary contact)	When depressed, disconnects AST sense circuitry and connects output of null test frequency generator to AST error output. See Section 5, Part II.
17	4R114	NULL FREQ potentiometer	Provides adjustment of AST null frequency. Used with NULL TEST switch 4S2 (index 16). See Section 5, Part II.

(Continued next page)

Table 3-6. Card Cage PWA Edge-Mounted Controls and Indicators (Continued)

Index No.	Reference Designation	Control	Function
18	4R115	JUMP LEVEL potentiometer	Provides adjustment of AST jump track gain See Section 5, Part II.
19	4S3	AST ON/OFF switch	Normally ON. When ON, ensures accurate tracking of recorded video material. OFF position is used when checking video head tracking performance. See Section 5, Part II.
20	2DS1 (525-line systems)	RS170A window indicator (green)	When lighted, indicates that color frame phase (ScH) is within RS170A specification. See Section 3, Part II.
20	2DS1 (625-line systems)	STD (Sc-H) indicator (green)	When lighted, indicates that color frame phase (ScH) is within EBU specification. See Section 3, Part II.
21	1R133	DG CONT potentiometer	Provides differential gain adjustment. See Section 3, Part II.
22	1R248	DP CONT potentiometer	Provides differential phase adjustment. See Section 3, Part II.

3-6 MODES OF OPERATION

Five basic operating modes can be selected: stop, record, playback, shuttle, and cue. Within each mode, various conditions can be established that enable the VTR to perform special functions such as still frame, slow-motion playback, editing, and unthread. All modes of operation can be initiated locally on the primary control panel, or from the remote control accessory. Any operating mode can be terminated by commanding any other basic mode. It is not necessary to command stop mode before entering another mode. The following paragraphs describe each basic mode and operating condition. Detailed operating instructions are given in the *VPR-80 Installation and Operation* manual.

3-7 Stop Mode

Stop mode has two conditions: standby and ready. When power is initially applied to the VTR, the machine is automatically in stop mode/standby condition.

3-8 Standby Condition

In standby condition, all motors are stationary, reel brakes are engaged, and tape is not under tension. The VTR is automatically placed in stop mode/standby condition when power is first applied, at end-of-tape, or as a result of certain malfunctions. If the VTR is in stop mode/standby condition, and the operator presses one of the basic mode switches, the scanner motor will immediately start, but the commanded mode cannot be entered until the scanner motor reaches near-synchronous speed.

3-9 Ready Condition

In the ready condition, the scanner motor is running at synchronous speed. After tape is threaded, the VTR can be placed in ready condition (from standby condition) by pressing READY. READY and SERVO indicators will light, and the scanner motor will start and come up to speed. Ready condition is achieved when the scanner motor reaches lock speed. At that time the lighted SERVO indicator goes out. From the ready condition, the VTR can be commanded to immediately enter any other mode.

3-10 Still-Frame Operation

Assuming that a prerecorded tape has been threaded and that the VTR is in stop mode/ready condition, switching from EE to tape (EE indicator not lighted) produces still-frame playback on the video monitor. The video head on the scanner continuously reads the same helical scan track (video field) on the tape. The time-base corrector corrects it and produces a standard two-field (NTSC) or four-field (PAL) video frame which is routed to the video output and monitor. This method of still-frame operation can be exited by pressing the EE switch/indicator to return to EE operation (EE indicator lighted).

In order to prevent tape and video head damage, tape tension is released, and tape-to-EE signal switching will occur automatically after approximately 4 minutes of still-frame operation. After the first 3-1/2 minutes of still-frame operation the READY indicator will flash, indicating still-frame termination in approximately 30 seconds. You can continue still-frame operation beyond that interval by depressing READY, thereby resetting the 4-minute timer. If you know in advance that you will want more than 4 minutes of still-frame operation, it is not necessary to wait for the READY indicator to flash. STOP can be pressed at any time to recycle the 4-minute timer.

3-11 Record Mode (Nonedit)

All normal recording and editing operations are functions of record mode. In normal (nonedit) recordings, all record heads are active and all tracks are recorded. Recordings on individual, selected tracks are considered to be editing operations. Record mode is entered by simply pressing RECORD and PLAY at the same time.

3-12 Playback Modes

Playback mode includes normal speed playback of prerecorded material, still-frame playback, and variable-speed playback. Variable-speed playback ranges from still frame to approximately 1.5X normal speed forward. Variable-speed playback is enhanced by the AST feature and the time-base corrector accessory, both of which enable the VPR-80 to provide broadcast quality video without noise bars and picture breakup.

3-13 Normal

Normal (nonedit) playback mode is initiated by simply pressing PLAY. Prerecorded material can be viewed on the monitor. Edit play modes are discussed in paragraph 3-21.

3-14 Tape Speed Override

When the VPR-80 is part of a centrally controlled editing system, VTRs in the system are synchronized by the central edit controller. In the absence of system sync, TSO ADVANCE and RETARD switches provide local control for synchronization. These momentary contact switches are enabled in play mode, and while depressed, they provide a 7% increase or decrease in tape speed. Thus, synchronization is achieved by advancing or retarding playback tape speed of one VTR until the indicated tape time, picture, or audio matches that of the other(s).

3-15 Variable Play

Variable-play playback mode is initiated by simply pressing VAR PLAY. The tape speed knob is then rotated to control play (tape) speed as desired. Tape speed is continuously variable from still frame at the maximum counterclockwise position of the tape speed control to 1.5X normal play speed at the maximum clockwise position. When tape speed control is rotated to the PLAY position, the PLAY indicator lights. At this position of tape speed control, tape speed may not be precisely normal play speed, but it is very close.

3-16 Pause

Pause capability enables tape travel to be stopped when in variable play mode and then restarted at the same tape speed commanded by the rotational position of the tape speed control knob. Pause is commanded by simply pressing the VAR PLAY switch a second time. It is therefore a convenient means of stopping the tape in variable play mode while the tape editor makes a note of the tape time or makes other editing decisions. While the tape is thus stopped, the VAR PLAY indicator flashes. Tape travel is restarted at the same variable speed simply by pressing VAR PLAY again.

3-17 Still Frame

Still-frame operation can be initiated when in stop mode/ready condition as described in paragraph 3-10. However, when initiated in variable-play mode the operator is able to view a succession of still frames.

In still-frame operation of variable-play mode, tape tension is released, and EE signal switching will occur automatically after approximately 4 minutes of still-frame operation. After the first 3-1/2 minutes of still-frame operation the READY indicator will flash, indicating still-frame termination in approximately 30 seconds. You can continue still-frame operation beyond that interval by depressing the READY switch, thereby resetting the 4-minute timer. If you know in advance that you will want more than 4 minutes of still-frame operation, it is not necessary to wait for the READY indicator to flash. Pressing STOP at any time recycles the four-minute timer.

3-18 Shuttle Mode

Tape can be moved at speeds up to 300 in/s (762 cm/s) in either direction using the SHUTTLE switch and tape speed control. Depressing SHUTTLE places the VPR-80 in shuttle mode. The SHUTTLE indicator lights and remains on steadily. In shuttle mode, tape speed control is then used to move tape in the desired direction at selected speed.

When the tape speed knob pointer is centered at the top of the knob, there is no tape motion. Rotating the knob clockwise shuttles tape forward to the takeup reel. Tape travel speed is directly proportional to the degree of knob rotation (300 in/s at maximum clockwise rotation). Forward tape travel will automatically stop at a point near the end of tape. Rotating the knob counterclockwise shuttles tape in reverse to the supply reel. As in forward shuttle, tape speed is proportional to the degree of knob rotation. Reverse tape travel will automatically stop at the end-of-tape (EOT) point which is approximately 60 seconds of tape travel from the beginning of the tape.

3-19 Unthread Command

The unthread command (a variation of shuttle mode) causes tape to be unthreaded from the transport and shuttled to the supply reel.

Pressing SHUTTLE twice in succession is the unthread command. On the second closure of the SHUTTLE switch, the indicator begins flashing, and tape is rewound at maximum shuttle speed to the EOT point. When the unthread command is given, the EOT point will not cause the tape to stop. When the EOT point is reached, tape motion slows down, and the scanner motor is turned off. While the scanner motor slows to a stop, the balance of tape on the transport and takeup reel is gently unthreaded.

If the VPR-80 is in shuttle mode (tape shuttling in either direction), pressing SHUTTLE a second time is the unthread command. Unthread operation then proceeds as explained above.

3-20 Cue Mode

Assuming that edit entrance and exit points have been previously set, pressing CUE automatically moves tape at shuttle speed to the selected preroll point ahead of the entrance point. To cue to the entrance point without preroll, simply press CUE twice in succession. When the switch is pressed for the second time, the CUE indicator begins flashing, indicating cue without preroll.

Cueing to the preroll point ahead of the exit point is done by pressing EXIT and then CUE. To cue to the exit point without preroll, press EXIT and then CUE twice in succession. The EXIT indicator is lighted and CUE indicator flashes, indicating cue to the exit point without preroll.

3-21 Editing Modes

An insert edit replaces a segment of existing information within a continuous recording. The inserted edit recording is made exactly over the recording which is replaced. Both entrance and exit points are preselected. In an insert edit the operator must provide individual channel selection to determine exactly which channels of information (audio and/or video) to replace.

An assemble edit patches together individual pieces of raw material into one continuous train on tape. It effectively accomplishes the transition from playback recording to new material recording. Therefore, all channels are recorded, and the operator is concerned only with controlling the timing of the entrance point. All assemble edits are open-ended. In auto assemble edit mode, the operator manually terminates edit recording by switching to another mode (i.e., stop mode). Enough material must be recorded so that the next assemble edit can be made where desired.

3-22 Preview Modes

Preview modes enable the operator to preview a proposed edit and make decisions as to just where he wants to establish the edit point without actually recording the edit on tape. When using preview modes, the operator can mark an edit point, preview it, and trim the edit point until he is satisfied.

3-23 **Edit Preview.** The edit preview mode is used for checking the placement of the edit entrance and exit points.

When previewing is done at the source VTR, the INSERT (or ASSEM) indicator is off and AUTO indicator is on. The tape is first cued to the preroll point ahead of the entrance point. Edit preview is initiated by pressing PLAY. The source VTR is in EE operation during the preroll. It switches to off-tape playback during the edit interval, and switches back to EE operation at the edit exit point.

When previewing is done at the record VTR, INSERT (or ASSEM) and AUTO indicators are on. Tape is first cued to the preroll point ahead of the entrance point. Edit preview is initiated by pressing PLAY. The record VTR is in off-tape playback mode during preroll. It switches to EE operation during the edit interval, and switches back to off-tape playback mode at the edit exit point.

3-24 **Exit Point Preview.** The exit point preview mode is used for checking the exit point of an edit when the edit interval is lengthy. For example, if the edit interval is several minutes long, exit preview mode spares the operator from having to run through the entire edit in order to check the exit point.

When previewing is done at the source VTR, the INSERT (or ASSEM) indicator is off, and AUTO indicator is on. Both VTRs are first cued to the preroll point ahead of the exit point. Exit point preview is initiated by pressing the PLAY switch. The source VTR is in off-tape playback mode during the preroll and edit interval. It switches to EE operation at the edit exit point.

When previewing is done at the record VTR, INSERT (or ASSEM) and AUTO indicators are on. Both VTRs are first cued to the preroll point ahead of the exit point. Exit point preview is initiated by pressing the PLAY switch. The record VTR is in EE operation during the preroll and edit interval. It switches to off-tape playback mode at the edit exit point.

3-25 Auto Edit Mode

Auto edit mode is enabled when two VPR-80 machines (one source and one record VTR) are connected via the multi-VTR cable. The AUTO indicator of the record VTR is lighted, and AUTO and REM 2 indicators of the source VTR are lighted. The lighted REM 2 indicator on the source VTR indicates that cue and play operations of the source VTR are slaved to the record VTR. The auto edit procedure is controlled from the record VTR.

When the CUE switch on the record VTR is pressed, both source and record VTRs are cued to the preroll point ahead of the entrance point. Auto edit mode is initiated by pressing PLAY and RECORD at the same time. Both VTRs are in play mode during the preroll. At the entrance point, the record VTR switches to record mode, recording incoming material from the source VTR. At the exit point, the record VTR switches back to play mode.

3-26 Edit Review Mode

The edit review mode is used after the edit has been recorded, enabling the operator to go back and look at what he has just committed to tape on the record VTR. The edit review procedure enables the last edit to be monitored directly off the record VTR without taking the record VTR out of auto edit mode. This means that the AUTO and either INSERT or ASSEM switches are left ON and do not need to be turned off when doing an edit review. The edit review procedure is controlled from the record VTR.

Edit review mode is initiated by pressing PLAY twice in succession. When in edit review mode, the PLAY indicator flashes. The record VTR tape is cued to the entrance preroll point and off-tape playback of the edit begins. If the review is to be repeated, the operator simply presses PLAY again. Tape cues to the entrance preroll point, and playback of the edit is repeated. The PLAY indicator continues flashing during playback until the exit point is reached. At that time the PLAY indicator remains on steadily, indicating that edit review is complete.

3-27 Open-Ended Insert Edit Mode

An open-ended insert edit involves marking an entrance point and then recording an edit without setting a specific exit point beforehand. The open-ended insert edit is terminated with the STOP (or any other mode command) switch at the operator's discretion. The open-ended edit mode is enabled by making contents of the entrance and exit registers equal.

3-28 Manual Editing

When making manual edits, the operator is not primarily concerned with tape time, but is observing program material recorded on the master tape and initiating and terminating the edit recording at appropriate times. Runup time to the entrance point must be calculated by the operator, and play-to-record-mode switching must be done skillfully in the absence of automation provided by the auto edit mode.

3-29 **Manual Insert Edit**. When making a manual insert edit, the operator is concerned with both ingoing and outgoing edit points. Characteristic picture breakup at the end of nonedit and assemble edit recordings is avoided since the control track record head is not turned on, and edit recording is synchronized to the existing control track on tape. Two methods of making manual insert edits are given in the *VPR-80 Installation and Operation* manual.

3-30 **Manual Assemble Edit**. When making a manual assemble edit, edit recording is initiated by pressing PLAY and RECORD at the same time, as in nonedit recording. The operator terminates the edit by pressing the PLAY (or any other mode) switch. No matter how the edit is exited, picture breakup is produced at the outgoing point on the master tape. This also occurs on nonedit recordings.

The new control track to be recorded with the assemble edit must be properly phased before edit recording begins. Therefore, the tape must have a continuous control track recording, at least over the proposed runup period. The operator must consider two major aspects in deciding where to make the ingoing edit point. First, regardless of whether the assemble edit is to be added to a previous assemble edit or to a nonedit recording, the new edit segment must re-record over the picture breakup at the end of the recording on tape. Second, the operator must also allow enough runup time for all servos to lock, and control track recording to rephase, before edit recording begins. When making a series of assemble edits, the operator should therefore make each assemble edit recording longer than actually desired. Thus, ample time is allowed for runup to [illegible] ingoing point of the next assemble edit.

3-31 Remote Control Modes

There are four different mechanisms for remote control of the VPR-80: multi-VTR, simple, parallel, and serial remote control. Multi-VTR control is a standard capability and can be enabled at the primary control panel. Multi-VTR control is used for automatic editing between source and record VTRs without the use of any external editing accessories. Connections for simple remote control, which are also standard, are included in the multi-VTR connector. Implementation of simple remote control is left to the user's option. Parallel and serial remote control capabilities are accessories to the VPR-80. The Parallel Remote PWA provides a 75-pin connector for parallel control and interfacing with Ampex video tape editing accessories. The serial control accessory is a SMPTE-proposed RS422-compatible serial remote interface.

Whereas the REM 2 switch activates standard multi-VTR remote control capability, the REM 1 switch activates either parallel, serial, or simple remote control capability. The source of remote control input is determined by the remote 1 input selection setup procedure.

PART I
SECTION 4
SYSTEM MAINTENANCE

4-1 GENERAL

This section of the manual presents the general maintenance information which is referenced in Part II. Measurement and adjustment procedures are given which assure interchangeability of Type C format tapes recorded by different VTRs. The derivation and significance of nonstandard condition (system) and fault indications are tabulated. None of the maintenance procedures in this section requires removal of the VPR-80 from rack, consolette, pedestal, or console mounting.

Detailed adjustment and part replacement instructions for individual PWAs and subassemblies, where removal from the VPR-80 is required, are given in Part II of this manual.

4-2 MAINTENANCE INFORMATION

4-3 Recommended Tools and Test Equipment

Maintenance and servicing of the VPR-80 should be done in a well-lighted, dust-free, and temperature-controlled environment. The maintenance facility should be equipped with the tools, test equipment, and other special-purpose items listed in Table 4-1. In addition, accessory VPR-80 General Service and Maintenance Tools and Parts Kits are considered essential to VPR-80 maintenance. A Diagnostic Kit (Ampex P/N 1450981) which includes the diagnostic probe is required for troubleshooting when using the diagnostic programs.

4-4 Accessory Kits

Three accessory kits of tools and other VTR maintenance equipment are available from Ampex. The VPR-80 General Service Kit (which includes this manual) is an accessory to VPR-80s with NTSC, PAL/SECAM, or PAL-M video systems. See paragraph 4-5. Two maintenance tool kits are also available, one for 60-Hz systems, and one for 50-Hz systems. See paragraph 4-6. Contents of these kits complement tools and test equipment listed in Table 4-1. Table 4-2 is a list of recommended miscellaneous parts.

4-5 General Service Kit. Contents of the VPR-80 General Service Kit (Ampex No. 1450013) are listed in Table 4-3.

4-6 Maintenance Tool Kits. Contents of the VPR-80 Maintenance Tool Kit for 60-Hz systems (Ampex No. 1467850) are listed in Table 4-4. Contents of the VPR-80 Maintenance Tool Kit for 50-Hz systems (Ampex No. 1467853) are largely the same as those of the 60-Hz system kit. Differences are noted in Table 4-4.

Table 4-1. Recommended Tools and Test Equipment

Equipment Type	Suggested Model	Used For
Flutter meter	Micom (Bahrs) Model 8100-W	Measuring transport wow and flutter.
AC voltmeter	Hewlett-Packard Model 400FL or 3400A	Measuring ac voltages.
Digital voltmeter	Hewlett-Packard Model 3435A	Measuring dc voltages.
Frequency counter	Hewlett-Packard Model 5300A/5302A	Measuring tape record mode speed.
Wideband oscilloscope with high gain preamplifier	Tektronix Model 7603 with 7A13, 7A26, and 7B53A plug-ins	Alignment and servicing.
Current transformer probe	Tektronix Model CT-2, P/N 015-046 mV/mA into 50 Ω	General servicing and adjusting video.
Television signal generator	Tektronix Model 147 (NTSC) or Model 148 (PAL) or Model 148-M (PAL-M)	Video signal system alignment and servicing.
Gen Lock Test Signal Generator	Tektronix Model 146 (NTSC) or Model 145 (PAL) or Model 145-M (PAL-M)	Video signal system alignment and servicing.
Color Field Identifier	Ampex P/N DT1392863	Video signal system alignment and servicing.
Spectrum analyzer	Hewlett-Packard Model 141T RF Section 8553B IF Section 8552B Tracking Gen. 8443A	Video signal system alignment and servicing.
Spectrum analyzer	Hewlett-Packard Model 3580A	Audio harmonic distortion and erasure check.
Video noise meter	Rohde and Schwarz Model BN120312	Measuring video signal-to-noise ratio.
Audio oscillator	Hewlett-Packard Model 651B or 209A	Performance check and alignment.
Color picture monitor	Tektronix 655 NTSC/PAL	Video signal system alignment and servicing.

(Continued next page)

Table 4-1. Recommended Tools and Test Equipment (Continued)

Equipment Type	Suggested Model	Used For
Vectorscope	Tektronix 520 NTSC	Video signal system alignment and servicing.
Waveform monitor	Tektronix 529	Video signal system alignment and servicing.
Storage scope	Tektronix Model 7313 or other dual trace storage scope	Verifying edit timing.
Scanner shipping and carrying case	Ampex P/N 1401347	Shipping scanner assembly.
Head demagnetizer	Ampex P/N 4040575	Demagnetizing audio and video heads, tape guides, and capstan (115V operation only).
Bulk demagnetizer	Taberaser	Demagnetizing trim plates and other large components in tape path.
Head cleaner	Ampex P/N 087-007.	Cleaning heads, scanner, and tape guides.
Precision plastic shim stock; 10 mil, 12 mil	Artus Corp. (10 x 20 in. kit) (Ampex P/N 940-007)	Pin-to-scanner gap measurement
Gram gauge, – 1g	Correx Co. Model 475-15	Pin-to-scanner gap measurement.
Dial indicator	Starrett Model 711-HS	Replacing scanner slip ring brushes.
Feeler gauge	Starrett Model 467	Measuring various transport clearances.
Spring scale, 10 lb (4.54 kg)	Catillon, Model DPP-2500 (Ampex P/N 650-104)	Pinch roller pressure adjustment.
Isopropyl alcohol–92%		Cleaning capstan pinch roller and shaft.

(Continued next page)

Table 4-1. Recommended Tools and Test Equipment (Continued)

Equipment Type	Suggested Model	Used For
Soft lint-free tissues	Kimwipes Ampex P/N 110-015	Various cleaning and component replacement procedures.
Cotton swabs, cotton-tipped swabs	Q-Tip, Ampex P/N 650-080	Various cleaning and component replacement procedures.
Lacing cord	Ampex P/N 296-004	Capstan pinch roller pressure adjustment.
Oil lubricant	Ampex P/N 087-579	Replacing capstan shaft and pinch roller.
Scanner service leg set assembly	Ampex P/N 1401302	Supporting scanner assembly when removed from transport
Collet tool	Ampex P/N 360-489	Removing knob from potentiometer shaft.
Dry film lubricant	Ampex P/N 087-581	Replacing pinch roller arm.

Table 4-2. VPR-80 Miscellaneous Parts Kit

Ampex P/N	Description	Quantity
1463203	Tool, Brush Installation	1
060-407	Lamp, Incandescent, 14V, 80 MA	5
070-492	Fuse Part, Holder	2
070-004	Fuse, Cartridge, Slow Blow, 1 Amp, 3 AG	5
070-020	Fuse, Cartridge, Slow Blow, 5 Amp, 3 AG	5
070-486	Fuse, Ceramic Tube, 10 Amp, 250V	5
070-487	Fuse, Ceramic Tube, 15 Amp, 250V	5
070-490	Fuse Part, Carrier Cap, for 3 AG Fuse	6
070-491	Fuse Part, Carrier Cap, for 5 x 20 MM Fuse	6
102-118	Reel, Take-up, 11.75 Dia.	1
140-437	Connector, Plug, 2 Socket (Jumper)	5
177-216	Connector Part, Kit, Strain Relief (Serial)	1
177-217	Connector Part, Kit, Strain Relief (Monitor)	1
177-218	Connector Part, Kit, Strain Relief (Multi-VTR)	1
177-210	Connector Part, Kit, Strain Relief (TBC)	1
167-845	Connector Part, Body, Plug, Rect, 9 Pos (Serial)	1
167-639	Connector Part, Body, Plug, Rect, 15 Pos (Monitor)	1
167-079	Connector Part, Body, Plug, Rect, 25 Pos (Multi-VTR)	1
167-648	Connector Part, Body, Plug, Rect, 37 Pos (TBC)	1
167-763	Connector Part, Contact, Pin, 20-24 AWG	86

Table 4-3. VPR-80 General Service Kit

Ampex P/N	Description	Quantity
1463203	Tool, Brush Installation	1
1430334	PWA, 6802 No-Op Generator	1
1430246	Schematic, 6802 No-Op Generator	1
1809547	VPR-80 Service Manual	1
1809548	VPR-80 Parts Lists and Schematics Manual	1
360-449	Screwdriver, Key, Hex, Ball-Ended, 0.140 AF	1
360-489	Nut Driver, Metric, Slotted, 15 mm	1
435-239	Test Clip, IC, 28-Position	1
800-790	Test Clip, IC, 16- Position	16

Table 4-4. VPR-80 Maintenance Tool Kits

Ampex P/N	Description	Quantity	Notes
1498600	Tape, Audio Alignment, 525/NTSC	1	*
1498601	Tape, Audio Alignment, 625/PAL	1	**
1498604	Tape, Highband Carrier Video Reference, 525/NTSC		*
1498605	Tape, Highband Carrier Video Reference, 625/PAL	1	**
1498608	Tape, Guide Adjustment, 625/PAL	1	*
1498609	Tape, Guide, Adjustment, 625/PAL	1	**
1498614	Tape, Biased Control Track Reference Level	1	**
360-029	Screwdriver, Xcelite R-144	1	
360-049	Screwdriver, Xcelite R5166	1	
360-054	Screwdriver, Xcelite X-101	1	
360-053	Screwdriver, Xcelite X-102	1	
360-420	Screwdriver, Xcelite X-103	1	
360-419	Solder Remover, Soldavac SV-26	1	
360-421	Screwdriver Set, Xcelite PS-88	1	
360-422	Allen Screwdriver Set, Xcelite 99-PS-40	1	
360-423	Nut Driver, Set, Xcelite PS-120	1	
360-445	Tool, Handle, Snap-Lock	1	
360-446	Tool, Screwdriver, Key, Hex, 0.094 AF	1	
360-448	Tool, Screwdriver, Key, Hex, Ball-Ended, 0.109 AF	1	
360-498	Weight Set, Tension Gauge, Calibration	1	
360-449	Screwdriver, Key, Hex, Ball-Ended, 0.140 AF	1	
360-497	Gauge, Tape Tension (Tentelometer)	1	
360-489	Tool, Metric, Knob Removal	1	
360-496	Tool, Extractor (Elco)	1	
435-244	Clip, Test, IC, 40-Pin	2	

* Part of Tool Kit 1467850(60 Hz) only
** Part of Tool Kit 1467853(50 Hz) only
Note: Items without asterisks are included in both parts kits.

(Continued next page)

Table 4-4. VPR-80 Maintenance Tool Kits (Continued)

Ampex P/N	Description	Quantity	Notes
435-239	Clip, Test, IC, 28-Pin	2	
800-790	Clip, Test, IC, 16-Pin	2	
1400250	PWA, Record Driver Extender	1	
1401302	Leg Set Assy, Scanner Service	1	
1461390	Tool Assy, Tension Adjust	1	
1465475	Flux Loop Assy	1	
1463203	Tool, Brush Installation	1	
1463350	Kit, Tip Projection Gauge	1	

4-7 Reference and Alignment Tapes

Ampex reference and alignment tapes are listed in Table 4-5. Most of them are included in the maintenance tool kits (Table 4-4). Other tapes listed in Table 4-5 can be ordered separately.

Table 4-5. Reference and Alignment Tapes

Ampex Catalog Number	Standard	Description	Length (Min)	Notes
1498600	525/NTSC	Audio Alignment	15	*
1498601	625/PAL	Audio Alignment	15	**
1498602	525/NTSC	Audio Flutter (3 kHz at 9.6063 in/s)	5	
1498603	625/PAL	Audio Flutter (3 kHz at 9.4409 in/s)	5	
1498604	525/NTSC	Highband Carrier Video Reference	30	*
1498605	625/PAL	Highband Carrier Video Reference	30	**
1498606	625/SECAM	Highband Video Reference	30	
1498608	525/NTSC	Guide Adjustment	10	*
1498609	625/PAL	Guide Adjustment	10	**
1498614	625/PAL	Biased Control Track Reference Level (1 kHz at 9.4409 in/s, 100 nWb/m)	5	**
1498623	525/NTSC	Video and Audio Reference (Recorded in accordance with SMPTE document V56.4-634)	10	
1498625	525/NTSC	Programmed Dropout	15	
1498626	525/PAL	Programmed Dropout	15	

* Included in Maintenance Tool Kit 1467850 (60 Hz) only
** Included in Maintenance Tool Kit 1467853 (50 Hz) only

Every Ampex alignment tape is a first-generation original, produced by specially modified master recorders. Before any reference or alignment tape is recorded, each machine is carefully aligned and calibrated to a master vault tape. It is then monitored continuously to assure absolute compliance and adherence to frequency reproduction and other measurement parameters. Though voice tags are dubbed, all test signals are supplied directly to record amplifiers from the most accurate programmable tone and signal generators available.

4-8 Caring for Alignment Tapes

Due to the precise nature of alignment tapes, certain precautionary measures should be taken in order to prolong their usefulness. One enemy of any magnetic tape is physical deterioration. Tape edge deformation, for example, can result in uneven tracking. Edge deformation occurs whenever tape is unevenly spooled and subsequently crushed by reel flanges. Care should be taken to allow for a smooth, compact tape pack, during both play and shuttle modes.

Magnetized heads and tape guides must be avoided. It is essential to clean and demagnetize heads and tape guides frequently in accordance with the instructions given in paragraph 4-14. Use only approved cleaners noted in paragraph 4-14.

Alignment tapes should always be stored in a safe, dry environment. Changing temperature and humidity can have an adverse effect on tape base material, causing it to alternately swell and shrink. This results in tape degradation, affecting tape's usefulness as a reference tape. When an alignment tape is played, it should *never* be stopped during the middle of a test. If a mistake occurs, allow the tape to play through to the end. Then rewind it carefully and start again. Stopping and starting a tape during a pass results in unnecessary tape tension changes, thus increasing the possibility of tape stretch and distortion of the recorded signal.

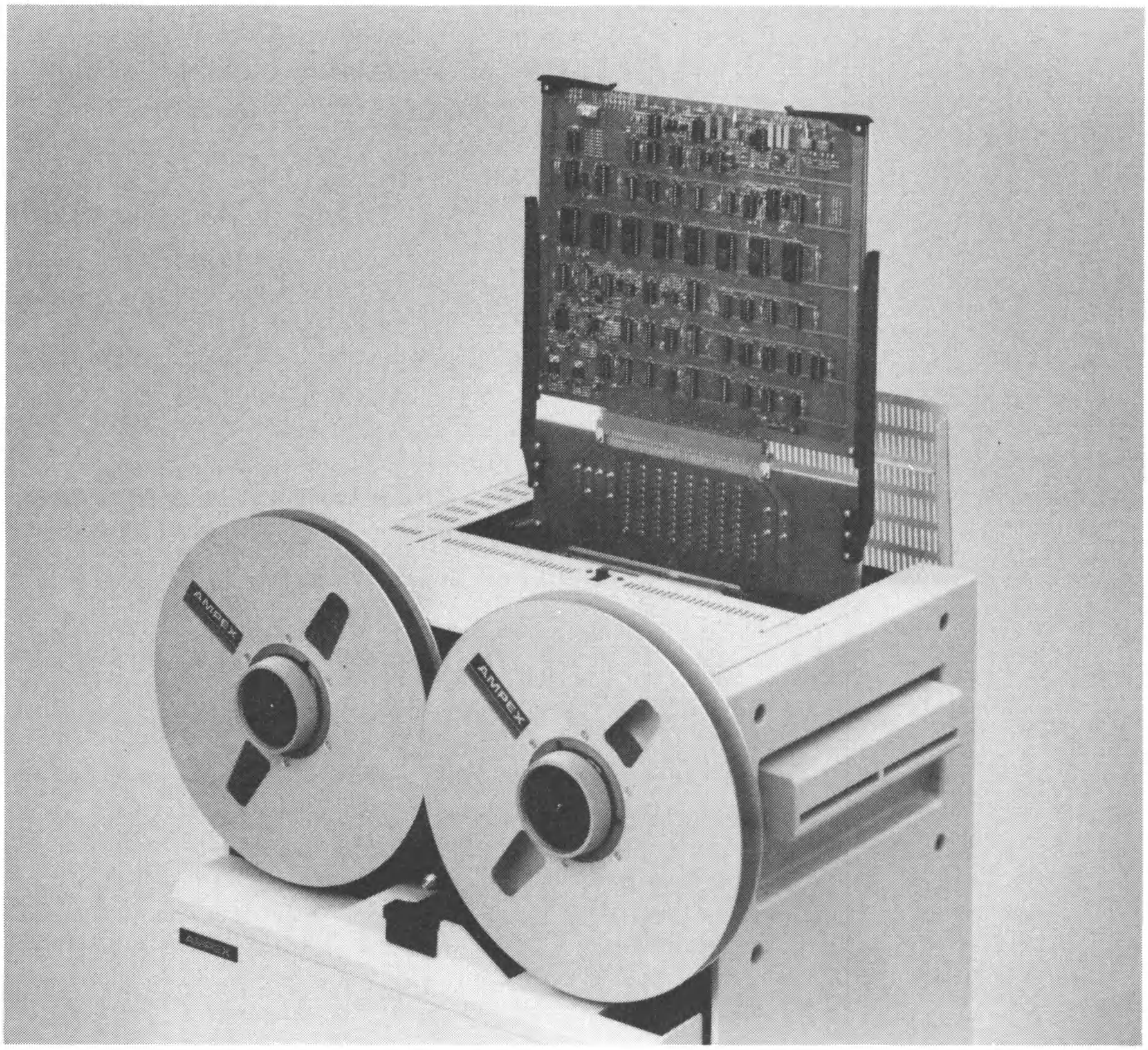
Finally, two factors which cannot be ignored: wear and age. Each time a tape is played, physical wear and signal deterioration occur. Thus, an alignment tape should be carefully monitored, and after 20 to 25 passes or one to two years of use, it should be replaced.

4-9 Maintenance Access

4-10 General

Limited access is available for maintenance purposes without panel removal or other disassembly of the VPR-80. Opening one door on the VPR-80 cabinet top provides access to the PWA-edge test points and controls in the card cage. Opening this door also allows PWAs in the card cage to be mounted on extender boards as shown in Figure 4-1.

Access to Control Panel PWAs, the AST Driver PWA, speed control pot, speaker, and other components beneath the primary control panel is obtained by loosening two captive screws and pivoting the control panel assembly forward, as shown in Figure 4-2. To make access to these components easier, it is possible to allow the transport front cover to hang straight down. Access to the Audio PWA, MDAs, rear



15942-12

Figure 4-1. PWA Mounted on Extender Board

of the transport assembly, and the card cage motherboard is obtained by loosening two captive screws and pivoting the entire rear door assembly backward as shown in Figure 4-3.

Instructions for removal of hardware-attached PWAs and subassemblies from the VPR-80 are spelled out in individual sections of Part II of this manual.

4-11 Trim Removal

4-12 **Transport Trim.** The transport trim piece and longitudinal head cover must be removed for access to the transport subsystem components.

Remove transport trim piece from the VPR-80 as follows:

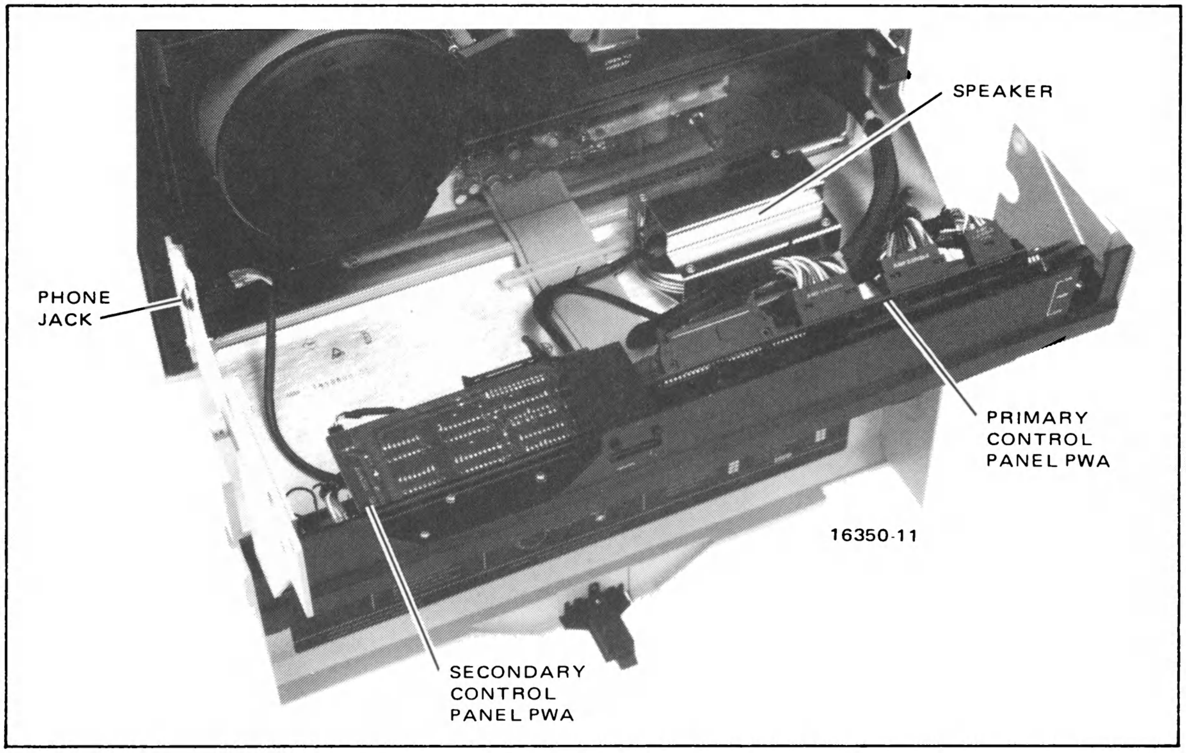


Figure 4-2. Control Panel Assembly Pivoted Forward

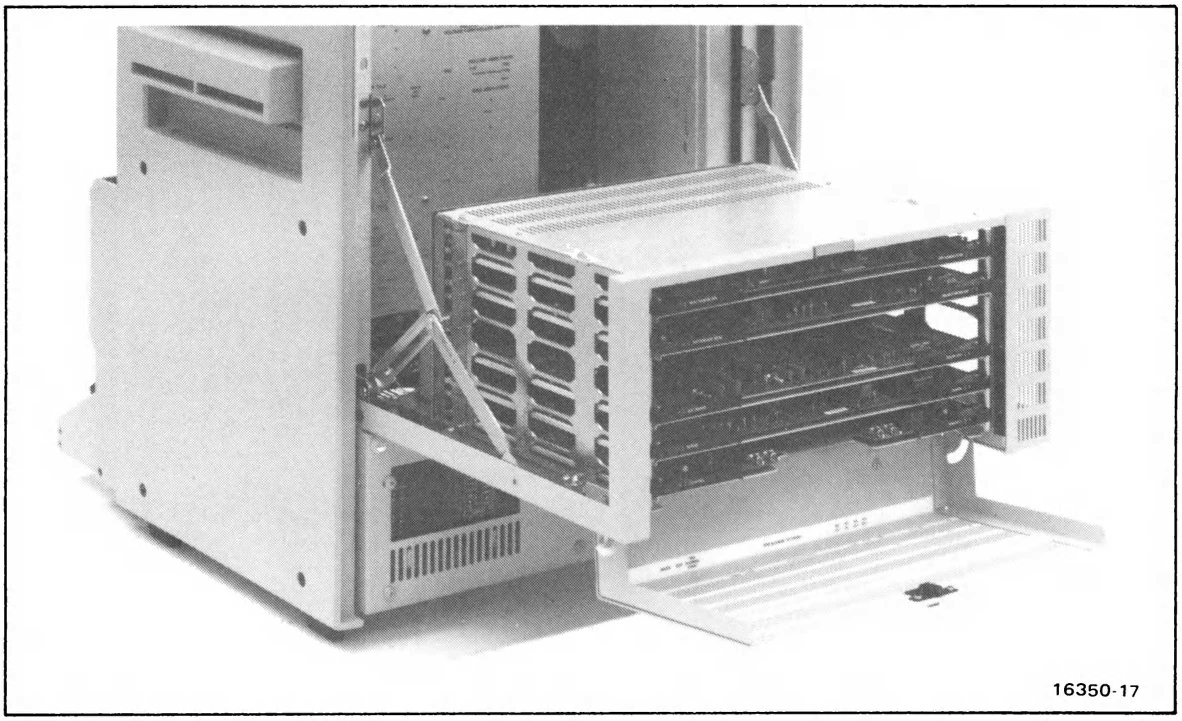


Figure 4-3. Rear Door Assembly Pivoted Backward

STEP 1 Remove tape reels, if installed, and lower hinged transport cover assembly.

STEP 2 Loosen captive screw which secures head cover (Figure 4-4) and detach head cover.

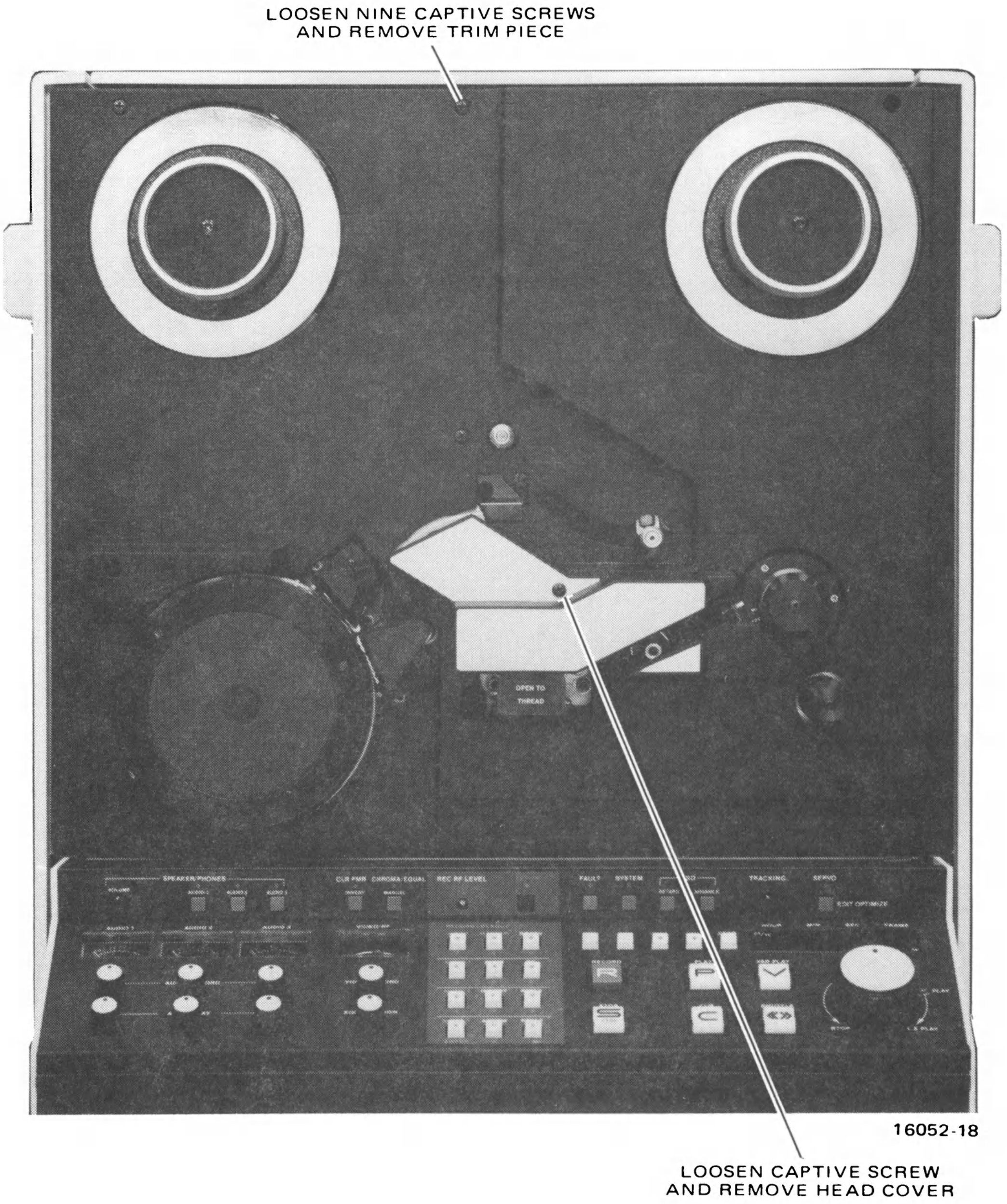

LOOSEN NINE CAPTIVE SCREWS AND REMOVE TRIM PIECE
16052-18
LOOSEN CAPTIVE SCREW AND REMOVE HEAD COVER

Figure 4-4. Head Cover and Transport Trim Removal

STEP 3 Loosen nine captive screws which secure transport trim piece.

STEP 4 Gently pull transport trim piece straight forward and away from transport. Be careful not to damage scanner surface or video heads.

4-13 **Side Panels.** The side panels cover attaching hardware for the power supply and regulator subsystem. The side panels need not be removed unless it is necessary to remove the power supply for maintenance. Six screws and washers secure each side trim panel. Remove this hardware, and detach the two side trim panels as shown in Figure 4-5.

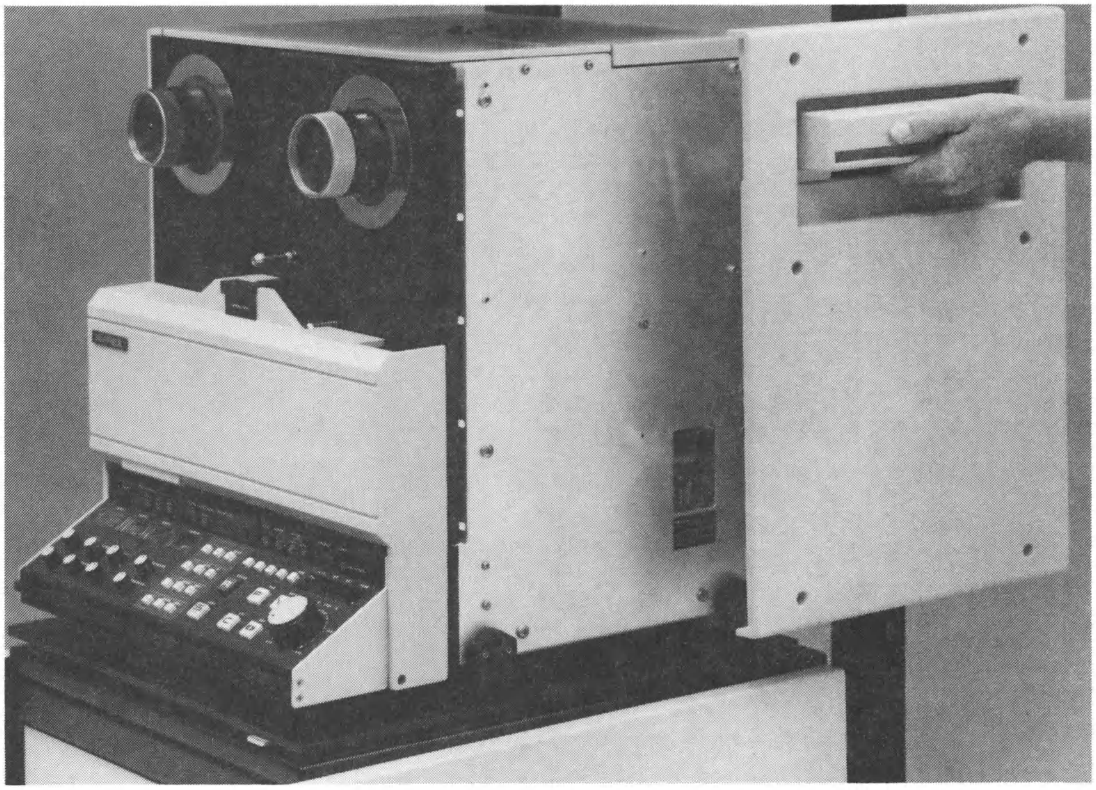


Figure 4-5. Side Panel Removal

4-14 Cleaning Instructions

Cleaning operations which do not involve disassembly of the VPR-80 are a responsibility of the VTR operator, and instructions are given in the *VPR-80 Installation and Operation* manual. However, since they are referenced in many of the following maintenance procedures (and include several important precautions) these instructions are repeated in the following paragraphs.

4-15 Schedule

Keeping the VPR-80 transport and scanner components clean is essential to maintaining recording quality. Table 4-6 lists recommended cleaning intervals.

Table 4-6. Cleaning Schedule

Parts To Be Cleaned	Cleaning Interval	Paragraph Reference
Heads, tape path, scanner, capstan, and pinch roller	8 hr (once/week min.)	4-16-4-19
Trim panels and cabinet surfaces	As required	
Capstan motor brushes and rotor	2000 hr	4-20
Scanner slip ring and brush assembly	1000 hr	4-20
Scanner motor brushes and rotor	1000 hr	4-20

4-16 Heads and Tape Path

Oxide particles from magnetic tape tend to collect on components in the tape path. These oxide accumulations degrade VTR performance. Heads and all other components in the tape path must be cleaned after each 8 hours of operation, or more frequently, depending on operational environment and the type and cleanliness of the tape used. Visual inspection of scanner, guide, and capstan surfaces should be made before every major record/playback session. If oxide is present on any of these surfaces, the oxide should be removed with cleaning agents recommended in the following paragraphs.

CAUTION

IT IS IMPORTANT TO RESTRICT USE OF CLEANING AGENTS TO PARTS INTENDED TO BE CLEANED, AND TO AVOID USING EXCESS AMOUNTS OF CLEANING AGENT. ALSO AVOID ACCIDENTAL SPILLAGE OF AMPEX HEAD CLEANER. THE CLEANER, WHICH IS XYLENE-BASED, WILL CAUSE SURFACE BLEMISHES ON VPR-80 TRIM PANELS.

4-17 Video Heads and Scanner

Clean video heads and scanner as follows.

CAUTION

DO NOT CLEAN HEADS USING A CLEANING MOTION AT RIGHT ANGLES TO HEAD TRAVEL. THIS CAN CAUSE HEAD DAMAGE. ALSO, DO NOT USE ALCOHOL TO CLEAN SCANNER SURFACE.

ALCOHOL TENDS TO LEAVE A PERSISTENT RESIDUE THAT CAN INCREASE FRICTION BETWEEN TAPE AND SCANNER.

STEP 1 Moisten a cotton swab with Ampex Head Cleaner (Part No. 087-007) or xylene. Hold swab steady in the vicinity of head to be cleaned and rotate upper scanner drum back and forth slowly so that head alternately contacts swab.

STEP 2 Clean scanner with a soft, clean, lint-free paper, using Ampex Head Cleaner or xylene.

STEP 3 Remove all residue from cleaned surfaces.

4-18 Tape Guides, Audio Heads, and Capstan

Clean tape guides, audio heads, and capstan with a cotton swab moistened with Ampex Head Cleaner or xylene. Remove all residue from cleaned surface.

4-19 Pinch Roller

CAUTION

DO NOT USE AMPEX HEAD CLEANER ON RUBBER CAPSTAN PINCH ROLLER. HEAD CLEANER DETERIORATES THE RUBBER SURFACE.

Clean surface of the pinch roller with a soft, clean, lint-free paper or cloth towel moistened with 92% isopropyl alcohol.

4-20 Scanner and Capstan Interiors

To ensure reliable performance, scanner slip rings and brushes may require periodic cleaning. The recommended interval is 1000 hours of operation. Scanner motor brushes and rotor also require cleaning after every 1000 hours of operation. In both cases, the scanner must be removed from the transport assembly and disassembled for cleaning. Detailed instructions are given in Section 5, Part II.

The capstan motor brushes and rotor should be cleaned after every 2000 hours of operation. The capstan is first removed from the transport assembly and then partially disassembled for cleaning. Detailed disassembly and cleaning instructions are given in Section 5, Part II of this manual.

4-21 INTERCHANGE PROCEDURES

VPR-80 playback and/or editing of a video tape recorded on another VPR-80 could be seriously hindered (or prevented) by differences in transport and scanner adjustments. In order to assure interchangeability of videotapes, all VPR-80s are calibrated with Ampex standard reference and adjustment tapes to uniform tape guiding and tracking parameters.

Compliance with criteria stated in the following procedures assures interchangeability. Measurement and adjustment procedures must be performed in the order shown below.

1. Pinch roller pressure adjustment
2. Tape tension adjustments
3. Noise free interval test
4. Track straightness adjustment
5. Scanner tach adjustment
6. Head tip projection measurement
7. Helical scan dropout duration and position adjustments
8. Control track position adjustment

4-22 Pinch Roller Pressure Adjustment

When the capstan pinch roller solenoid is energized (in play and record modes), the pinch roller pressure against the capstan shaft should be 7.00 lb ±0.22 lb (3.2 kg ±0.1 kg). Pinch roller pressure is adjusted by turning a locknut that compresses a spring on the solenoid plunger. See Figure 4-6. To measure and adjust capstan pinch roller pressure, and, if required, to adjust capstan-to-pinch-roller clearance, proceed as follows.

STEP 1 Remove tape and reels from VPR-80 transport.

STEP 2 Remove transport trim as outlined in paragraph 4-12.

STEP 3 Measure clearance between capstan shaft and rubber pinch roller. Clearance should be 0.125 in. ±0.020 in. (3.1 mm ±0.5 mm).

STEP 4 If pinch roller clearance is not correct, loosen two screws that secure stop bracket to solenoid mounting plate (Figure 4-6, A). Adjust position of stop bracket to middle of its range, and tighten screws.

STEP 5 Loosen three screws (B) that secure solenoid mounting plate to transport casting, and adjust solenoid position to obtain clearance specified in step 3.

STEP 6 Place a cotton swab, or other light barrier, between halves of the tape-in-path (TIP) sensor (C). This enables the capstan to rotate and solenoid to be energized in play mode with no tape threaded on the transport.

STEP 7 Thread a metal or plastic hook (approximately 1/2 in.—13 mm—in diameter) on a length of nylon lacing cord. Knot the cord in a loop which should be 6 to 8 in. (152 to 203 mm) long when pulled taut. Place the loop of cord on the hook of the spring scale specified in Table 4-1. See Figure 4-7.

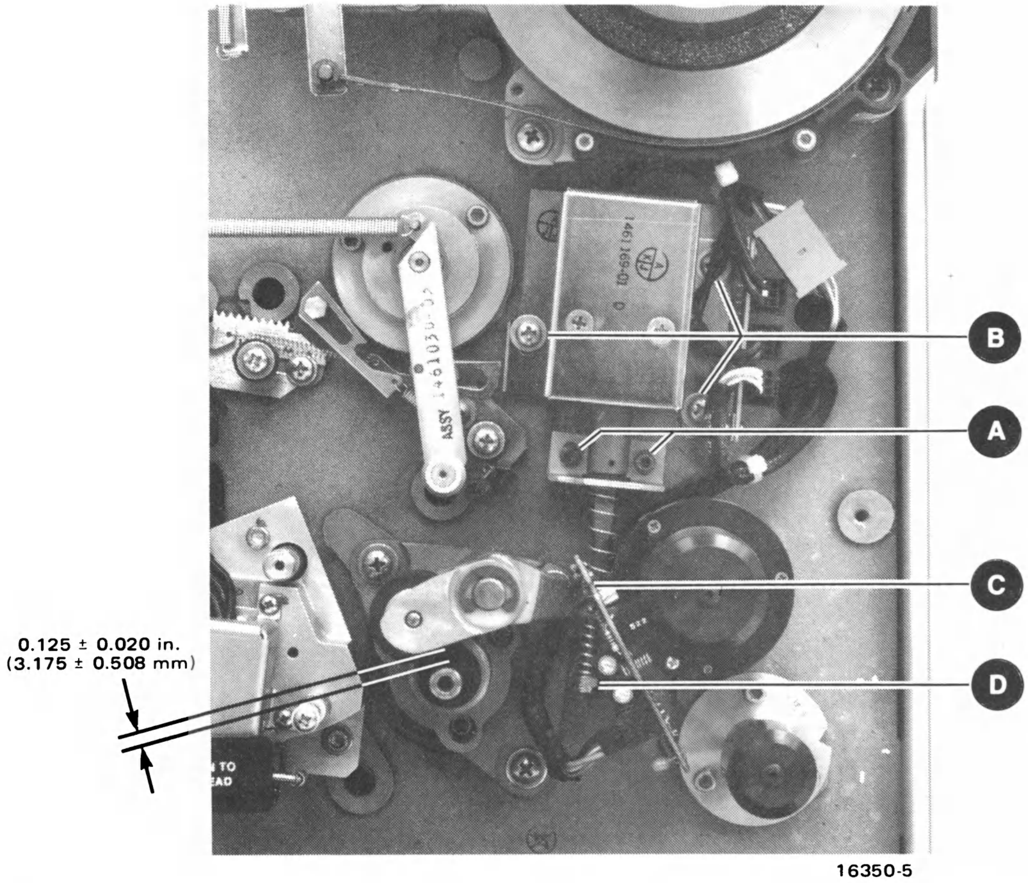


Figure 4-6. Pinch Roller Pressure Adjustment

Note

If a hook, as specified in step 7, is not available, a 4-40 panhead screw can be threaded into the setscrew hole. The nylon cord can then be looped around the panhead screw.

STEP 8 Apply power to VTR. Press PLAY to energize solenoid.

STEP 9 Place point of hook at end of cord loop in the setscrew hole in bottom of pinch roller arm. Hold spring scale upright, as shown in Figure 4-7, to maintain tension on lacing cord.

STEP 10 Maintaining light finger contact on rotating pinch roller, lift spring scale, and observe amount of force required to eliminate pinch-roller-to-capstan contact. The pinch roller will stop rotating when it breaks contact with the capstan. Force required should be 7.00 lb ±0.22 lb (3.2 kg ±0.1 kg).

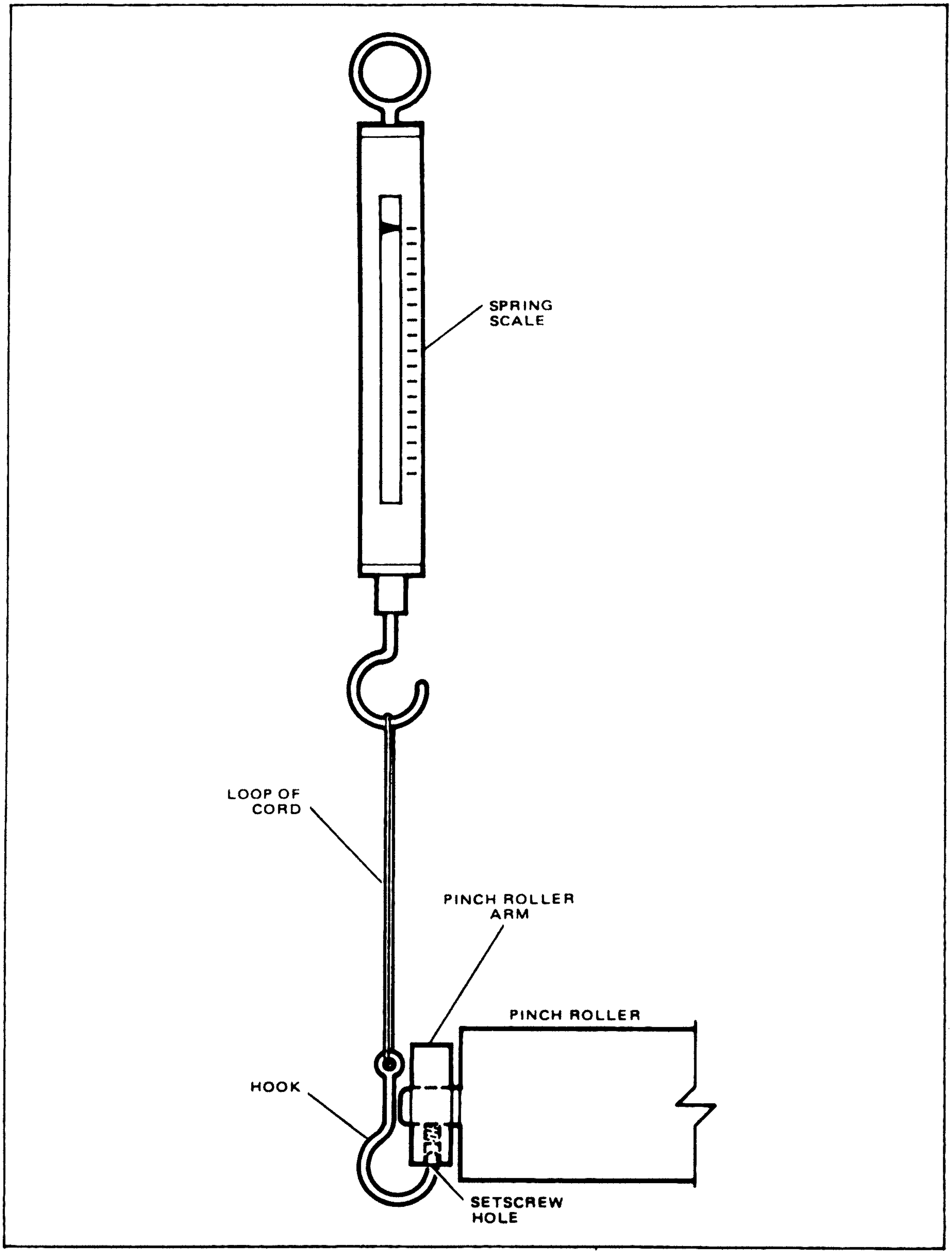


Figure 4-7. Pinch Roller Pressure Measurement

STEP 11 If force needs adjustment, turn solenoid force adjustment locknut (Figure 4-6, D) in small increments (clockwise increases force).

STEP 12 If sufficient force is not attainable, the solenoid is probably not seating fully because locknut is too tight. Turn VTR power off, and loosen locknut until spring is slack and repeat adjustment. Repeat steps 8 through 11, as required.

STEP 13 Press STOP to deenergize solenoid.

STEP 14 Repeat step 3.

STEP 15 Remove light barrier from TIP sensor.

4-23 Tape Tension Adjustments

Note

Before checking or adjusting tape tension, make sure capstan pinch roller pressure is correct. (Refer to paragraph 4-22.)

Note

Tape tension adjustments must be made in the following sequence:

1. **Play mode—see paragraph 4-24**
2. **Reverse shuttle mode—see paragraph 4-25**
3. **Slow forward shuttle mode—see paragraph 4-26**

Tape tension is measured with the Tentelometer gauge (Table 4-4), and the tension arm is adjusted with the tension arm adjustment tool, Ampex Part No. 1461390 (also listed in Table 4-4).

Before starting tape tension checks and tension arm adjustments, remove transport trim as outlined in paragraph 4-12 and check calibration of tape tension gauge.

4-24 Play Mode

STEP 1 Install a reel of prerecorded tape on supply reel hub and thread tape to takeup reel.

STEP 2 Press PLAY. Check tape guiding.

STEP 3 With VTR in play mode, measure tape tension at scanner entrance. Tension should be 4.25 oz ±0.50 oz (120g ±14g). If it is, omit steps 4 through 7, and continue with paragraph 4-25.

STEP 4 Press SHUTTLE, and shuttle enough tape to takeup reel so that tape coming off supply reel does not interfere with insertion of tension arm adjustment tool in hole A. See Figure 4-8.

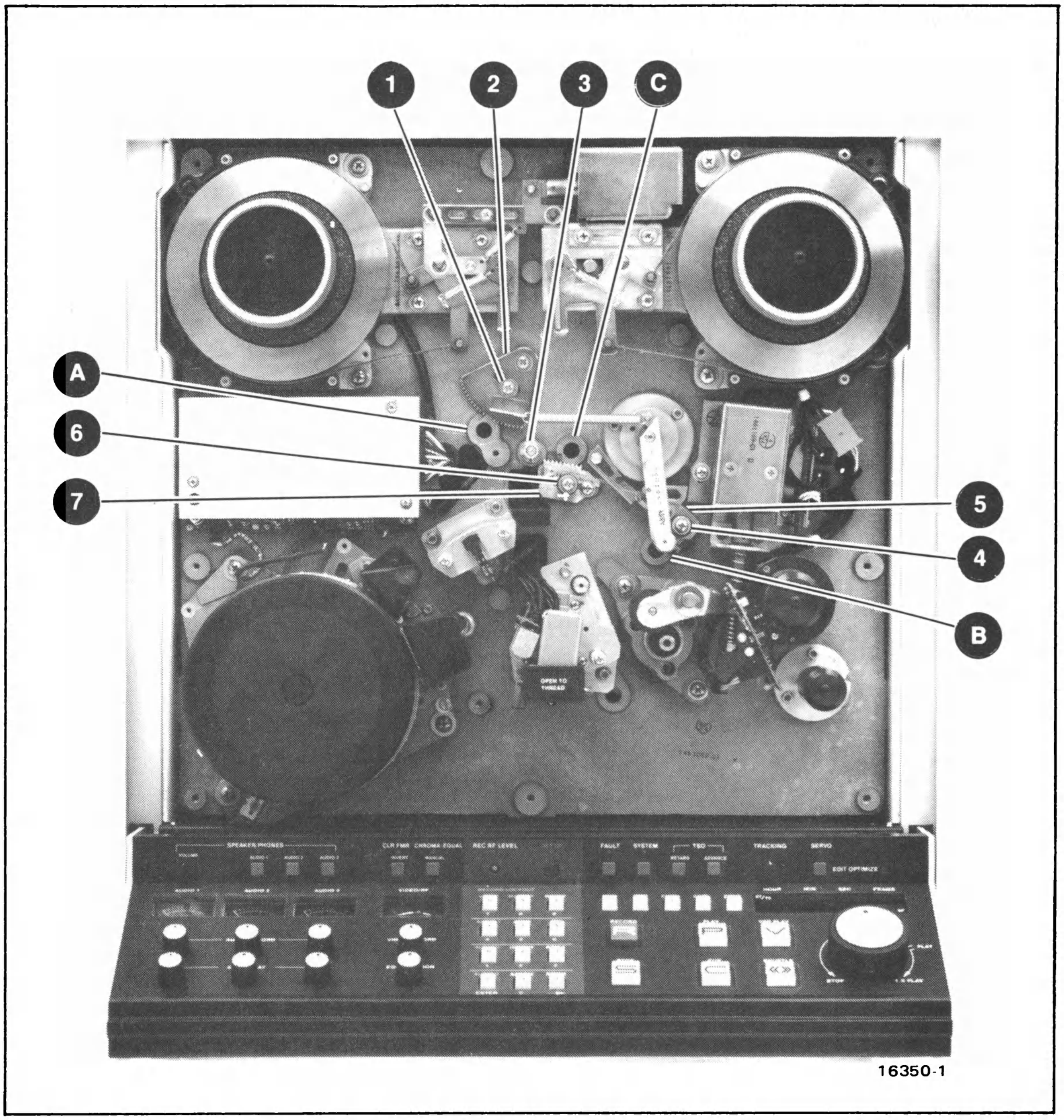


Figure 4-8. Tape Tension Adjustments

Note

If adjustment tool specified in paragraph 4-23 is not available, use a flat blade screwdriver of appropriate width for engaging the teeth on the serrated plate, Figure 4-8 (2). Notch near hole A is the rest and fulcrum for screwdriver blade.

STEP 5 Press button on end of tension arm adjustment tool and insert tool in hole A.

STEP 6 Loosen screw (1) and engage gear on tension arm adjustment tool with teeth on serrated plate (2).

Note

Clockwise rotation of tension arm adjustment tool reduces tape tension, counterclockwise rotation increases tape tension.

STEP 7 Press PLAY, and measure tape tension at scanner entrance while adjusting angular position of serrated plate (2). When tape tension is within tolerance, tighten screw (1), and remove tension arm adjustment tool from hole A.

STEP 8 Verify that takeup tension between turnaround idler and takeup reel is 16.00 oz ±1.00 oz (454g ±28g). If tension is not within tolerance, check reel servo MDA and takeup motor. (See Section 7, Part II of this manual.)

4-25 Reverse Shuttle Mode

STEP 1 With tape threaded on transport, press SHUTTLE and rotate tape speed control full counterclockwise.

STEP 2 With VPR-80 in full speed reverse shuttle mode, measure tape tension between supply reel and guide post (3). Tension should be 14.00 oz ±1.00 oz (397g ±28g). If it is, omit steps 3 through 5, and continue with paragraph 4-26.

STEP 3 Press button on end of tension arm adjustment tool and insert tool in hole B.

STEP 4 Loosen screw (4) and engage gear on tension arm adjustment tool with teeth on serrated plate (5).

Note

Clockwise rotation of tension arm adjustment tool reduces tape tension, counterclockwise rotation increases tape tension.

STEP 5 Press SHUTTLE switch, and measure tape tension between supply reel and guide post (3) while adjusting angular position of serrated plate (5). When tape tension is within tolerance, tighten screw (4), and remove tension arm adjustment tool from hole B.

4-26 Slow Forward Shuttle Mode

The following adjustment is not required on VPR-80s that do not contain the low-tension spring mechanism. Tension is set by software against the main tension spring. If the VPR-80 does contain the low tension spring mechanism as shown in Figure 4-8, continue as follows.

STEP 1 With tape threaded on transport, press SHUTTLE and rotate tape speed control clockwise to shuttle tape forward at rate of 5 to 8 frames per second.

STEP 2 With VPR-80 in slow forward shuttle mode, measure tape tension at scanner entrance. Tension should be 2.00 oz ±0.25 oz (57g ±7g). If it is, omit steps 3 through 5.

STEP 3 Press button on end of tension arm adjustment tool and insert tool in hole C.

STEP 4 Loosen screw (6) and engage gear on tension arm adjustment tool with teeth on serrated plate (7).

Note

Clockwise rotation of the tension arm adjustment tool reduces tape tension, counterclockwise rotation increases tape tension.

STEP 5 Press SHUTTLE switch, and measure tape tension at scanner entrance while adjusting angular position of serrated plate (7). When tape tension is within tolerance, tighten screw (6), and remove tension arm adjustment tool from hole C.

4-27 Noise-Free Interval Test

For video tape recordings to be interchangeable among all Type C, 1-in. helical VTRs, the helical path described by the video head as it scans the tape must be the same on one machine as it is on the next. The helical path is determined primarily by the factory-set helical guide band on the lower scanner, but is also affected by the adjustable entrance and exit guides. These guides determine position and attitude of tape as it begins and ends its wrap around the scanner. Helical alignment is checked by comparing video head tracking to the tracking standard provided on a guide adjustment tape (see Table 4-4 for proper adjustment tape).

One method for analyzing head tracking is to measure the noise-free interval time. This time is the total amount of time the video head can be moved with relation to the control track pulses and not pick up video from either adjacent video track. TRACKING control is used to vary timing, and, when using guide adjustment tape, crossover of the video head into an adjacent track is evidenced by breakup or interference in the picture on the video monitor. To measure the noise-free interval time, proceed as follows:

STEP 1 Remove transport trim as outlined in paragraph 4-12, and clean scanner, heads, guides, and capstan as described under paragraph 4-14. Demagnetize all tape path components.

STEP 2 Thread appropriate guide adjustment tape (Table 4-4) on transport.

STEP 3 Verify that AUTO, INSERT, and ASSEM indicators are not lighted.

STEP 4 Hold RECORD switch down, and press MASTER RECORD LOCKOUT switch: red indicator should be lighted.

STEP 5 On Control PWA, set REF SELECT switch 6S5 to INPUT.

STEP 6 On AST Servo PWA, set AST ON/OFF switch 4S3 to OFF.

STEP 7 Connect scope probe to TP17 (INPUT RF) on Mod/Demod PWA, and trigger scope on TP5 (CT PLAY) on Servo PWA.

STEP 8 Press PLAY, and adjust TRACKING control (on secondary control panel) for best video picture.

Note

SYSTEM indication 01 may be displayed when play mode is entered. It is not significant to this adjustment. Simply press SYSTEM to clear indication, and continue.

STEP 9 Adjust scope to display rf envelope for one field (Figure 4-9).

STEP 10 Turn TRACKING control until picture on monitor just begins to deteriorate. Return control to borderline area where picture looks good.

STEP 11 Adjust scope so that edge of rf presentation is at a convenient reference point with respect to scope graticule.

STEP 12 Turn TRACKING control in opposite direction to that of step 10 until picture again begins to deteriorate. Return control to borderline area where picture looks good.

STEP 13 Measure displacement (time shift) of rf envelope on scope to determine noise-free interval time. Time should be at least 8.0 ms.

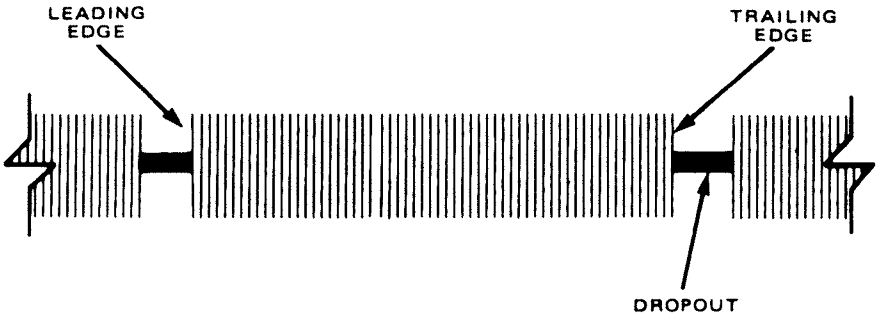


Figure 4-9. Ideal Interchange RF Envelope

STEP 14 Observe that when TRACKING control is turned from maximum rf position, rf envelope shows uniform collapse. Breathing, undulations, and fluctuations in rf envelope should be no more than 10% of envelope amplitude.

If noise-free interval and rf envelope appear as described in steps 13 and 14, omit paragraph 4-28 and proceed with paragraph 4-29. Otherwise, continue with paragraph 4-28.

4-28 Track Straightness Adjustment

This adjustment procedure optimizes symmetry of the rf envelope. Track straightness is indicated when the envelope is as rectangular as possible and when breathing, undulations, and fluctuations do not exceed 10% of envelope amplitude.

Adjustments A and B (shown in Figure 4-10) adjust angle of guide pins, and adjustments C and D set guide pin height. The entrance guide pin is tapered, whereas the exit guide pin is straight. Figure 4-11 shows an ideal rf envelope with adjustments A and B correctly set, as well as the appearance of the envelope with adjustment A incorrectly set.

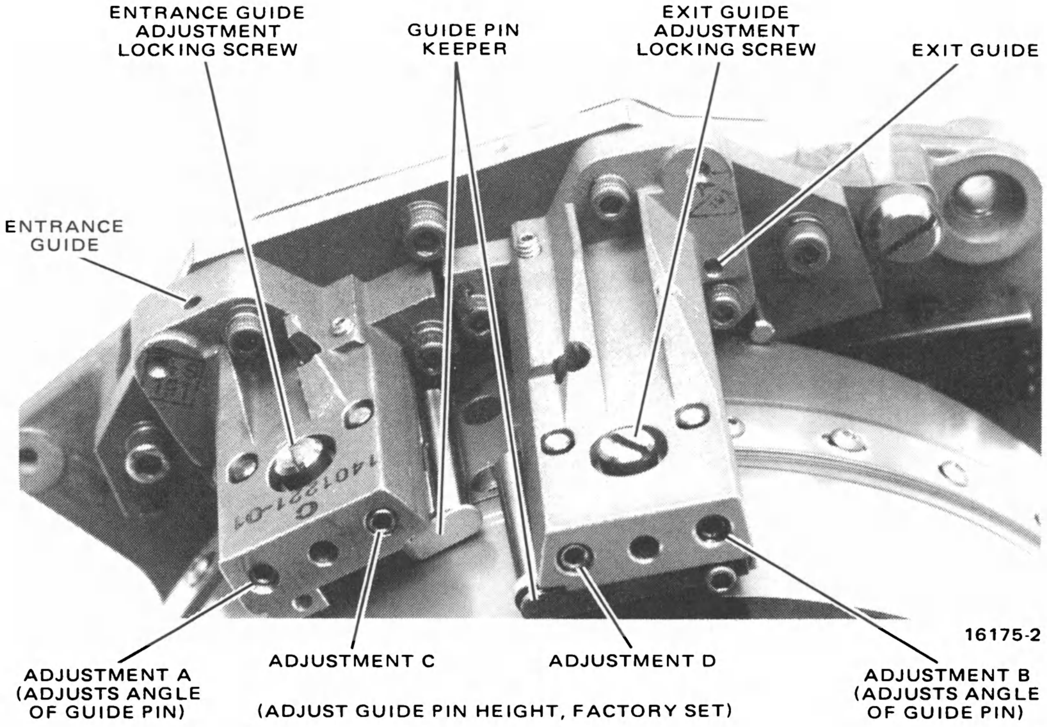

ENTRANCE GUIDE ADJUSTMENT LOCKING SCREW
GUIDE PIN KEEPER
EXIT GUIDE ADJUSTMENT LOCKING SCREW
EXIT GUIDE
ENTRANCE GUIDE
16175-2
ADJUSTMENT A (ADJUSTS ANGLE OF GUIDE PIN)
ADJUSTMENT C
ADJUSTMENT D
(ADJUST GUIDE PIN HEIGHT, FACTORY SET)
ADJUSTMENT B (ADJUSTS ANGLE OF GUIDE PIN)

Figure 4-10. Scanner Entrance and Exit Guide Adjustment Screws

Adjustment screws designated C and D are factory set to provide approximately a 0.005-in. (0.1270-mm) clearance between tape and keeper, and should not require readjustment following minor adjustment of screw A.

The upper keeper should not contact upper tape edge in normal operating modes and is present only to prevent tape damage, particularly during tape unthreading. To adjust entrance and exit guide pins, proceed as follows:

STEP 1 Remove transport trim as outlined in paragraph 4-12, and thread appropriate guide adjustment tape (Table 4-4) on the transport.

STEP 2 Verify that AUTO, INSERT, and ASSEM indicators are not lighted.

STEP 3 Press MASTER RECORD LOCKOUT; red indicator should be lighted.

STEP 4 On Control PWA, set REF SELECT switch 6S5 to INPUT.

STEP 5 On Servo PWA, set SCANNER PHASE switch 5S1 (8-section DIP switch) to all zeros (open).

STEP 6 On AST Servo PWA, set AST ON/OFF switch 4S3 to OFF.

STEP 7 Remove scanner entrance and exit guide covers (one screw secures each cover).

STEP 8 Connect scope probe to 1TP31 on Mod/Demod PWA, and trigger scope on 4TP6 (TAPE HORIZ) on AST Servo PWA.

STEP 9 Press PLAY and adjust scope for 50 mV/cm and 5 µs/cm.

Note

SYSTEM indication 01 may be displayed when play mode is entered. It is not significant to this adjustment. Simply press SYSTEM to clear indication, and continue.

STEP 10 Loosen entrance guide adjustment locking screw and exit guide adjustment locking screw (Figure 4-10) one-quarter turn counterclockwise.

STEP 11 Slowly rotate TRACKING control back and forth to check that leading and trailing edges of rf envelope rise and fall at same amplitude. Adjust tilt angle of entrance and exit guide pins (adjustments A and B in Figure 4-11) for maximum output and flatness at leading and trailing edges of rf envelope, as shown in Figure 4-11. Repeat this step as required.

STEP 12 While in play mode, observe that there is approximately 0.005-in. (5-mil, or 0.1270-mm) clearance between upper edge of tape and keeper on entrance guide. Adjust screw C, if required. On exit guide, tape should be lifting ceramic guide 0.002 in. to 0.004 in. (0.0508 mm to 0.1016 mm). If not, adjust screw D.

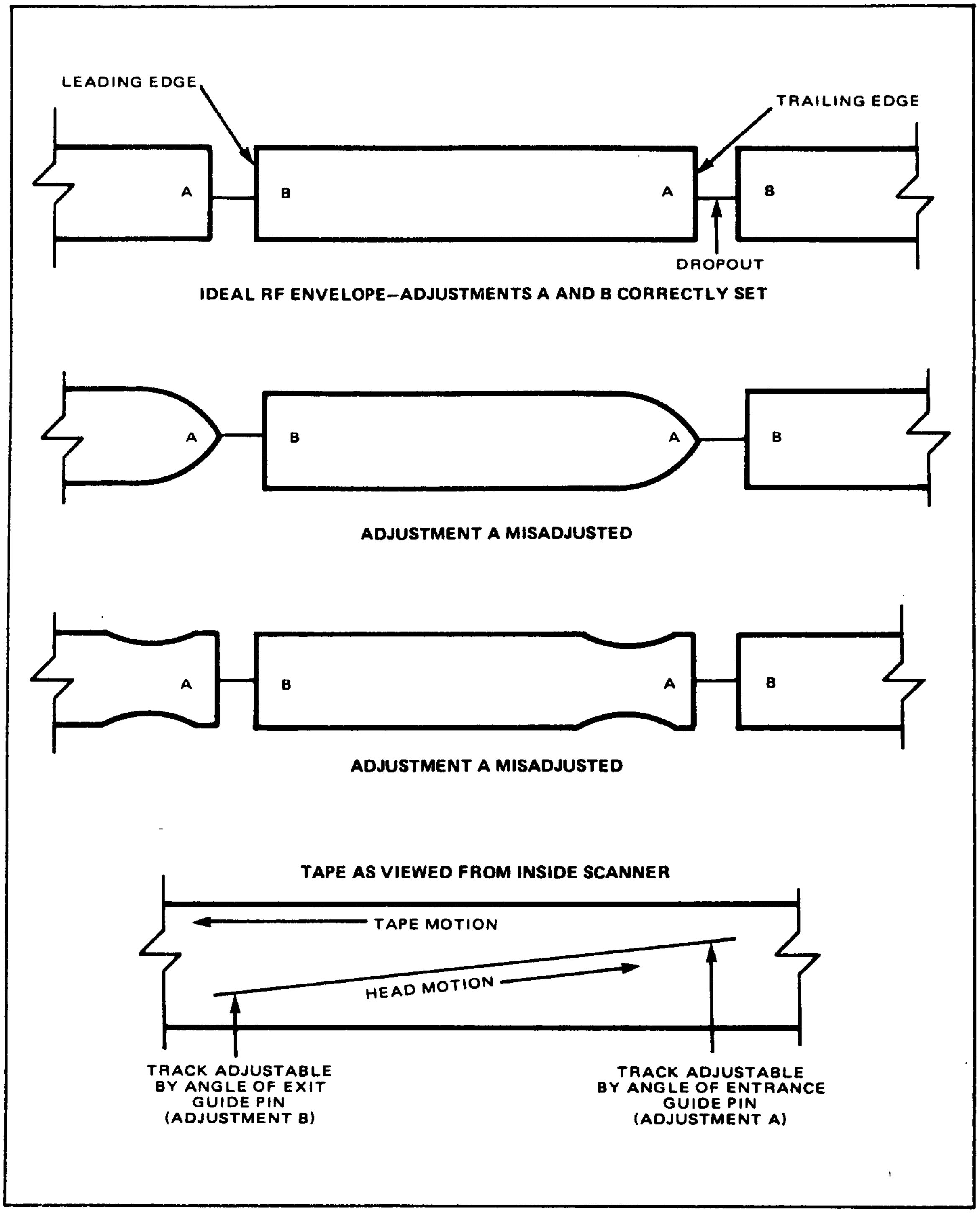

LEADING EDGE
TRAILING EDGE
A
B
A
B
DROPOUT
IDEAL RF ENVELOPE–ADJUSTMENTS A AND B CORRECTLY SET
A
B
A
B
ADJUSTMENT A MISADJUSTED
A
B
A
B
ADJUSTMENT A MISADJUSTED
TAPE AS VIEWED FROM INSIDE SCANNER
TAPE MOTION
HEAD MOTION
TRACK ADJUSTABLE BY ANGLE OF EXIT GUIDE PIN (ADJUSTMENT B)
TRACK ADJUSTABLE BY ANGLE OF ENTRANCE GUIDE PIN (ADJUSTMENT A)

Figure 4-11. Effects of Scanner Entrance and Exit Guide Adjustments

Note

If screws C and D are adjusted, step 11 must be repeated.

STEP 13 Tighten entrance and exit guide adjustment locking screws loosened in step 10, and repeat step 11 to ensure that adjustment has not changed after tightening screws.

STEP 14 Repeat test in paragraph 4-27.

STEP 15 Reinstall exit and entrance guide covers removed in step 7.

4-29 Scanner Tach Adjustment

The position of the scanner tach determines the height of video track recordings. This position has been set at the factory and should not require adjustment. However, if the scanner has been disassembled or if the VTR is making recordings with errors in dropout position, then tach position should be verified before making further adjustments. Proceed as follows:

STEP 1 Remove transport trim as outlined in paragraph 4-12, and thread appropriate guide adjustment tape (Table 4-5) on transport.

STEP 2 Verify that AUTO, INSERT, and ASSEM indicators are not lighted.

STEP 3 Press MASTER RECORD LOCKOUT; red indicator should be lighted.

STEP 4 Press EE; indicator should be lighted.

STEP 5 On Servo PWA, set SCANNER PHASE switch 5S1 (8-section DIP switch) to all zeros (open).

STEP 6 On Control PWA, set REF SELECT switch 6S5 to INPUT.

STEP 7 On AST Servo PWA, set AST ON/OFF switch 4S3 to OFF.

STEP 8 Press PLAY, and carefully adjust TRACKING control for absolute peak indication on VIDEO/RF meter.

Note

SYSTEM indication 01 may be displayed when play mode is entered. It is not significant to this adjustment. Simply press SYSTEM to clear the indication, and continue.

Note

Great care must be taken to determine absolute peak reading on rf meter. Improper adjustment of tracking can introduce reading errors in excess of measurement tolerances. It is recommended that measurement be performed two or more times to verify repeatability.

STEP 9 Press STOP, and press READY to stop scanner motor.

STEP 10 Connect scope channel A probe to 2TP1 (SELECTED VIDEO), and connect scope channel B probe to 1TP30 (DEMOD OUT). Trigger scope on 2TP27 (REF FRAME) so that an entire field can be seen.

STEP 11 Press READY to start scanner; then press PLAY.

STEP 12 Expand scope sweep to observe vertical sync area. Adjust scope channel A (SELECTED VIDEO) so sync coincides with a convenient graticule line on scope.

Note

Ensure that fields displayed on scope channels A and B are the same field by comparing last line of the field.

STEP 13 Observe that playback vertical sync (DEMOD OUT, observed on scope channel B) coincides with EE vertical sync (SELECTED VIDEO, observed on scope channel A) within ±15.0 µs.

STEP 14 If the coincidence is within ±15.0 µs, no adjustment is necessary. If coincidence is not within ±15.0 µs, loosen serrated lever holddown screw shown in Figure 4-12.

STEP 15 Use a screwdriver to adjust position of serrated lever, and adjust timing of the scanner tach so that playback vertical sync coincides with EE vertical sync within ±5 (five) µs.

STEP 16 Tighten serrated lever holddown screw to preserve coincidence of vertical sync observed on scope channels A and B.

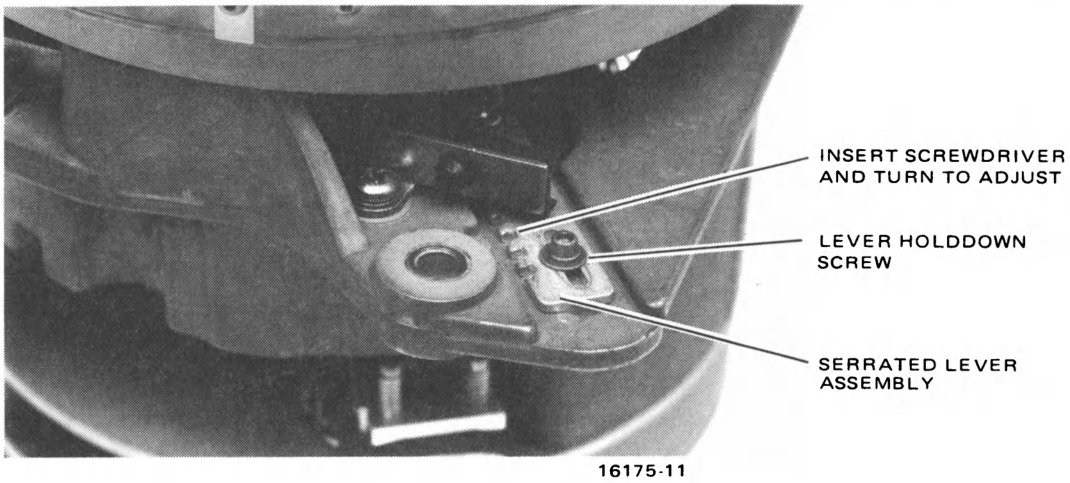


Figure 4-12. Scanner Tach Adjustment

4-30 Helical Scan Dropout

Helical scan dropout begins when the rotating video record/playback head leaves the tape near the scanner entrance guide and ends as the head begins its scan on tape just past the exit guide. Duration of the dropout is factory-set (by placement of the guides on the scanner guide block) to be nominally 10 horizontal lines wide (635 µs) for 525-line systems, or 12.5 horizontal lines wide (800 µs) for 625-line systems. Dropout duration increases with head wear, which causes shifting of the dropout position with respect to the vertical blanking interval. Lateral positioning of the guide block is provided to allow adjustment of the beginning of dropout relative to the leading edge of the third or fourth vertical sync broad pulse. Table 4-7 shows timing relationships of the dropout duration and position with respect to the third broad pulse and line 15 for 525-line systems as a function of tip projection. Table 4-8 shows corresponding data with respect to the fourth broad pulse and line 15 for 625-line systems.

Table 4-7. Dropout Duration and Position Vs. Head Tip Projection (525-Line Systems)

Tip Projection (mils)	Dropout Duration (± 10 µs)	X End of DO After Leading Edge of 3rd Broad Pulse (± 3 µs)	X End of DO Before Leading Edge of Line 15 (± 13 µs)
3.0	617	3.0	15.0
3.1	614	3.5	17.5
3.2	612	4.0	19.0
3.3	609	5.0	21.0
3.4	606	5.5	23.5
3.5	604	6.0	25.0

Table 4-8. Dropout Duration and Position Vs. Head Tip Projection (625-Line Systems)

Tip Projection (mils) (1 mil-0.0254 mm)	Dropout Duration (± 10 µs)	X End of DO After Leading Edge of 4th Broad Pulse (± 3 µs)	X End of DO Before Leading Edge of Line 15 (± 13 µs)
3.0	740	22.6	37.4
3.1	736	23.2	40.8
3.2	733	23.8	43.2
3.3	730	24.4	45.6
3.4	726	25.0	49.0
3.5	724	25.6	50.4

4-31 525-Line Systems

In 525-line systems, the interval from the leading edge of the third broad pulse to the leading edge of line 15 is 10 lines, or 635 μs. Dropout duration (in microseconds) conforms to the equation:

$$D = 635 - (X + Y)$$

where (as shown in Figure 4-13):

D = Dropout duration

X = Time from leading edge of third broad pulse to start of dropout

Y = Time from end of dropout to leading edge of line 15

Terms X and Y are functions of head wear. Both X and Y decrease as head tip projection decreases, and thus the dropout interval increases. For example, as seen in Table 4-7, a head tip projection of 3.3 mils produces a dropout duration of 609 μs:

$$609 = 635 - (5 + 21)$$

The start and end of the dropout are measured at the 50% point of full rf amplitude. Dropout duration and position tolerances are shown in Table 4-7.

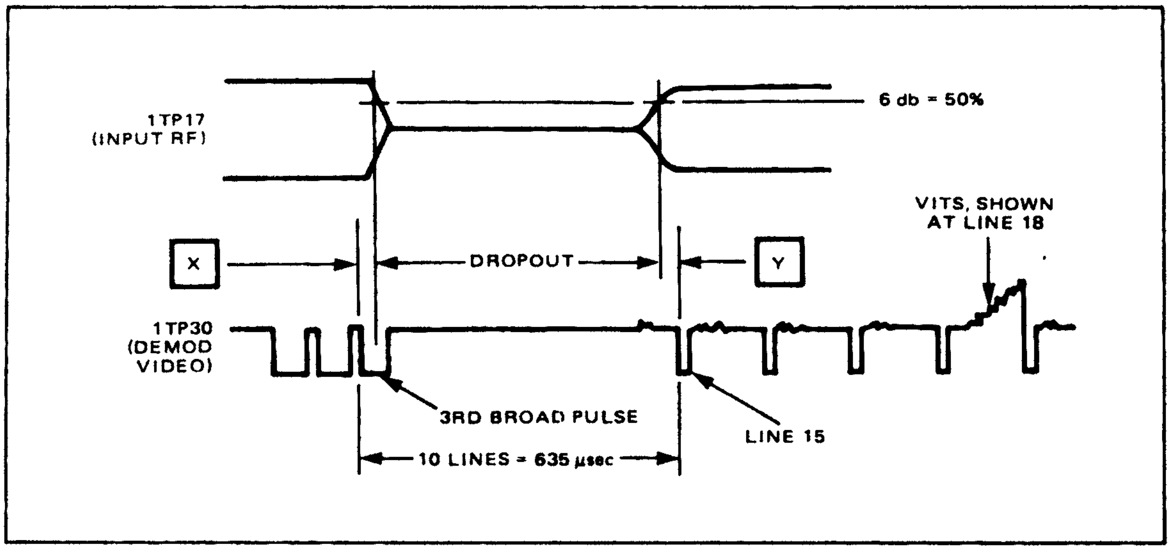


Figure 4-13. Dropout Duration and Position (525-Line Systems)

4-32 625-Line Systems

In 625-line systems, the interval from the leading edge of the fourth broad pulse to the leading edge of line 15 is 12.5 lines, or 800 μs. Dropout duration (in microseconds) conforms to the equation:

$$D = 800 - (X + Y)$$

where (as shown in Figure 4-14):

D = Dropout duration

X = Time from leading edge of fourth broad pulse to start of dropout

Y = Time from end of dropout to leading edge of line 15

Terms X and Y are functions of head wear. Both X and Y decrease as head tip projection decreases, and thus the dropout interval increases. For example, as seen in Table 4-8, a head tip projection of 3.3 mils produces a dropout duration of 730 µs.

$$730 = 800 - (24.4 + 45.6)$$

Start and end of the dropout are measured at the 50% point of full rf amplitude. Dropout duration and position tolerances are shown in Table 4-8.

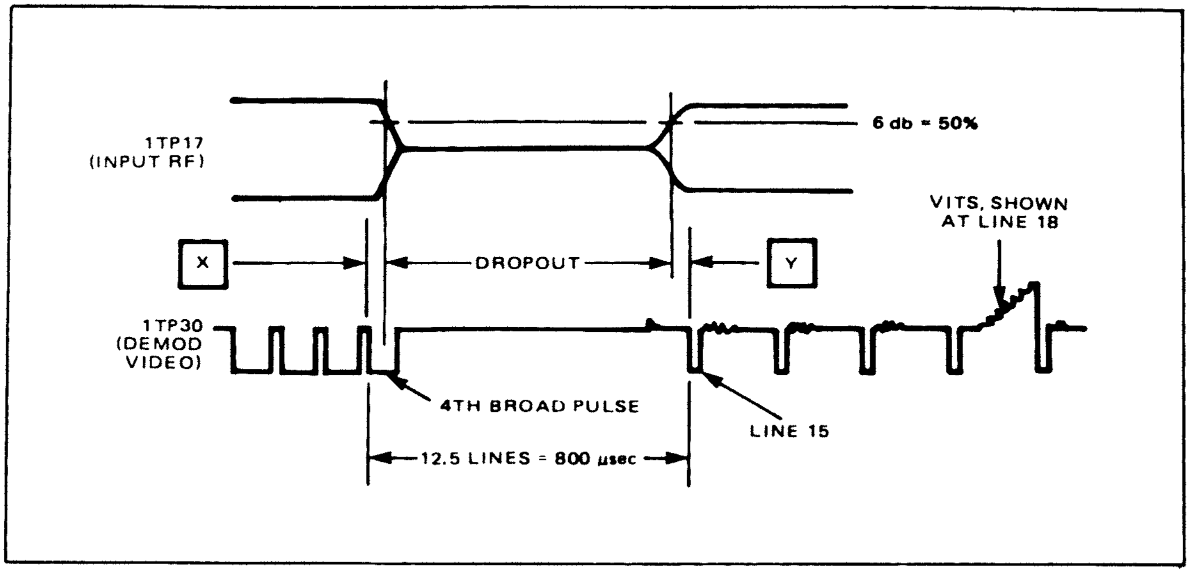


Figure 4-14. Dropout Duration and Position (625-Line Systems)

4-33 Head Tip Projection Measurement

Head tip projection is measured with the tip projection gauge listed in Table 4-4. The gauge is mounted on the scanner as shown in Figure 4-15.

CAUTION

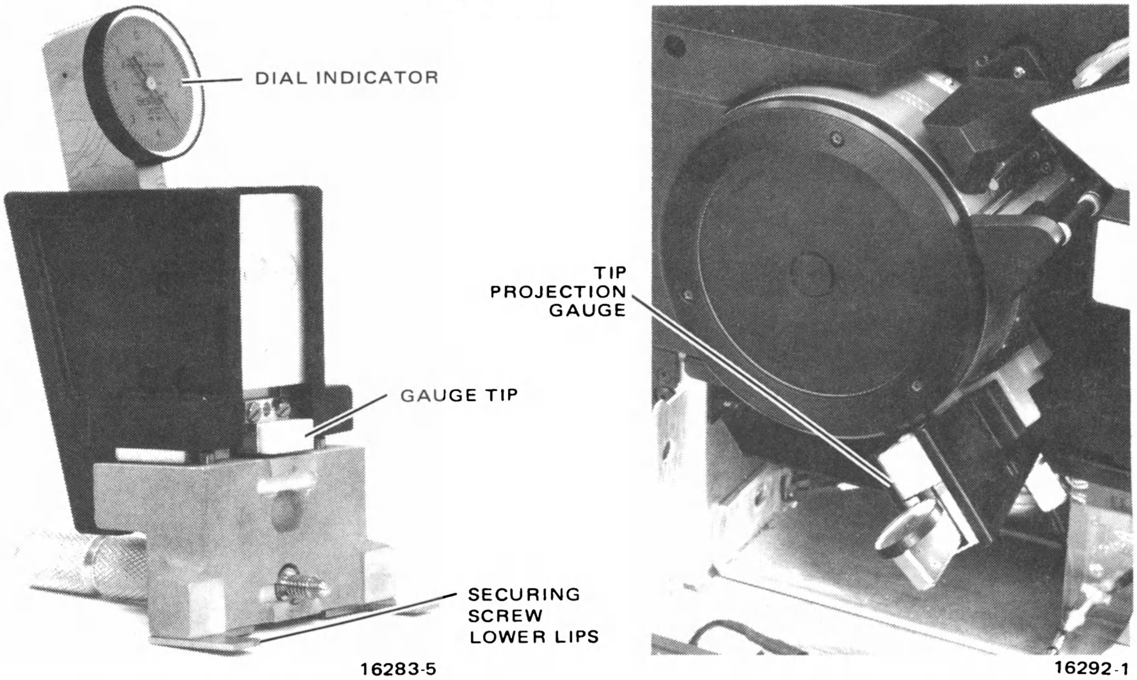
TURN VPR-80 POWER OFF BEFORE MEASURING HEAD TIP PROJECTION.

Measure head tip projection as follows:

STEP 1 With power off, open hinged transport cover.

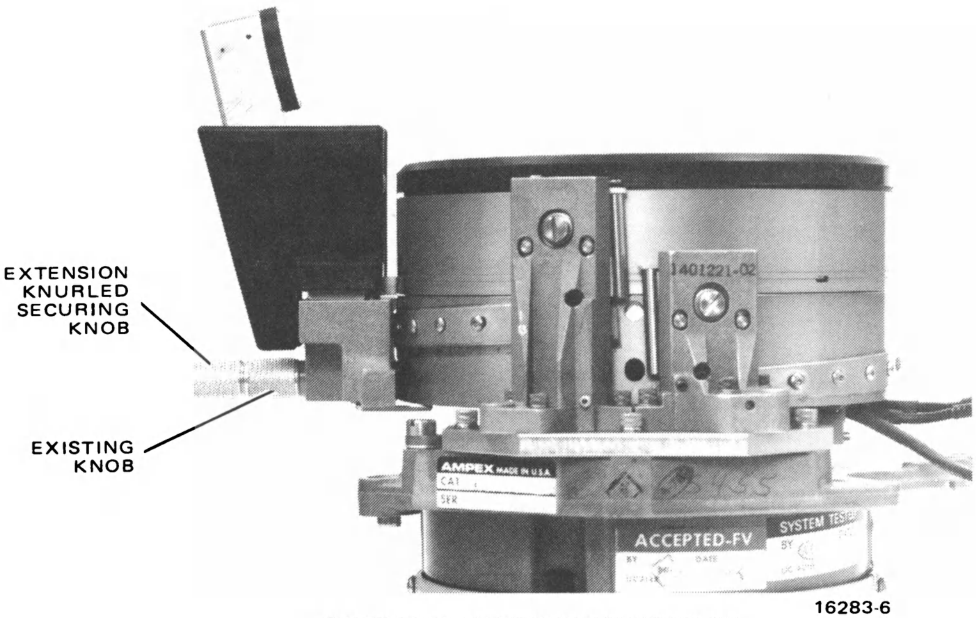
STEP 2 Remove two no. 10 cross-recessed screws (one on each side of control panel assembly), and pivot control panel assembly forward.

STEP 3 To ensure accurate readings, clean video record/play and edit erase heads, and scanner drum surface as outlined in paragraph 4-17 using Ampex head cleaner or xylene. Clean gauge tip with isopropyl alcohol.



TIP PROJECTION GAUGE

TIP PROJECTION GAUGE MOUNTED ON SCANNER



TIP PROJECTION GAUGE MOUNTED ON SCANNER REMOVED FROM TRANSPORT

Figure 4-15. Head Tip Projection Measurement

STEP 4 Attach knurled extension knob (Ampex Part No. 1463353) to knob on gauge as follows. Remove socket-head setscrew from center of extension knob. Use this screw to secure extension knob to existing knob on the gauge.

CAUTION

TIP OF GAUGE MUST NOT STRIKE ANY SCANNER HEAD DURING GAUGE INSTALLATION, AS DAMAGE COULD BE DONE TO THE HEAD. POSITION SCANNER DRUM SO THAT NO HEAD CONTACT IS MADE. ALSO, ALWAYS ROTATE SCANNER DRUM SLOWLY WHEN GAUGE IS INSTALLED.

STEP 5 Gauge is held to stationary scanner drum by a screw which is rotated by the knurled knob on the gauge. See Figure 4-15. With scanner positioned so that no head will be contacted, place gauge so that the two lower lips of gauge contact bottom surface of stationary scanner drum, and turn knob finger tight to secure gauge.

STEP 6 With gauge tip approximately 0.5 in. (13 mm) to the left of video record/play head, rotate gauge outer ring to zero the gauge.

STEP 7 Rotate scanner drum slowly clockwise to place head under gauge tip so that scanner head tip projection can be measured. Record the measurement.

Note

Gauge indicates tip projection in mils. Each small increment equals 0.1 mil (1 mil = 0.0254 mm).

STEP 8 Repeat steps 6 and 7 to measure erase head tip projection.

STEP 9 Turn scanner drum so that gauge tip is clear of scanner heads, and remove gauge.

STEP 10 Again clean heads, scanner surface, and gauge tip with appropriate cleaner.

STEP 11 Remove extension knob, and return gauge to its protective container.

STEP 12 Raise control panel assembly to operating position and secure with screws removed in step 2.

4-34 Pin-to-Scanner Gap Measurement

The gap between scanner and pins of the entrance and exit guides is critical. This gap affects duration of the dropout. For this reason, the pin-to-scanner gap for both guides should be measured, and adjusted, if necessary, before making dropout duration and position measurements (paragraph 4-36).

The pin-to-scanner gap procedure requires use of either precision plastic shim stock of 10-mil and 12-mil thickness, or a precision plastic feeler gauge. Prepare a gauge to measure pin-to-scanner gap. If precision plastic shim stock is to be used, it must be cut to a suitable size and shape. For ease of handling, stock material (both 10-mil and 12-mil) can be cut into a wedge 3 inches long, the wedge being 1/2 inch at the wide end, and 1/4 inch at the narrow end, with the narrow end rounded. A precision plastic feeler gauge can be used (instead) if available. Do not use a metal feeler gauge or other metal device in scanner/head area.

The procedure which follows applies to both entrance and exit guides.

STEP 1 Remove transport trim as outlined in paragraph 4-12. Also remove scanner entrance and exit guide covers.

STEP 2 Turn scanner so no head is near entrance/exit guides before proceeding (all heads are clear).

CAUTION

DELICATE SCANNER HEADS MUST BE CLEAR OF ENTRANCE/EXIT GUIDES BEFORE ATTEMPTING PIN-TO-SCANNER MEASUREMENT. OTHERWISE, HEAD DAMAGE CAN RESULT. TURN SCANNER AS REQUIRED.

STEP 3 Insert 10-mil precision plastic stock (or plastic gauge) into gap where video record/play head passes guide pin (see Figure 4-16). Insert narrow end first, and from outboard side, not from in-between pins. Measurement is valid only where head passes. The 10-mil stock (or gauge) should penetrate gap with little or no clearance. The gap between the record/play head path and guide pin should be 9 to 12 mils (1 mil = 0.0254 mm). A gap of 11 mils (0.2794 mm) is ideal.

STEP 4 Repeat step 3, using piece of 12-mil stock (or gauge). The 12-mil piece should not penetrate gap.

STEP 5 If pin-to-scanner gap for both guides is correct, proceed to step 6. If gap needs adjustment, continue with pin-to-scanner gap adjustment procedure, paragraph 4-35.

STEP 6 Turn scanner so record/play head is at 12 o'clock position. Replace guide covers, and continue with dropout duration and position measurements (paragraph 4-36).

4-35 Pin-to-Scanner Gap Adjustment

If the gap for either guide is too great or too small, it must be adjusted. Adjust gap, then remeasure to verify that adjusted gap is correct. This procedure applies to both entrance and exit guides.

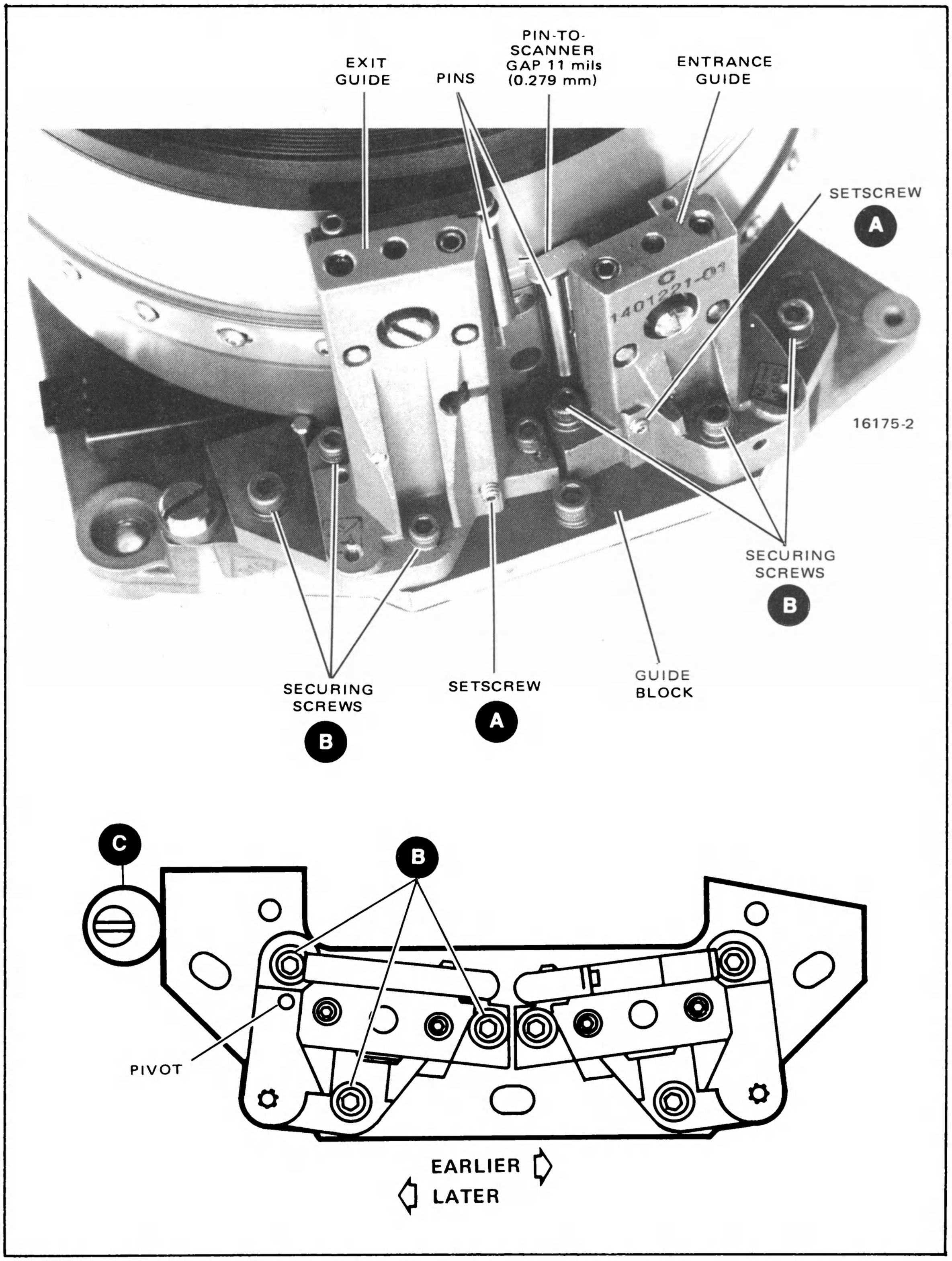


Figure 4-16. Pin-to-Scanner Gap Adjustment

STEP 1 Clean guide block in area around base of both guides (Figure 4-16), using isopropyl alcohol and a cotton swab. This removes dirt which may get under guide when moved and cause misalignment.

STEP 2 Turn hex-recessed setscrew (A in Figure 4-16) clockwise until it just contacts base of scanner. Do not tighten or torque down.

STEP 3 Loosen three screws (B) securing guide to guide block.

STEP 4 The guide may tend to be frozen into its position. To unseat guide, back out setscrew (A) about one turn, then press guide in at base and observe that it moves in. (Note that it pivots on dowel pressed into guide block.) Now that guide moves freely, tighten setscrew about one turn to restore guide to original gap value (approximately).

STEP 5 Turn setscrew (A) clockwise slightly to increase gap; turn counterclockwise slightly to decrease gap. Press in guide gently at base so setscrew tip contacts scanner.

STEP 6 While holding guide in at base, snug three securing screws (B) down gently. Before tightening screws, check gap with plastic shim stock (or plastic gauge) to see that it is close to proper gap measurement (gap may change when screws are tightened). Loosen screws and readjust as necessary. When gap is correct, tighten screws little by little—going from one to the other, until they are all tight and secure. Recheck gap; if incorrect, loosen securing screws and repeat steps 5 and 6.

STEP 7 When adjustment is complete, back out setscrew about two turns so it is clear of scanner. This prevents it from digging in should guide block itself be moved or adjusted.

STEP 8 Reinstall guide cover.

4-36 Dropout Duration and Position Measurements

After verifying compliance of pin-to-scanner gap measurements to specification in paragraph 4-34, dropout duration can be assumed to be within ±10 µs of the duration figure in Table 4-7 or 4-8 which is determined by head tip projection. Measure dropout duration and position as follows:

STEP 1 Remove transport trim as outlined in paragraph 4-12, and thread a work tape on the transport.

STEP 2 Make a short recording, and rewind tape.

STEP 3 Verify that AUTO, INSERT, and ASSEM indicators are not lighted.

STEP 4 Press MASTER RECORD LOCKOUT; red indicator should be lighted.

STEP 5 Press EE; indicator should be lighted.

STEP 6 On Servo PWA, set SCANNER PHASE switch 5S1 (8-section DIP switch) to all zeros (open).

STEP 7 On Control PWA, set REF SELECT switch 6S5 to INPUT.

STEP 8 On AST Servo PWA, set AST ON/OFF switch 4S3 to OFF.

STEP 9 Connect scope channel A probe to 1TP17 (INPUT RF), and connect connect scope channel B probe to 1TP30 (DEMOD OUT).

STEP 10 Press PLAY, and trigger scope so that an entire field can be seen.

Note

SYSTEM indication 01 may be displayed when play mode is entered. It is not significant to this measurement. Simply press SYSTEM to clear the indication, and continue.

STEP 11 Set scope for expanded sweep to view vertical blanking area. Dropout duration is that period of time in which rf amplitude is 50% or less (6 dB down) from normal rf amplitude as shown in Figure 4-13 or 4-14. Measure and record dropout position with respect to nominal position defined in Table 4-7 or 4-8 for measured head tip projection (paragraph 4-33).

When guide adjustment tapes are recorded by Ampex, great care is exercised in physically measuring exactly where video is laid down on the tape. Line 26 has been specifically measured with respect to its distance from the tape edge, and thus provides the most accurate position reference. Therefore, when measuring and adjusting tape position, lines 15 through 26 which appear after vertical interval are benchmarks for tape position.

You can tell if line 15 is the pulse which appears at the end of the rf dropout by measuring dropout duration and its beginning in relation to the leading edge of the third (or fourth) broad pulse.

If dropout position exceeds tolerances given in Table 4-7 or 4-8, proceed with dropout position adjustment outlined in paragraph 4-37.

4-37 Dropout Position Adjustment

To adjust position of dropout, proceed as follows:

CAUTION

MAKE ALL MECHANICAL ADJUSTMENTS WHEN POWER IS OFF AND SCANNER IS NOT ROTATING. OTHERWISE, DAMAGE TO HEADS CAN OCCUR.

STEP 1 Remove transport trim as outlined in paragraph 4-12.

STEP 2 Determine from measurement procedure (paragraph 4-36) the amount of dropout position error, and whether dropout appears early or late. If dropout is early (less than 3 µs), guide block must be moved to the left (as shown in Figure 4-16). If dropout is late (in excess of 13 µs) guide block must be moved to the right. One mil of guide block movement is equal to 1 µs (1 mil = 0.0254 mm).

Note

The eccentric stop (C in Figures 4-16 and 4-17) is used as reference to adjust guide block position. After adjustment, it allows guide block to be removed and reinstalled without dropout position readjustment.

If dropout is early, continue with steps 3, 4, 5, 9, 10, and 11.

STEP 3 Loosen screw that secures eccentric stop, and use feeler gauge to set spacing in mils (1 mil = 1 µs) between eccentric stop and guide block. Tighten eccentric stop screw.

STEP 4 Loosen three screws (Figure 4-17) securing guide block to scanner casting.

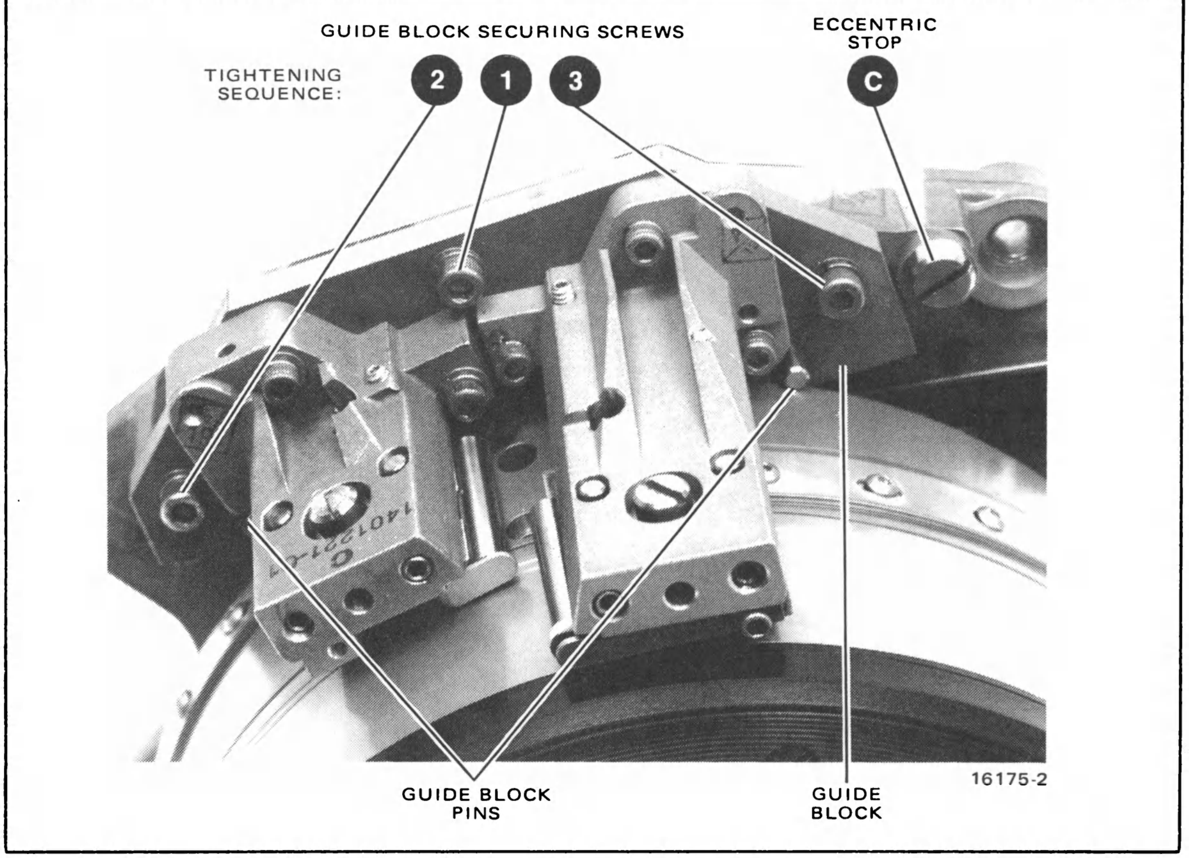


Figure 4-17. Dropout Position Adjustment

STEP 5 Slide guide block to left (as shown in Figure 4-16) so that guide block edge is pressed against eccentric stop and guide block locating pins are resting against lower scanner. Tighten three screws according to tightening sequence noted in Figure 4-17. Do not fully tighten any one screw on first pass. It is recommended that three tightening passes be made before full torque is applied.

If dropout is late, follow steps 6 through 11.

STEP 6 Loosen three screws (Figure 4-17) securing guide block to scanner casting. Slide guide block to the right (as shown in Figure 4-16), and using feeler gauge, set spacing between eccentric stop and guide block.

STEP 7 While maintaining spacing set in step 6, press guide block locating pins against lower scanner and tighten three screws according to tightening sequence noted in Figure 4-17. Do not fully tighten any one screw on first pass. It is recommended that three tightening passes be made before full torque is applied.

STEP 8 Loosen screw that secures eccentric stop, and rotate eccentric stop against guide block. Tighten eccentric stop screw.

STEP 9 Make new recording and determine dropout position while playing it back. Repeat adjustment procedure, and make a new recording each time until dropout position error is within tolerances stated in step 2. Verify dropout duration on each recording to be certain guide block pins are properly resting against scanner surface.

STEP 10 Repeat track straightness adjustment, paragraph 4-28.

STEP 11 Repeat dropout duration and position measurements, paragraph 4-36.

When dropout duration and position are within tolerances stated in Table 4-7 or 4-8, continue with control track position adjustment, paragraph 4-38.

4-38 Control Track Position Adjustment

This is the final adjustment of the series of interchange adjustment procedures. Due to the interactive nature of the interchange adjustments, control track position cannot be adjusted with meaningful results unless it is done last.

Adjust control track position as follows:

STEP 1 Remove transport trim as outlined in paragraph 4-12, and thread appropriate guide adjustment tape (Table 4-5) on transport.

STEP 2 Verify that AUTO, INSERT, and ASSEM indicators are not lighted.

STEP 3 Press MASTER RECORD LOCKOUT; red indicator should be lighted.

STEP 4 Press EE; indicator should be lighted.

STEP 5 On Servo PWA, set SCANNER PHASE switch 5S1 (8-section DIP switch) to all zeros (open).

STEP 6 On Control PWA, set REF SELECT switch 6S5 to INPUT.

STEP 7 On AST Servo PWA, set AST ON/OFF switch 4S3 to OFF.

STEP 8 Connect scope channel A probe to 2TP1 (SELECTED VIDEO), and connect scope channel B probe to 1TP30 (DEMOD OUT). Trigger scope on 2TP27 (REF FRAME) so that an entire field can be seen.

Note

Ensure that fields displayed on scope channels A and B are the same field by comparing the last line of the field.

STEP 9 Loosen three screws (Figure 4-18, A, B, and C) which secure the audio and control track record/play head assembly. Head assembly can thus be moved about the pivot point (B).

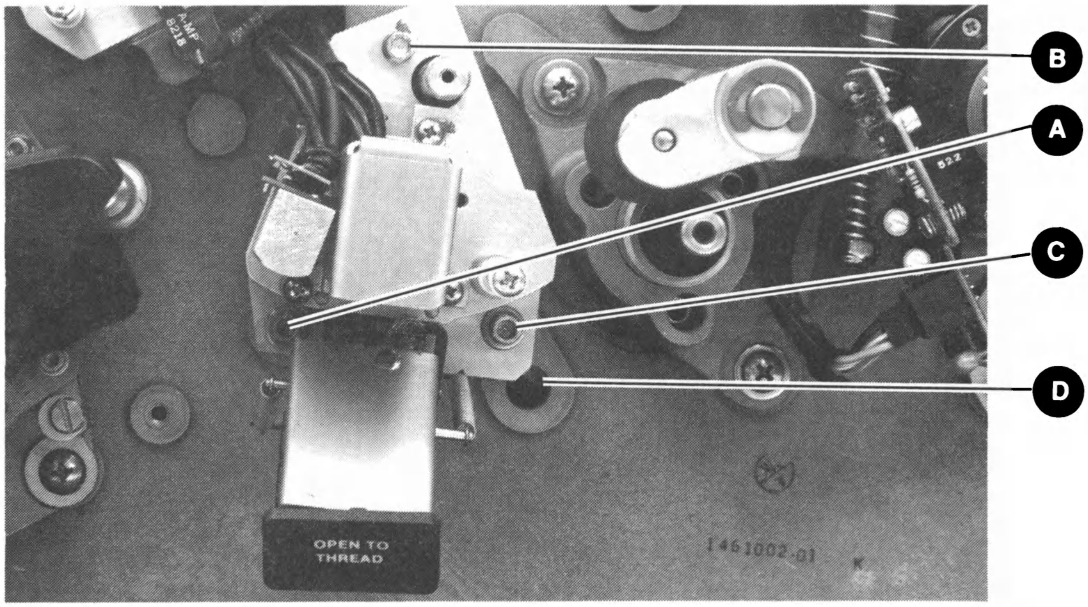


Figure 4-18. Control Track Position Adjustment

STEP 10 Press PLAY and expand scope sweep to observe vertical sync area. Adjust scope channel A (SELECTED VIDEO) so sync coincides with a convenient graticule line on scope.

Note

SYSTEM indication 01 may be displayed when play mode is entered. It is not significant to this adjustment. Simply press SYSTEM to clear indication, and continue.

STEP 11 Insert adjustment tool (Ampex Part No. 1461390) in hole (D), and adjust position of the audio and control track head assembly about the pivot as necessary so that playback vertical sync (DEMOD OUT, observed on scope channel B) coincides with EE vertical sync (SELECTED VIDEO, observed on scope channel A) within ±5.0 µs.

STEP 12 Tighten three screws which were loosened in step 9 to preserve coincidence of vertical sync observed on scope channels A and B.

STEP 13 Rewind and replay tape to confirm adjustment. Repeat steps 9 through 12, if necessary.

STEP 14 Restore SCANNER PHASE switch 5S1 to the original setting.

STEP 15 Place AST ON/OFF switch 4S3 in ON position.

STEP 16 Return REF SELECT switch 6S5 to AUTO position.

Completion in sequence of all adjustments listed in paragraph 4-21 fulfills interchange requirements. Remove test equipment, and reinstall transport trim.

4-39 TROUBLESHOOTING

When self-test logic in the VPR-80 detects a fault condition, the FAULT indicator is lighted. The operator should then press the FAULT switch to observe the numerical indication of the fault on the display. If two or more faults are detected, fault indications are queued for display. Fault indications are not prioritized, but are queued for display in the reverse order in which the faults were detected. Fault indications in the queue cannot be displayed if the cause of the first fault indication displayed is persistent and is not corrected. Therefore, it is important to remember to press the FAULT switch again after a fault has been cleared. This will cause any additional fault indications in the queue to be displayed.

The numerical indication of an intermittent fault can be recalled for display only once. Therefore, it is prudent to take careful note of all fault indications when displayed. Continue to press the FAULT switch until the FAULT indicator goes out. This assures that all latent fault indications have been displayed. The same holds true for system (nonstandard condition) indications.

4-40 System Indications

When the SYSTEM indicator is lighted, a nonstandard condition or operating limitation has been detected by VPR-80 self-test logic. Nonstandard condition and operating limitation indications are listed in Section 9, Part II

The term "shutdown," as used in Section 9, Part II indicates that the VPR-80 is forced to stop mode/standby condition, with remote control modes and MDAs inhibited, brakes on, and pinch roller disengaged.

4-41 Fault Indications

When the FAULT indicator is lighted, a machine fault has been detected by the VPR-80 self-test logic. FAULT indications are five-digit code numbers. The first three digits indicate the subsystem or PWA in which the fault is detected. The two-digit dash number indicates the localized area at fault. Wherever possible, the dash number corresponds to the particular chip number which is most suspect. FAULT indications are listed in Section 9, Part II.

The term "shutdown," as used in Section 9, Part II indicates that the VPR-80 is forced to stop mode/standby condition, with remote control modes and MDAs inhibited, brakes on, and pinch roller disengaged.

Detailed troubleshooting is done with the diagnostic probe assembly. The probe, which is part of the accessory Diagnostic Kit (Ampex No. 1450981), enables the technician to isolate a detected fault to the individual chip or group of discrete components. The probe assembly, shown in Figure 4-19, is plugged into a PWA-edge connector on the Control PWA. Diagnostic firmware in ROM storage on this PWA is enabled and accessible when the VPR-80 is placed in diagnostic setup modes. Detailed instructions on the use of the diagnostic probe (Ampex P/N 1809549) are given in Section 9, Part II.

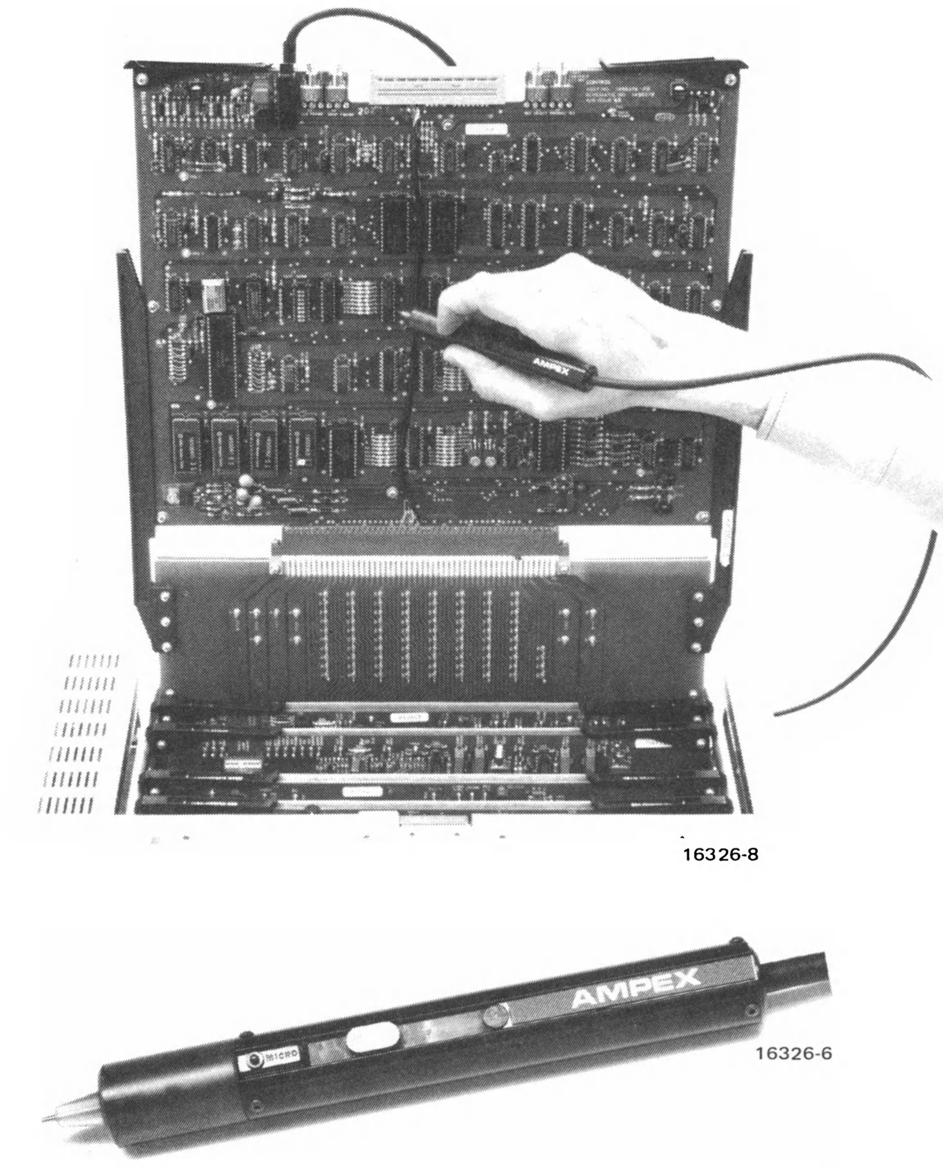


Figure 4-19. VPR-80 Diagnostic Probe Accessory

PART II
SECTION 1
GENERAL INFORMATION

1-1 SCOPE AND ORGANIZATION

1-2 Organization of Topics

Part II is organized around the six major VPR-80 subsystems. Sections 2 through 7 each cover a separate subsystem; accessory PWAs are covered in Section 8, Diagnostics in Section 9. General organization of Part II of this manual is as follows:

Section	Subject
1	General Information
2	Power System
3	Video System
4	Audio System
5	Servo System
6	Control System
7	Transport System
8	Accessories
9	Diagnostics

Classification, under subsystem, of assemblies which are separately serviceable (and replaceable) is somewhat arbitrary. For example, the capstan assembly could conceivably be part of either the transport, the control, or the servo system. However, because of the kind of theory and maintenance information provided, the capstan assembly is included under the servo system (Section 5). Breakdown of serviceable assemblies by subsystem is shown in Figure 1-1.

Each section in Part II provides the same essential information:

- Statement of subjects covered
- Reference to applicable drawing information
- Theory of operation explanations
- Instructions for removing (and reinstalling) replaceable assemblies
- Instructions for repairing assemblies

- Confidence check procedures (where applicable)
- Alignment procedures, including all test, adjustment, and performance verification instructions

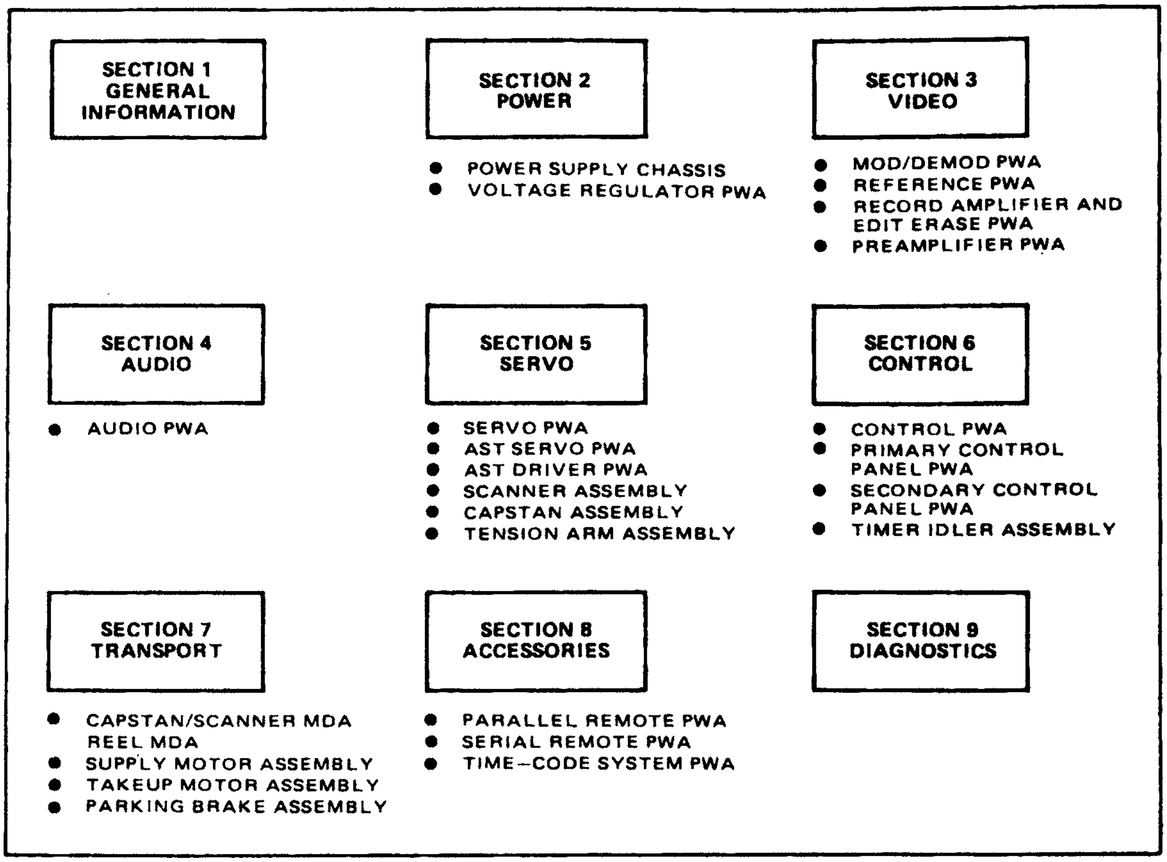


Figure 1-1. Organization of Topics in Part II

1-3 Index of Assemblies

An alphabetical listing of PWAs and replaceable assemblies showing where they are covered in Part II of this manual is given in Table 1-1.

1-4 RELATED DRAWINGS

The introductory paragraph in each section of Part II of this manual references related Ampex drawings. Drawings are found in the *VPR-80 Parts Lists and Schematics* manual. Drawing information includes assembly drawings, related parts lists, schematics, and wiring diagrams.

1-5 INTEGRATED CIRCUITS

Appendix A of the *VPR-80 Parts Lists and Schematics* manual contains pinout drawings and truth tables for all integrated circuits used in the VPR-80. The

Table 1-1. Index of Assemblies

PWA or Replaceable Assembly	Assembly Drawing No.	Covered in Part II, Section
AST Driver PWA	1450266	5
AST Servo PWA	1450256	5
Audio PWA	1450422	4
Capstan Assembly	1461100	5
Capstan/Scanner MDA	1450586	7
Capstan Tach PWA	1463431	5
Control PWA	1465505	6
Mod/Demod PWA (525)	1450206	3
Mod/Demod PWA (625)	1450216	3
Motor Drive Amplifier (MDA) Assembly	1450560	7
Parallel Remote PWA	1450466	8
Parking Brakes	1461148	7
Photo Potentiometer PWA	1461341	5
Pinch Roller Assembly	1461090	7
Power Supply Chassis	1450501	2
Preamplifier PWA	1468551	3
Primary Control Panel PWA	1450660	6
Record Amplifier and Edit Erase PWA	1450296	3
Reel MDA	1450593	7
Reference PWA (NTSC)	1450346	3
Reference PWA (PAL-M)	1450363	3
Reference PWA (PAL/SECAM)	1450356	3
Scanner Assembly	1461430	5
Secondary Control Panel PWA	1450640	6
Serial Remote PWA	1472470	8
Servo PWA	1462534	5
Supply Motor Assembly	1461010	7
Takeup Motor Assembly	1461020	7
Tape Timer Tach/Tip PWA	1468560	6
Tension Arm Assembly	1461040	5
Time-Code System PWA	1450410	8
Timer Idler Assembly (60 Hz)	1461160	6
Timer Idler Assembly (50 Hz)	1461161	6
Transport Assembly	1461000	7
Voltage Regulator PWA	1465498	2

technician should familiarize himself with two ICs in particular: the Motorola MC6802 microprocessor (Ampex Part No. 589-759) and the Intel 8253 programmable interval timer (Ampex Part No. 589-617).

The MC6802 microprocessor is used in both the control and servo subsystems of the VPR-80. The 8253 programmable interval timer (PIT) is used throughout digital control portions of the control and servo subsystems. Need for familiarity with characteristics of the microprocessor is self-evident. The PIT chip is composed of three independent 16-bit down counters. Each counter can be placed in one of six modes of operation under software control. Counters can be used as programmable rate generator, event counter, binary rate multiplier, real-time clock, digital one-shot, or complex motor controller. Because of the versatility of the PIT chip, the technician must be familiar with its several capabilities when reading schematics.

The technician's familiarity with the microprocessor and the PIT chips is assumed in the following sections of this manual.

1-6 CONVENTIONS

1-7 Circuit Designations

In this part of the manual, PWAs, integrated circuits, and individual pins of ICs are designated on block diagrams as follows:

5U77-1 = pin 1 of circuit U77 on Servo PWA (PWA5)

The PWA number is given first (see Part I, Table 2-1) and then the IC reference designator. The dash number designates the pin contact.

1-8 Connector Symbology and Addressing

The following paragraphs explain connector symbology and addressing conventions used on block diagrams in this part of the manual, and on schematics in the *VPR-80 Parts Lists and Schematics* manual. PWA and circuit designations, signal mnemonics, and connector numbers shown in the following illustrations are all hypothetical and are for explanation purposes only.

1-9 Block Diagrams

Many block diagrams show two (or more) PWAs on the same sheet of the diagram. Each PWA is enclosed in phantom boundary lines, and the PWA number (i.e., A5) is enlarged and included within the phantom lines. See Figure 1-2. Where electrical connection between PWAs is made via PWA edge connector, the connector contact number is enclosed in a circle as shown between PWA5, contact 14 and PWA4, contact 2 in Figure 1-2.

When a signal exits a PWA to an external destination, such as via the I/O connector panel, the exiting connector contact number is enclosed in a square (J1-29 in Figure 1-2). When a signal enters a PWA from an external source, such as via the I/O connector panel, the entering connector contact number is also enclosed in a square (J2-38 in Figure 1-2).

Where signals exit or enter a PWA via a connector in the field of the PWA (not a PWA edge connector), the connector contact number is enclosed in a square which is shown in the phantom line boundary of the PWA. See J3-16 and J4-13 in Figure 1-2.

Some odd-numbered PWA edge connector contact symbols also include a dot within the circle indicating that a jumper is included in the PWA edge connector. The jumper is placed straight across the two rows of connector contacts. Thus, the next higher even-numbered contact is also connected electrically. This is shown in the inset of Figure 1-2.

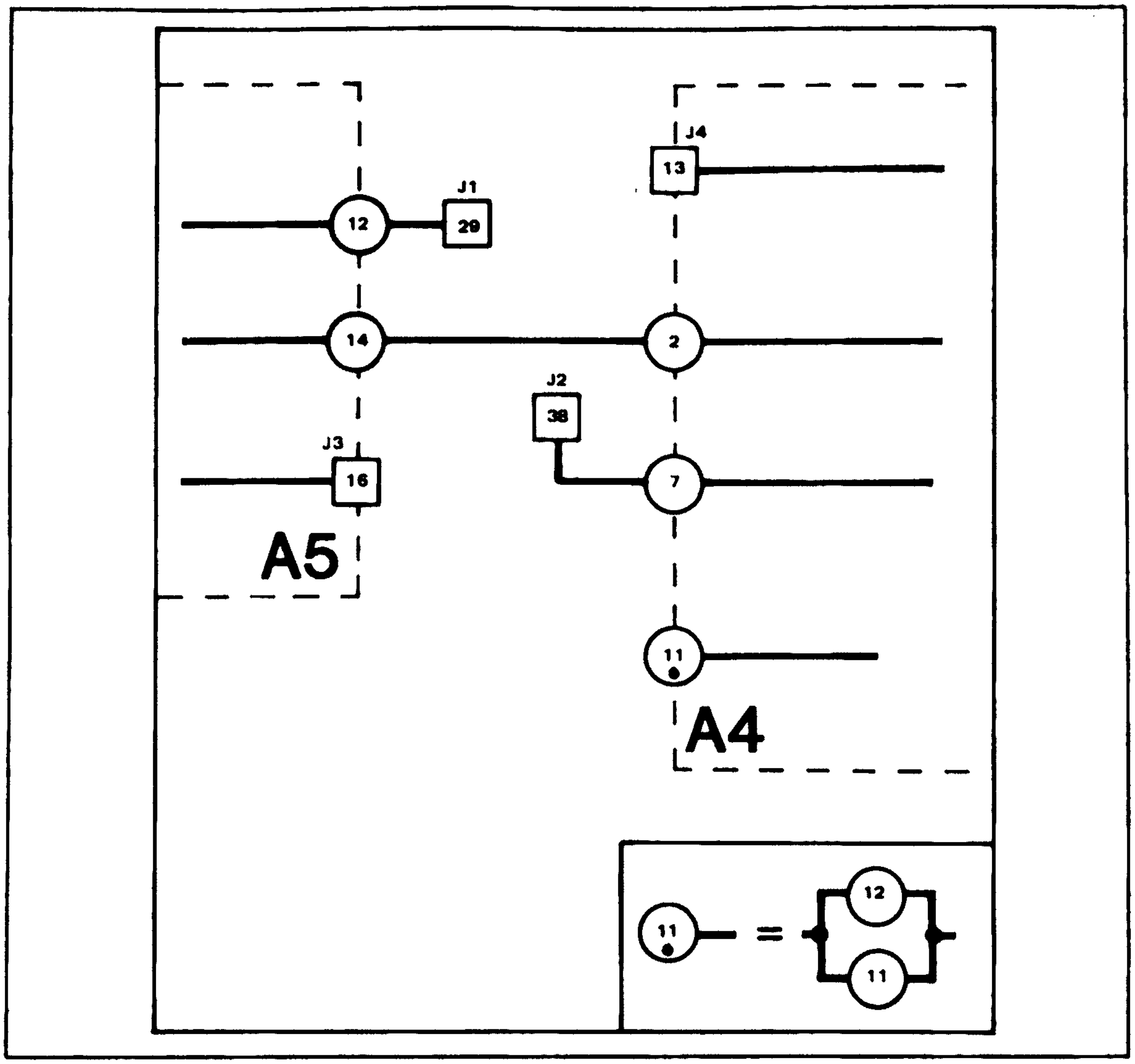


Figure 1-2. Block Diagram Connector Symbology

When a signal line must be broken for clarity of the drawing, the line is terminated by the signal mnemonic enclosed in a hexagon. Continuation of the signal line is begun with the signal mnemonic (also enclosed in a hexagon) which may appear at more than one point in the diagram. See Figure 1-3. This convention is used when the signal destination(s) is shown on the same block diagram.

Signals which exit the block diagram to appear on another diagram are given other symbology and/or addressing.

In most cases, address decoder outputs are fanned out to several destinations. At the source, the decoder output mnemonic is enclosed in the symbol shown in Figure 1-4. The mnemonic, enclosed in the same symbol, is shown at each destination, which may be on several different diagrams.

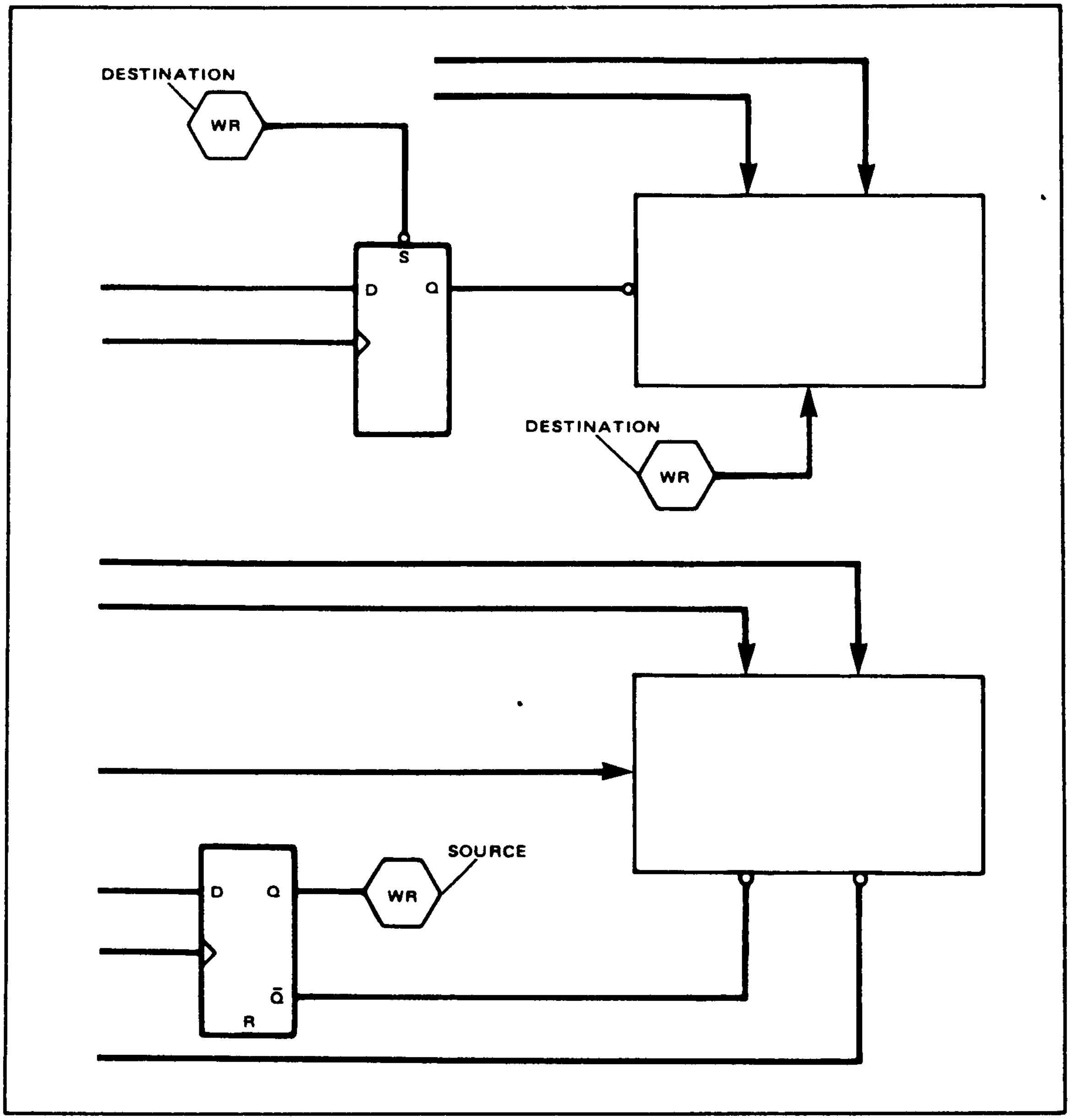


Figure 1-3. Connector Symbology within Same Block Diagram

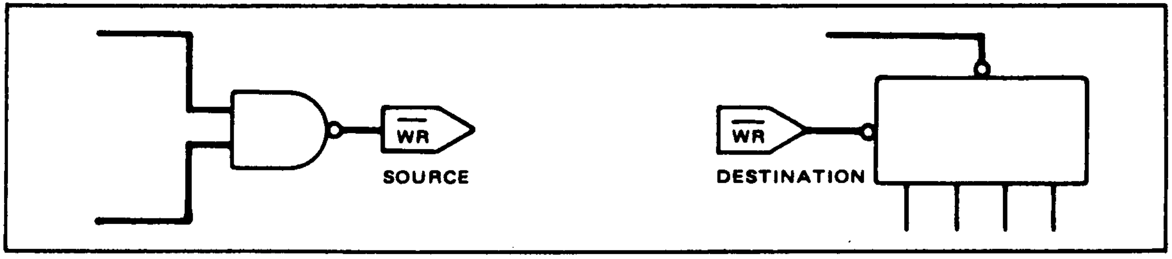


Figure 1-4. Decoded Address Connector Symbology

Forward and back addressing are used on the block diagrams, wherever possible. Figure 1-5 shows the simplest example where the signal source on one PWA and the destination on another PWA are linked via the motherboard. In this case, PWAs are shown on different block diagrams.

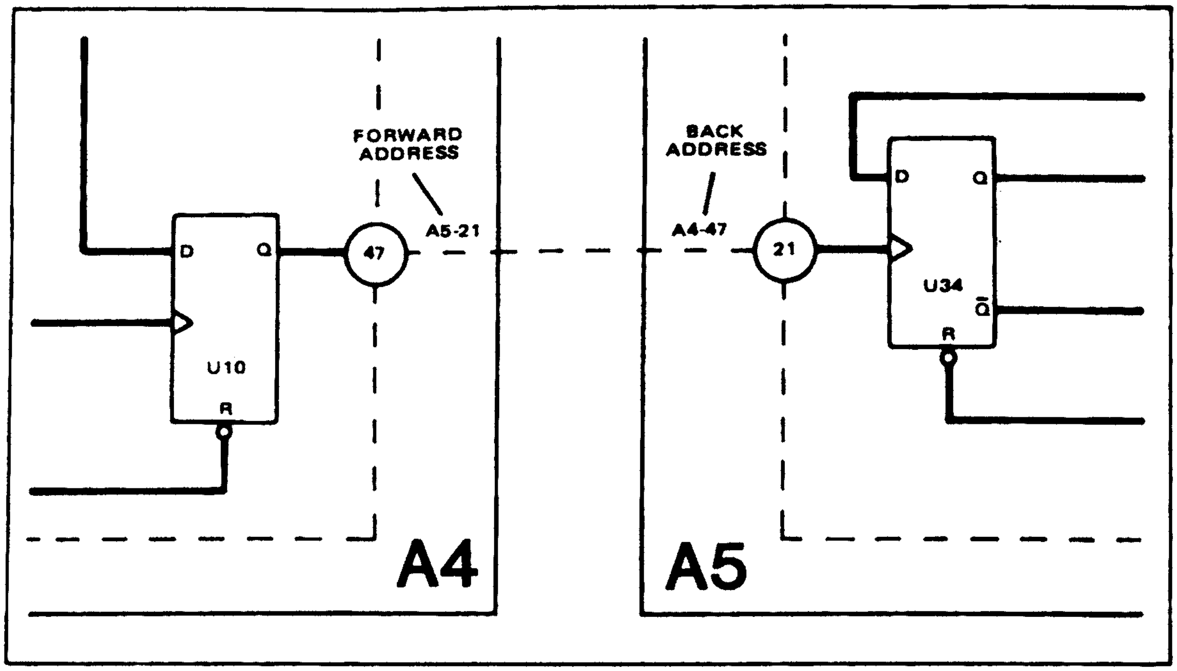


Figure 1-5. Addressing Between PWA Edge Connectors on Block Diagrams

Simple forward and back addressing between PWA edge connectors is not always possible. This depends upon how the block diagram is laid out. To keep the diagrams as clear as possible, symbology shown in Figure 1-6 is often used. The signal name and address are enclosed in an arrow-shaped symbol. The forward address and figure number of the diagram are shown in the symbol at the source. At the destination, the symbol includes the source address and its figure number.

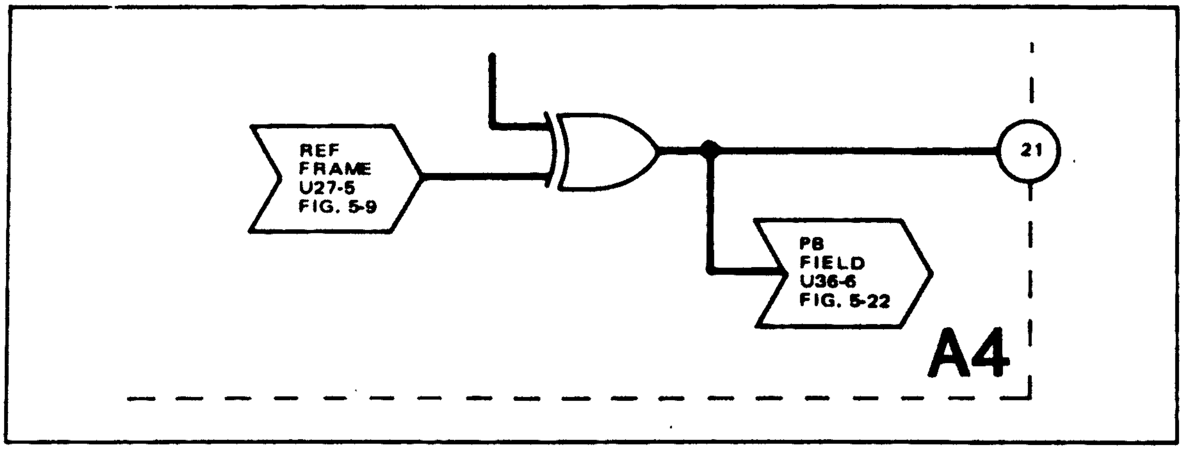


Figure 1-6. Addressing Between Different Block Diagrams

1-10 Schematics

Schematic diagrams, found in the *VPR-80 Parts Lists and Schematics* manual, employ slightly different, although consistent, symbology. Schematics are composed of one to three sheets.

A signal line which exits one sheet of a schematic diagram and appears on another sheet is terminated on the first sheet by a letter enclosed in a hexagon, as shown in Figure 1-7. Continuation of the signal line on another sheet of the same schematic is shown on that sheet by the same letter, also enclosed in a hexagon.

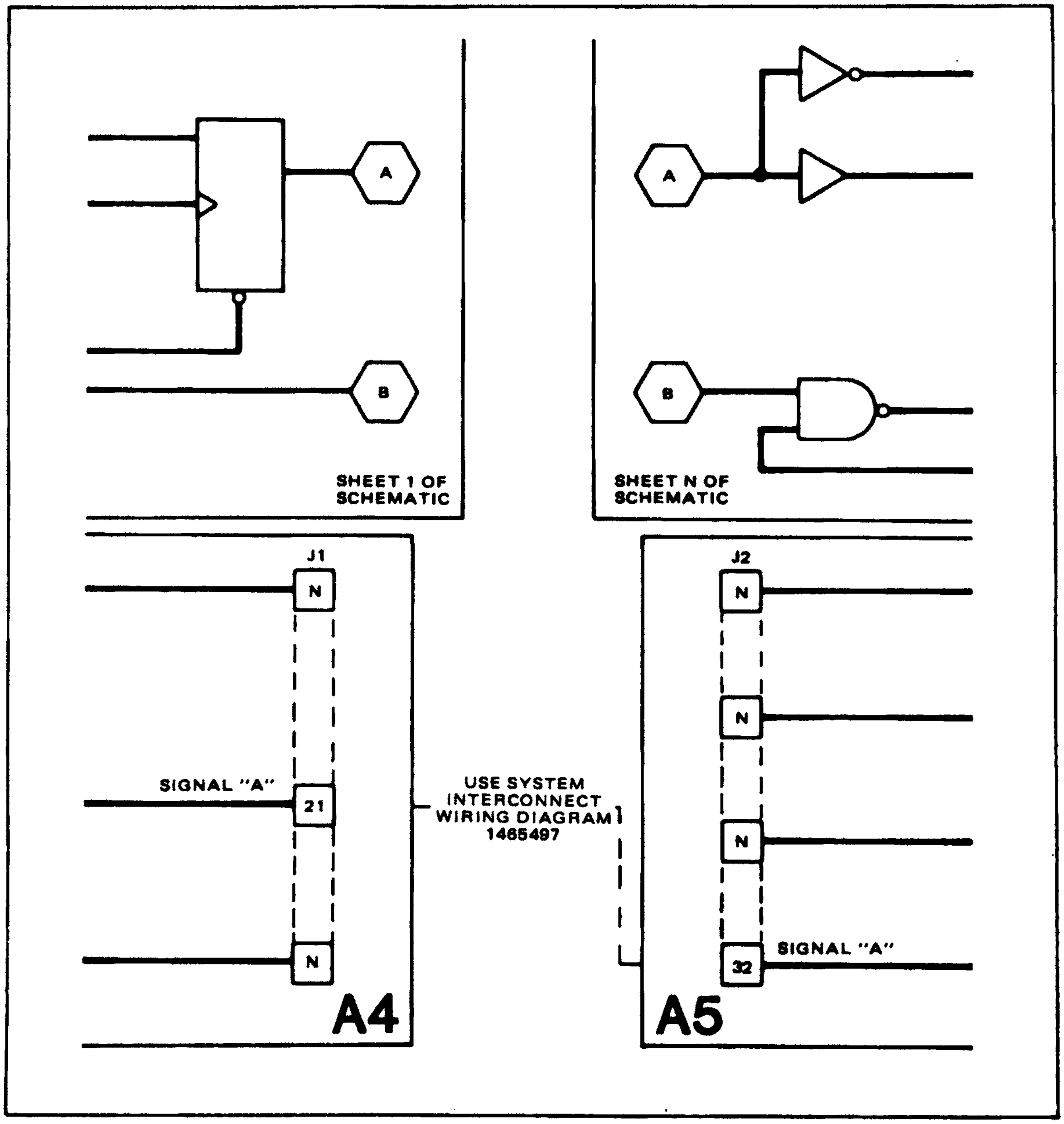


Figure 1-7. Schematic Diagram Connector Symbology

When a signal line exits one schematic (PWA) and appears on another schematic (PWA), the connector designation is shown, and the pin contact is shown below it, enclosed in a square. To follow the signal, the System Interconnect Wiring Diagram (Drawing No. 1465497) should be used. The wiring diagram provides a road map of signals between PWAs and subassemblies. Each conductor on the wiring diagram shows the individual signal name or designation.

PART II
SECTION 2
POWER SYSTEM

2-1 GENERAL

This section provides theory of operation explanations for the power supply and instructions on removal of the power supply from the VPR-80. In addition, voltages at each test point are tabulated, and instructions for adjustment of the power switch pushrod are given.

The following drawings, which are included in the *VPR-80 Parts Lists and Schematics* manual, are referenced in this section.

Drawing	Drawing No.
Power Supply Chassis Assembly	1465504
Voltage Regulator PWA	1465498
Voltage Regulator PWA Schematic	1465500
System Interconnect Wiring Diagram	1465497

2-2 THEORY OF OPERATION

The power system is composed of the power supply chassis assembly and the voltage regulator assembly. Each assembly includes interconnecting wiring harnesses. The voltage regulator assembly consists of the Voltage Regulator PWA and the heat sink upon which the three series pass transistors are mounted.

2-3 Power Supply Chassis

The power supply chassis assembly is composed of power transformer T1, bridge rectifiers CR1, CR2, and CR3, the ac input and fuse panel, circuit breaker CB1, and a cooling fan. Primary power inputs from 100 Vac to 260 Vac are accepted. Figure 2-1 shows the power supply chassis, the Voltage Regulator PWA, and distribution of the power supply outputs to the various subassemblies and PWAs in the VPR-80.

Main power is applied through an LC input filter to circuit breaker CB1. When the operator turns VPR-80 power on, the PWR switch closes CB1 by means of a mechanical pushrod assembly. Transformer T1 primary windings are connected in parallel for ac inputs in the 100—130-Vac range, or are connected in series for ac inputs in the 200—260-Vac range. The selection of appropriate connections on the primary side of T1 is made by the installation of two jumper plugs in the voltage tap selection connector J1. Figure 2-2 includes a table which shows where jumper plugs are installed for each ac input voltage. Outputs of three T1 secondary windings are applied to bridge rectifiers CR1, CR2, and CR3. Rectifier outputs are ±25 Vdc, +10 Vdc, and +11 Vdc, respectively, which are applied to the Voltage Regulator PWA. The 6V backup battery output (on VPR-80s manufactured prior to October 1985) for volatile RAM storage is also routed to the Voltage Regulator PWA. The secondary side of T1 also furnishes 220 Vac to the AST Driver PWA.

2-4 Voltage Regulator PWA

The Voltage Regulator PWA receives unregulated dc outputs of the power chassis and +5-Vdc and ±15-Vdc remote sense levels from the card cage motherboard. Its regulated outputs are +5 and ±15 Vdc. The Voltage Regulator PWA provides linear voltage regulation, linear current limiting, and switched overvoltage protection for these outputs. It also supplies unregulated +10.5 Vdc, +11 Vdc, ±25 Vdc, and +6 Vdc (battery supply). Refer to the Voltage Regulator PWA block diagram shown in Figure 2-2.

2-5 Voltage Regulation

The voltage regulator for +15 Vdc consists of sense amplifier U4-1, comparator U4-14, driver transistor Q10, and series pass transistor Q2. The +15V remote sense input from the motherboard is applied to the noninverting input of sense amplifier U4-1. Inverting input is connected to motherboard ground level. The differential error output of U4-1 is applied to the inverting input of comparator U4-14 which compares it with a +5.1V reference.

The +5.1V reference is derived from unregulated +25 Vdc by zener diodes VR5—VR7, resistors R54-R56, and precision resistors R57 and R77. Adjustment of the reference is provided by R78. This adjustment is sealed with Glyptol at manufacture.

If the +15-Vdc sense level tends to go high, the output of U4-14 goes low, decreasing the conduction of series pass transistor Q2 through driver Q10. The +15-Vdc output is thus regulated downward.

The voltage regulators for +5 Vdc and -15 Vdc operate in identical fashion on the unregulated +10.5-Vdc and -25-Vdc outputs of the power chassis.

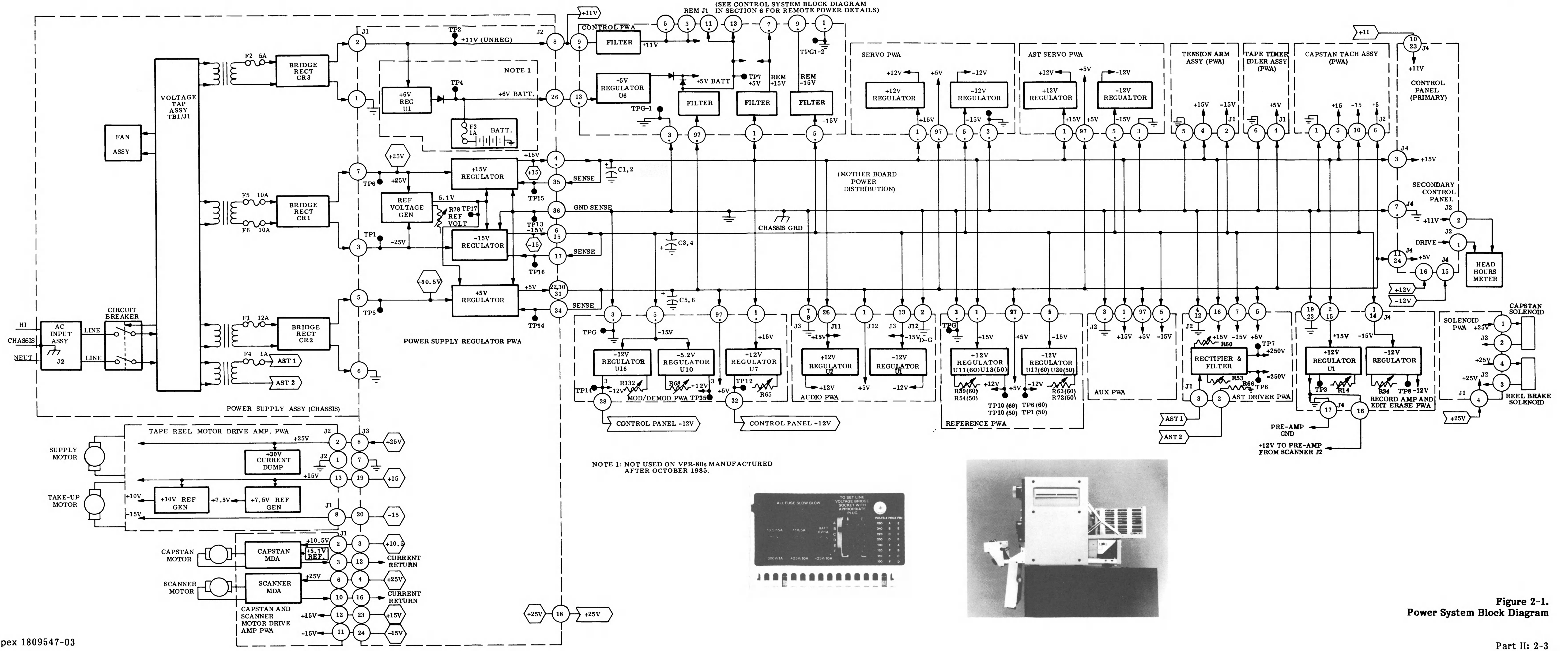
2-6 Current Limiting

Current limiting for the +15-Vdc output is provided by comparator U4-7 and sensing resistor R59. If current delivered tends to exceed nominal value, the output of U4-7 rises, thus decreasing the conduction of Q10 and Q2. As the +15-Vdc output current decreases, control is returned to voltage regulator U4-14.

Current limiters for +5 Vdc and -15 Vdc operate in identical fashion on the unregulated +10.5-Vdc and -25-Vdc outputs of the power chassis.

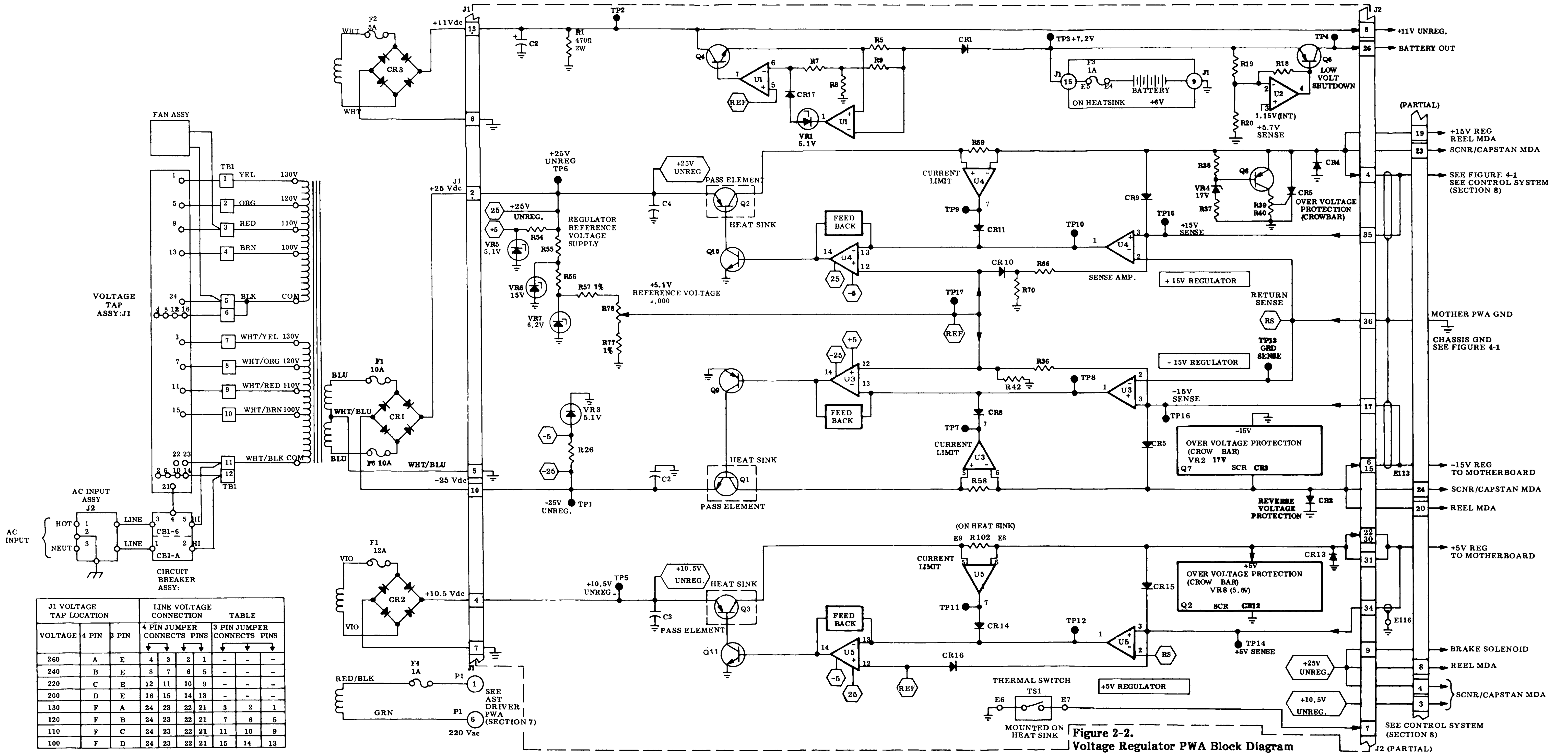
2-7 Overvoltage Protection

Overvoltage protection for the load on the +5-Vdc supply is provided by a zener/SCR network, or crowbar, composed of zener diode VR8, SCR CR12, and transistor Q12. If the +5-Vdc output voltage rises above the 5.6V zener value of



NOTE 1: NOT USED ON VPR-80s MANUFACTURED AFTER OCTOBER 1985.

Figure 2-1.
Power System Block Diagram



J1 VOLTAGE TAP LOCATION			LINE VOLTAGE CONNECTION TABLE						
VOLTAGE	4 PIN	3 PIN	4 PIN JUMPER CONNECTS PINS				3 PIN JUMPER CONNECTS PINS		
260	A	E	4	3	2	1	-	-	-
240	B	E	8	7	6	5	-	-	-
220	C	E	12	11	10	9	-	-	-
200	D	E	16	15	14	13	-	-	-
130	F	A	24	23	22	21	3	2	1
120	F	B	24	23	22	21	7	6	5
110	F	C	24	23	22	21	11	10	9
100	F	D	24	23	22	21	15	14	13

Figure 2-2.
Voltage Regulator PWA Block Diagram

VR8, Q12 is turned on. The emitter of Q12 supplies the trigger to SCR CR12. The +5-Vdc output is thus shorted to ground, and resulting excessive current sensed by R59 causes U4-7 to shut down the +5-Vdc supply. Capacitor C33 prevents triggering of the crowbar by momentary transient overvoltage outputs.

2-8 Battery Backup

On VPR-80s manufactured prior to October 1985, the unregulated +11-Vdc output of the power supply chassis is applied to the battery charger composed of U1-1, U1-7, Q4, Q5, VR1, and CR1. The regulated +7.2-Vdc output charges the battery (on the power chassis) and is supplied through Q6 to a +5V regulator on the Control PWA. When VPR-80 power is off, the battery supplies backup power to RAM chips on the Control PWA. Transistor Q6 is turned on by comparator U2-4 as long as the battery (or charger) output is above +5.7 Vdc. When battery output decays below +5.7 Vdc, U2-4 causes Q6 to cut off battery output.

2-9 Overtemperature Sensor

Thermal sensor TS1 is mounted on the side of the series pass transistor heat sink. If heat sink temperature rises above 165°F (73.8°C)*, TS1 closes, grounding connector pin J2-7. Self-test circuitry on the Control PWA detects this condition and causes the SYSTEM indicator to light—nonstandard condition code 20. It does not cause shutdown, but the operator is thus warned that the cause of overheating should be investigated at the next opportunity.

2-10 CONFIDENCE CHECKS

Two maintenance setup codes are available for confidence checks of the power supply and regulator assembly. Setup code 20 enables a quick check of battery voltage, and setup code 30 enables a quick check of the ±15-Vdc regulated supplies and the +11-Vdc unregulated supply.

2-11 Battery Voltage

On VPR-80s manufactured prior to October 1985, setup code 20 enables the technician to read the battery output voltage on the VPR-80 primary control panel as follows:

STEP 1 With the VPR-80 in stop mode, press SETUP.

STEP 2 Enter 20 on keypad numeric switches.

STEP 3 Press keypad ENTER switch. Timer display will show eight hexadecimal (hex) digits which are identified in Figure 2-3. The third and fourth digits from the right indicate battery voltage. (The other digits which indicate local and remote shuttle control and local tracking control are explained in Section 6.)

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*195 °F (90.6°C) in earlier VPR-80s.

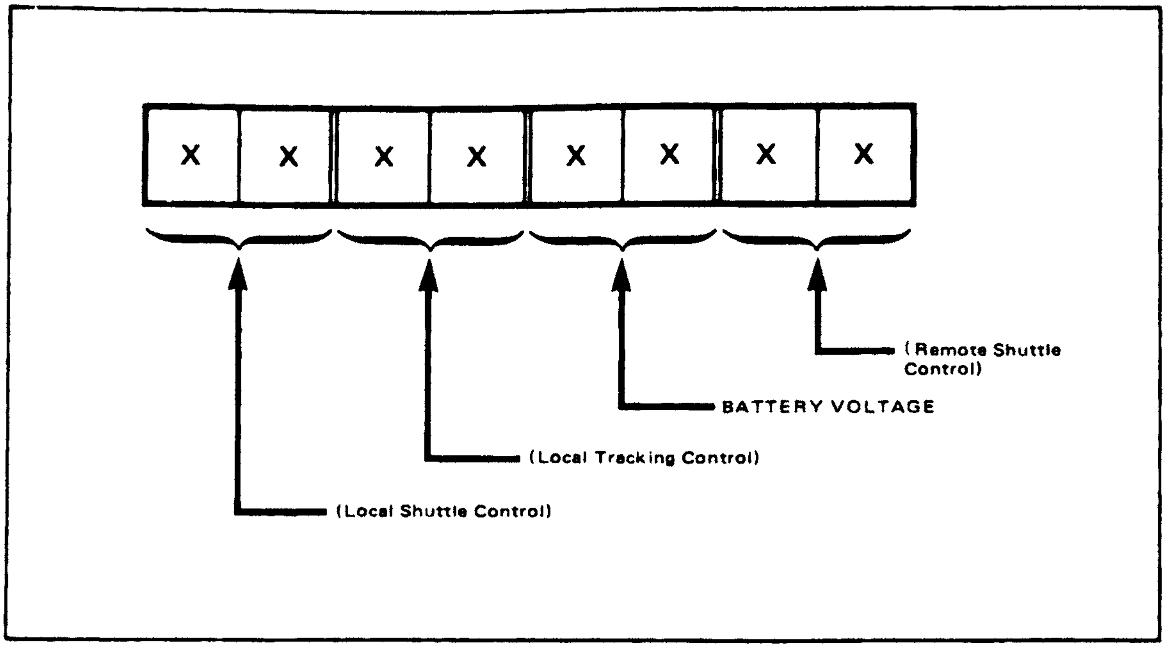


Figure 2-3. Setup Code 20 Display—Battery Voltage

Battery voltage is indicated by two hex digits. Voltage value is divided into 256 binary increments. Thus, the displayed range is **00-FF** (hex), where **80** (hex), or half scale, is the nominal voltage.

STEP 4 Press alternate action SETUP switch to exit setup mode.

The battery voltage is continually monitored at field rate as part of the vertical interval interrupt (INT 0). (See Section 6.)

2-12 Power Supply Voltages

Setup code 30 enables the technician to read three power supply output voltages on the VPR-80 primary control panel display: ±15-Vdc regulated and +11 Vdc unregulated. They are indicated as follows:

STEP 1 With the VPR-80 in stop mode, press SETUP.

STEP 2 Enter 30 on keypad numeric switches.

STEP 3 Press keypad ENTER switch. Timer display will show eight hexadecimal (hex) digits which are identified in Figure 2-4.

Each of the three voltages is indicated by two hex digits. Each voltage value is divided into 256 binary increments. Thus, displayed range is **00-FF** (hex), where **80** (hex), or half scale, is the nominal voltage.

STEP 4 Press alternate action SETUP switch to exit setup mode.

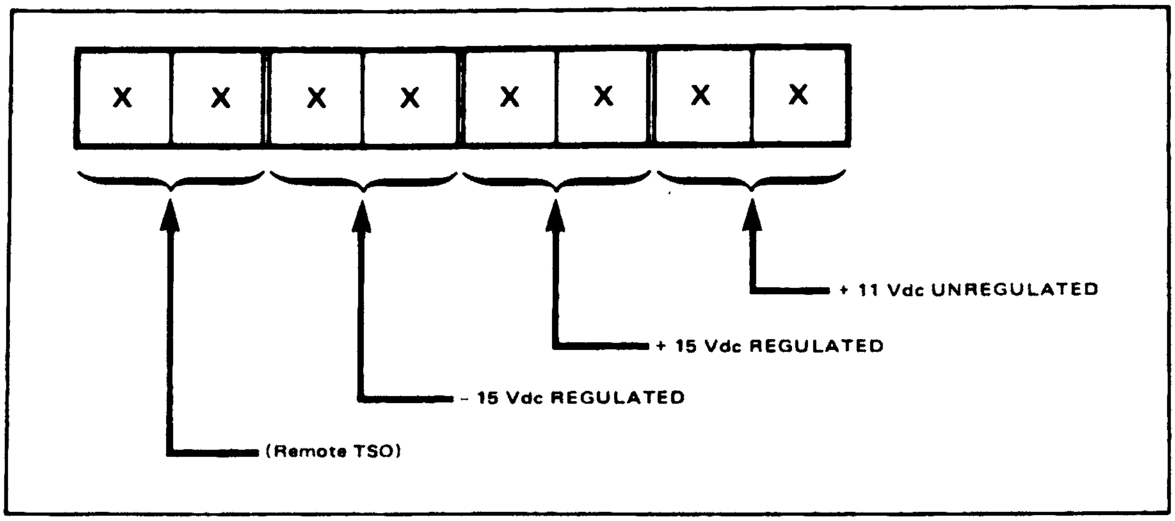


Figure 2-4. Setup Code 30 Display—Power Supply Voltages

The ±15-Vdc regulated outputs are continually monitored by diagnostic routine as follows:

- A value of **88** (hex) is the upper limit, which when reached, produces fault indication **108-01** or **108-04**.
- A value of **78** (hex) is the lower limit, which when reached, produces fault indication **108-03** or **108-05**.
- A value of **6F** (hex) is the minimum, which when reached, produces fault indication **108-02** or **108-06**.

The +11-Vdc unregulated output is monitored as an analog of the ac line input voltage. System indications **17** (HI LINE) and **18** (LO LINE) are produced when the upper and lower limits of the ac line input voltage are reached. Table 2-1 shows the ac line voltage, +11-Vdc output, and the corresponding hexadecimal display of +11-Vdc. Values are shown for each placement of the line voltage select jumpers (VPR-80 in stop mode/ready condition).

Table 2-1. Unregulated +11 Vdc Supply with Various AC Line Inputs

Placement of Line Voltage Select Jumper for (Vac)	Setup Code 30 Indication (Hex) of +11 Vdc Supply	System Indication (Hex) of +11 Vdc Supply	Without Accessory PWAs		With Parallel Remote Control Panel	
			Line Input (Vac)	+11 Vdc Supply	Line Input (Vac)	+11 Vdc Supply
100 60 Hz	95	17 (Hi Line)	107	12.90	111	12.88
100	8A-83 (nominal)		100	11.93	100	11.33
100	6F	18 (Lo Line)	83	9.54	87.5	9.62
100	68-61 (minimum)		78	9.02	78.5	8.52
110 60 Hz	95	17 (Hi Line)	117	12.86	121.5	12.88
110	8C-84 (nominal)		110	12.01	110	11.37
110	6F	18 (Lo Line)	90.7	9.52	95.7	9.59
110	64-5E (minimum)		82.7	8.62	83.6	8.26

(Continued next page)

Table 2-1. Unregulated +11 Vdc Supply with Various AC Line Inputs (Continued)

Placement of Line Voltage Select Jumper for (Vac)	Setup Code 30 Indication (Hex) of +11 Vdc Supply	System Indication (Hex) of +11 Vdc Supply	Without Accessory PWAs		With Parallel Remote Control Panel	
			Line Input (Vac)	+11 Vdc Supply	Line Input (Vac)	+11 Vdc Supply
120 60 Hz	95	17 (Hi Line)	126	12.78	132	12.87
120	8C-84 (nominal)		120	12.06	120	11.49
120	6F	18 (Lo Line)	98.5	9.52	104	9.58
120	61-5C (minimum)		88	8.46	88	8.10
130 60 Hz	95	17 (Hi Line)	136	12.77	143	12.86
130	8D-85 (nominal)		130	12.11	130	11.52
130	6F	18 (Lo Line)	105.5	9.50	112	9.55
130	68-62 (minimum)		100	9.02	100	8.55
200 50 Hz	95	17 (Hi Line)	214	12.82	223	12.86
200	86-83 (nominal)		200	11.93	200	11.30
200	6F	18 (Lo Line)	166	9.57	175	9.61
200	6A-62 (minimum)		159	9.10	158	8.58
220 50 Hz	95	17 (Hi Line)	235	12.82	245	12.86
220	8A-83 (nominal)		220	11.89	220	11.37
220	6F	18 (Lo Line)	182	9.58	192	9.61
220	69-62 (minimum)		173	9.06	173	8.56
240 50 Hz	95	17 (Hi Line)	256	12.82	268	12.92
240	8A-83 (nominal)		240	11.94	240	11.29
240	6F	18 (Lo Line)	199	9.58	209	9.61
240	69-64 (minimum)		188	9.00	191	8.71
260 50 Hz	95	17 (Hi Line)	277	12.84	288	12.86
260	8A-83 (nominal)		260	11.93	260	11.33
260	6F	18 (Lo Line)	215	9.60	226	9.60
260	6D-5C (minimum)		209	9.38	193	8.01

2-13 REMOVAL/INSTALLATION

The power supply and regulator assembly must be removed from the VPR-80 for detailed troubleshooting and to make repairs. Remove the power supply and regulator assembly as follows:

STEP 1 Turn VPR-80 power off and remove VPR-80 power cord.

STEP 2 Remove two side trim panels from VPR-80 cabinet as outlined in Section 4, Part I, paragraph 4-13.

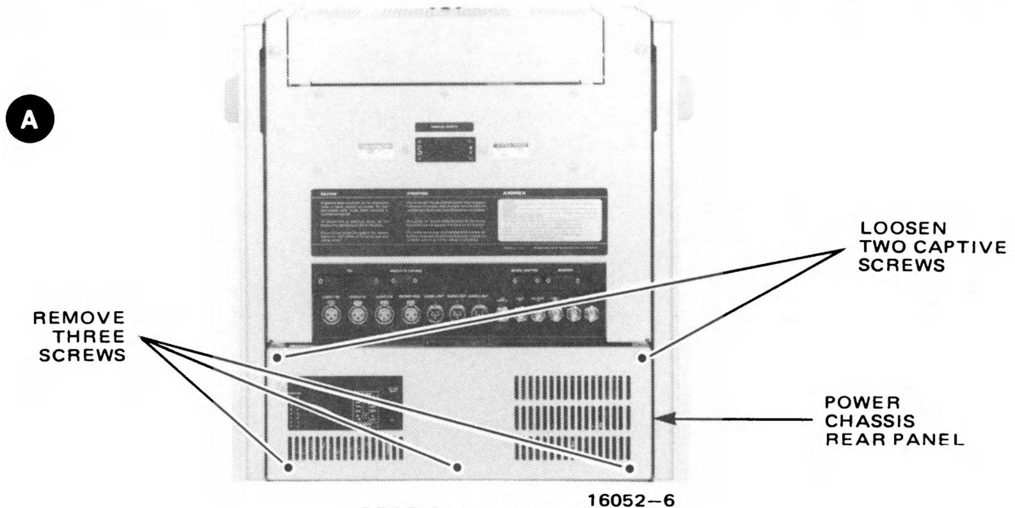
STEP 3 Remove three screws along lower edge of power chassis rear panel (see Figure 2-5, A).

STEP 4 Loosen two captive screws in upper corners of power chassis rear panel (see Figure 2-5, A) and remove panel.

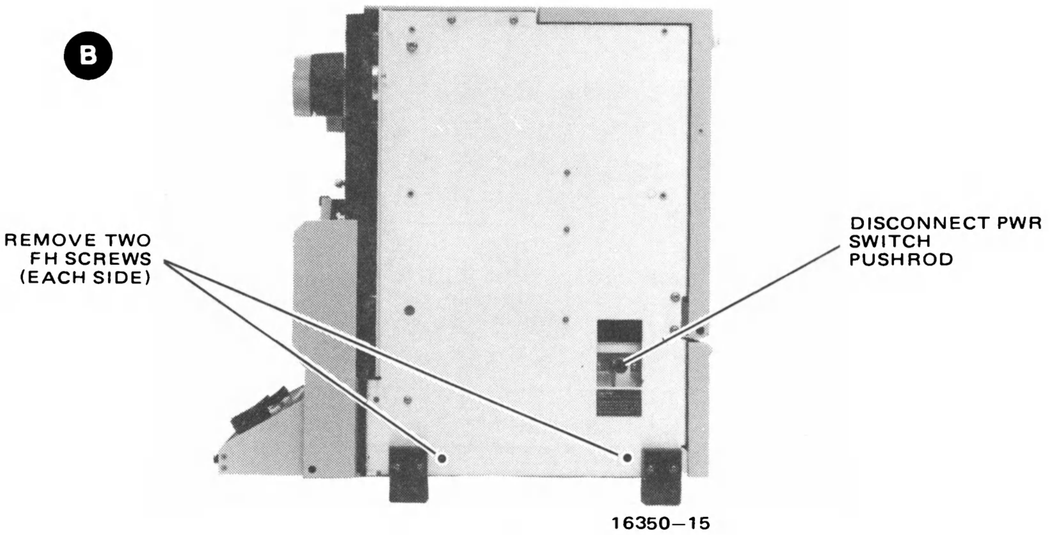
STEP 5 Remove two flathead screws at bottom of each side of VPR-80 cabinet which secure power supply and regulator assembly (see Figure 2-5, B).

STEP 6 Remove locknut securing PWR switch pushrod to circuit breaker. This is done through a cutout in right-hand side of cabinet (see Figure 2-5, B).

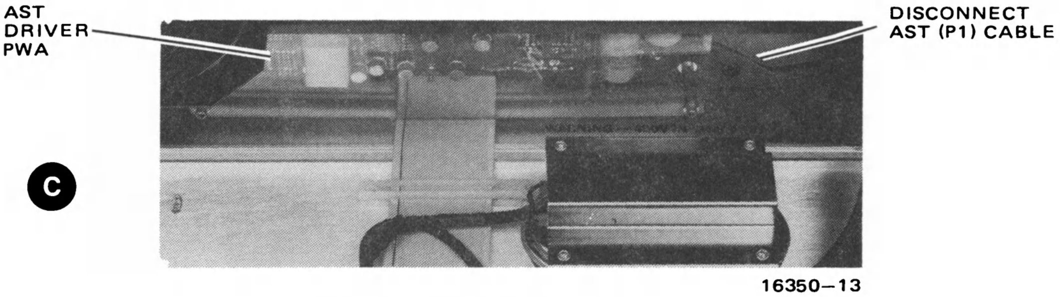
STEP 7 Pivot control panel assembly forward and disconnect AST (P1) cable (red/black and green) from AST Driver PWA (see Figure 2-5, C).



REAR OF VPR-80


B
REMOVE TWO FH SCREWS (EACH SIDE)
DISCONNECT PWR SWITCH PUSHROD
16350–15

RH SIDE OF VPR-80



CONTROL PANEL ASSEMBLY (PIVOTED FORWARD)

Figure 2-5. Removal of Power Supply and Regulator Assembly

STEP 8 Lower VPR-80 rear door assembly and disconnect two power chassis connectors (P2 and P3) at the Voltage Regulator PWA. Close rear door assembly.

STEP 9 Slide power supply and regulator assembly to rear and out of VPR-80 cabinet.

STEP 10 Lower rear door assembly again and place power supply and regulator assembly on upper side (front) of card cage.

STEP 11 Use extender cable (Ampex Part No. 1450790) to connect AST (P1) cable to AST Driver PWA.

STEP 12 Remove four screws and washers securing clear plastic shield to standoffs on top of Voltage Regulator PWA.

STEP 13 Reconnect two power chassis cables (P2 and P3) to Voltage Regulator PWA.

The power supply and regulator assembly is now ready for power-on troubleshooting.

The reinstallation procedure for the power supply and regulator assembly is essentially the reverse of its removal procedure. Some readjustment of the throw in the PWR switch pushrod may be necessary. See paragraph 2-14.

2-14 MECHANICAL ADJUSTMENT

Upon reinstallation of the power supply and regulator assembly it may be necessary to make an adjustment on the throw of the PWR switch pushrod. This adjustment is made as follows:

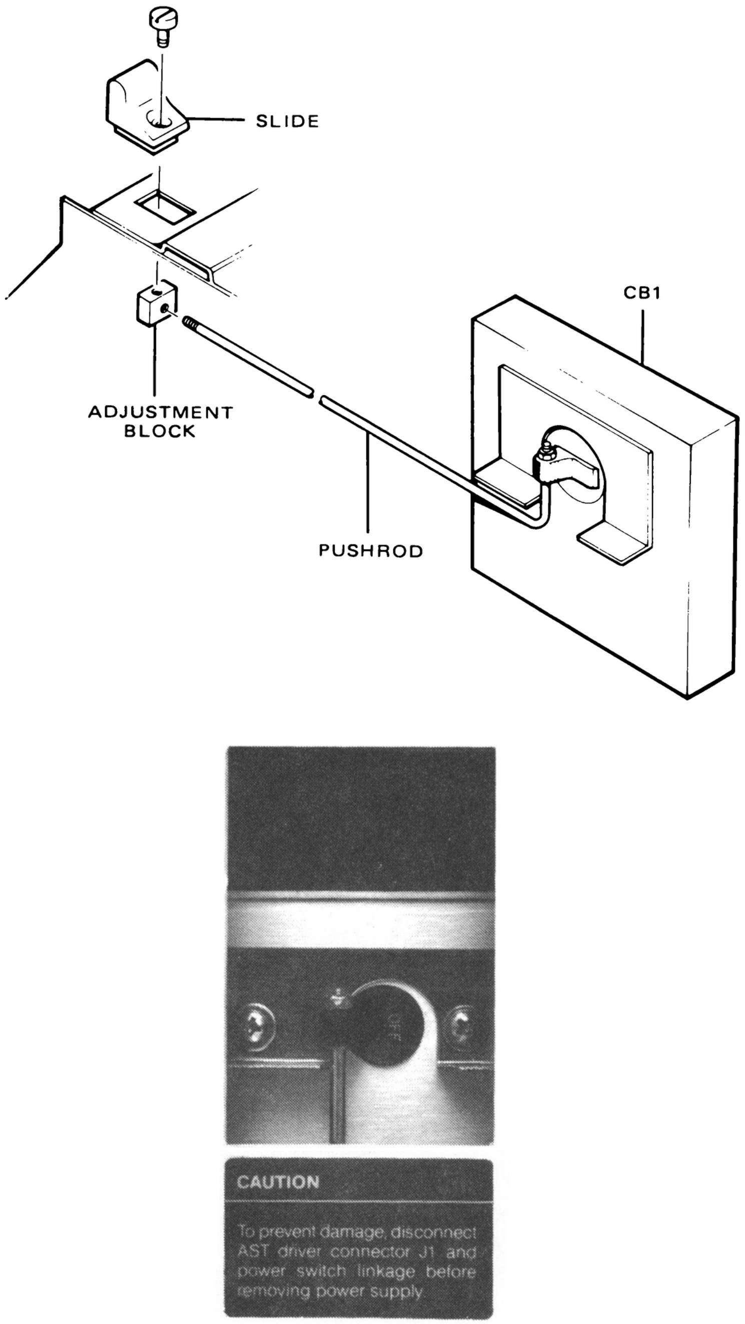
STEP 1 Remove screw securing PWR switch slide to adjustment block on pushrod (see Figure 2-6). Remove the slide.

STEP 2 With pushrod attached to the circuit breaker, pull it forward (power-on position) and rotate adjustment block on threads of the pushrod so that slide will line up with placard ON when slide is reattached to adjustment block.

STEP 3 Push the pushrod to rear (power-off position) and ensure that slide lines up with placard OFF. If it does not, detach slide and rotate adjustment block on threads of pushrod so that slide will line up with placard OFF when slide is reattached to adjustment block.

2-15 POWER SYSTEM ALIGNMENT

Figure 2-7 shows the location of each test point and the +5.1-Vdc reference adjustment control on the Voltage Regulator PWA. Table 2-2 lists power supply check points throughout the VPR-80 with nominal voltage measurements and tolerances. Adjustable components, where present, are also listed.



CAUTION

To prevent damage, disconnect AST driver connector J1 and power switch linkage before removing power supply.

Figure 2-6. Power Switch Pushrod Adjustment

Table 2-2. Power Supply Check Points

PWA	Check Point	Adjust	Voltage
Voltage Regulator	TP1		−25 Vdc unregulated
	TP2		+11 Vdc unregulated
	TP3		+6.8 ±0.7 Vdc*†
	TP4		Battery output †
	TP5		+10.5 Vdc unregulated
	TP6		+25 Vdc unregulated
	TP7		−15 Vdc current sense
	TP8		−15 Vdc differential error
	TP9		+15 Vdc current sense
	TP10		+15 Vdc differential error
	TP11		+5 Vdc current sense
	TP12		+5 Vdc differential error
	TP13		Ground sense
	TP14		+5 ±0.1 Vdc sense
	TP15		+15 +1.5/−0.5 Vdc sense
	TP16		−15 +0.5/−1.5 Vdc sense
	TP17	R78	+5.1 Vdc reference
Mod/Demod	TP12	R65	+12 ±0.01 Vdc
	TP14	R132	−12 ±0.01 Vdc
	TP35	R68	−5.2 ±0.01 Vdc
Audio	U2-2		+12 ±0.06 Vdc
	U1-3		−12 ±0.06 Vdc
Reference (525)	TP10	R42	+12 ±0.020 Vdc
	TP6	R68	−12 ±0.020 Vdc
Reference (625)	TP11	R57	+12 ±0.020 Vdc
	TP1	R75	−12 ±0.020 Vdc
Record Ampl. and Edit Erase	TP3	R14	+12 ±0.050 Vdc
	TP8	R34	−12 ±0.050 Vdc
Servo	TP31		+12 ±0.6 Vdc
	TP32		−12 ±0.6 Vdc
AST Servo	TP21		+12 ±0.6 Vdc
	TP25		−12 ±0.6 Vdc
AST Driver	TP7		+250 Vdc unregulated
	TP6		−250 Vdc unregulated
	TP5	R60	+125 ±2 Vdc‡
	TP4	R53	−125 ±2 Vdc‡
Control	TP7	R78 on Regulator	+5.000 +0.050 −0.00 Vdc
	C14/CR3		+5 ±0.2 Vdc

* Battery output with charger operating.

† Not used on VPR-80s manufactured after October 1985.

‡ Measure with a four-digit meter having probe impedance of 10M minimum. Measure with output connected to scanner (1M load resistor connected). This voltage appears when AST power is turned on and AST servo is centered. (See Section 5, Part II.) Plus and minus voltages must be matched ±0.25 Vdc.

(Continued next page)

Table 2-2. Power Supply Check Points (Continued)

PWA	Check Point	Adjust	Voltage
Parallel Remote	U20-3		−12 ±0.05 Vdc
	U19-2		+12 ±0.05 Vdc
	U17-2		+5 ±0.2 Vdc
	J1-3/4 or J2-18		+11 Vdc unregulated (±2 Vdc)
	J1-11		+5 ±0.5 Vdc

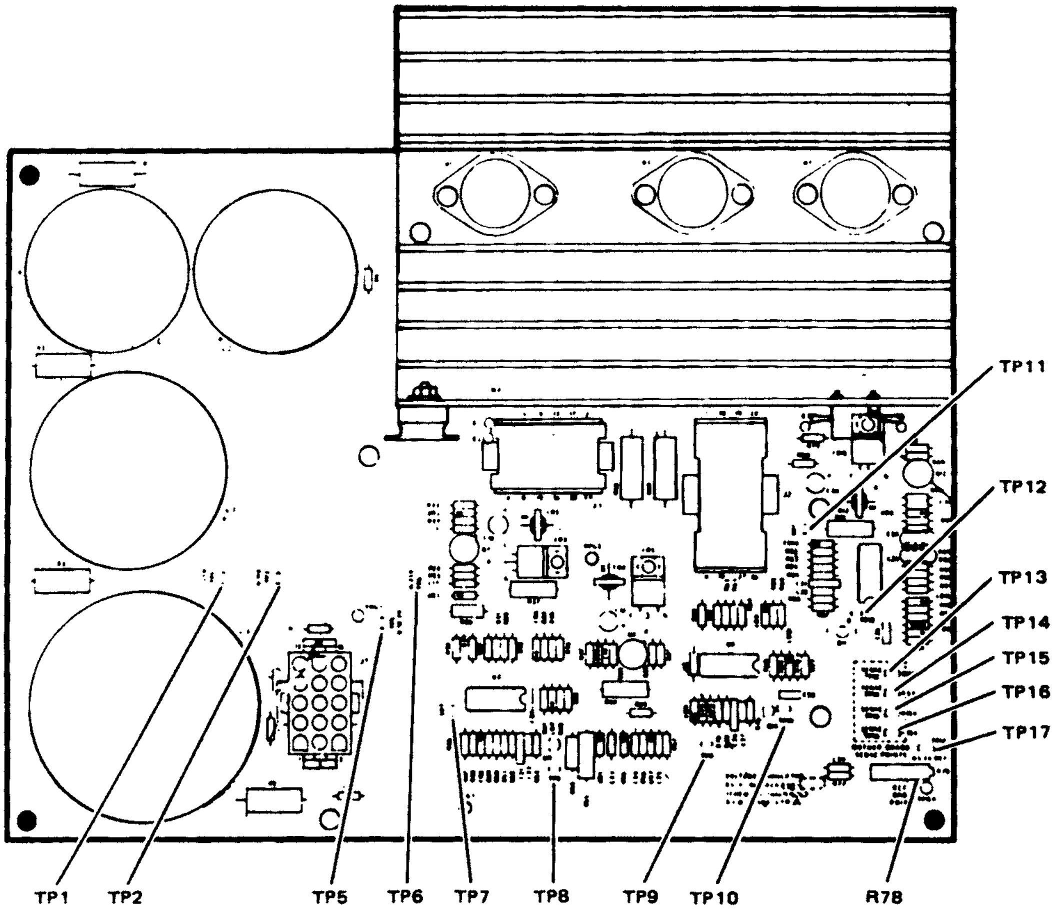


Figure 2-7. Voltage Regulator PWA (1455498) Test Points and Adjustment Control

PART II

SECTION 3

VIDEO SYSTEM

3-1 GENERAL

This section provides theory of operation information for the video system. Instructions are given for removal and reinstallation of the Record Amplifier and Edit Erase PWA. All procedures necessary for video signal system alignment and performance verification are spelled out in detail and illustrated with waveform photographs. Complete adjustment and calibration instructions for the Reference PWA are also included.

The following drawings, included in the *VPR-80 Parts Lists and Schematics* manual, are referenced in this section.

Drawing	Drawing No.
Mod/Demod PWA - 525/60	1450206
Mod/Demod PWA - 625/50	1450216
Mod/Demod PWA Schematic - 525/60 and 625/50	1450208
Reference PWA - NTSC	1450346
Reference PWA Schematic - NTSC	1450348
Reference PWA - PAL-M	1450363
Reference PWA Schematic - PAL-M	1450365
Reference PWA - PAL/SECAM	1450356
Reference PWA Schematic - PAL/SECAM	1450358
Record Amplifier and Edit Erase PWA	1450296
Record Amplifier and Edit Erase PWA Schematic	1450298
Preamplifier PWA	1468551
Preamplifier PWA Schematic	1468553
System Interconnect Wiring Diagram	1465497

In addition, the following illustrations are included at the end of this section.

Figure 3-65	Modulator/Demodulator PWA, NTSC/PAL-M and Modulator/-Demodulator PWA, PAL/SECAM Jumpers, Test Points, and Adjustments
Figure 3-66	Record Amplifier and Edit Erase PWA Test Points and Adjustments
Figure 3-67	Reference PWA, NTSC Jumpers, Test Points, and Adjustments
Figure 3-68	Reference PWA, PAL-M Jumpers, Test Points, and Adjustments
Figure 3-69	Reference PWA, PAL/SECAM Jumpers, Test Points, and Adjustments

3-2 THEORY OF OPERATION

The following paragraphs discuss video system theory of operation. The video system is composed of the Reference, Mod/Demod, Record Amplifier and Edit Erase, and Preamplifier PWAs.

3-3 Video Standards

The VPR-80 video system can be configured to comply with NTSC, PAL-M, PAL (PAL-I), or SECAM video standards. The VPR-80 is equipped with one of three video kits at manufacture, as specified by the customer: NTSC, PAL-M, or PAL/SECAM. Each kit is composed of a Reference PWA, Mod/Demod PWA, video record/play (AST) head, edit erase head, and timer idler assembly. Part numbers of these components are listed in Table 3-1.

Table 3-1. Part Numbers of Video Kit Components

	Components				
Video Kit	Mod/Demod PWA	Reference PWA	Edit Erase Head	AST Head	Timer Idler
NTSC	1450206	1450346	1401160	1451200	1461160
PAL-M	1450206	1450363	1401160	1451200	1461160
PAL/ SECAM	1450216	1450356	1401165	1451220	1461161

3-4 Mod/Demod and Reference PWAs

There are two configurations of the Mod/Demod PWA: one for NTSC and PAL-M, and one for PAL and SECAM. The principal difference between them is the component values. Both PWAs share the same schematic.

There are three configurations of the Reference PWA: one each for NTSC, PAL-M, and PAL/SECAM standards. Placement of one jumper on the PAL/SECAM Reference PWA makes the difference between PAL and SECAM configuration. The logic level determined by this jumper is placed on the motherboard bus and makes the same distinction for the Mod/Demod PWA.

3-5 Heads and Timer Idlers

The edit erase and record/play (AST) heads and the timer idler assemblies differ between standards for 60- and 50-Hz primary power. Therefore, there are two configurations of heads and timer idlers: one for NTSC and PAL-M (60 Hz), and one for PAL/SECAM (50 Hz) standards.

3-6 Other Components

The Record Amplifier and Edit Erase PWA and the Preamplifier PWA are not included in the video kits. One configuration of each is common to all video standards.

3-7 Reference PWA

The following discussions are grouped by Reference PWA type: NTSC (1450346), PAL-M (1450363), and PAL/SECAM (1450356). Components and test points are identified with the card cage PWA number preceding the control or test point reference designation. For example, 2TP4 indicates test point 4 on PWA2, the Reference PWA, and 1C44 indicates capacitor 44 on PWA1, the Mod/Demod PWA.

The Reference PWA is composed of four principal circuits: input video processing, reference selector, color field 1 identifier, and monitor/auxiliary video circuits. The Reference PWA receives record video input from the Mod/Demod PWA and station reference video input from the I/O connector panel. The reference selector, under command of the control system microprocessor (CPU), selects one of them as machine reference and provides selected composite sync to the servo system. The color field 1 identifier, also under control of the control system CPU, looks at the selected video input and provides the color field 1 reference pulse to the servo system. The Reference PWA also contains demod video processing for the picture monitor. This circuitry consists of a phase-locked oscillator and sync reinsertion circuitry to provide sync in the monitor output through what is normally the dropout region. The Reference PWA control interface also serves the Mod/Demod PWA. All communication between Control and Mod/Demod PWAs passes through the Reference PWA.

3-8 NTSC Standard

3-9 Input Video Processing. NTSC input video processing circuits are shown in Figure 3-1.

Generation of video reference pulses begins with either of two video inputs to the VPR-80: record video at J9 or station reference video at J10 (on the I/O connector panel).

Record video input from J9 is applied to input amplifier 1U5 on the Mod/Demod PWA which clamps blanking level to zero volts. Record video output of 1U5 is routed to video selector switches through connector contact 15 on the Reference PWA. Video selection is made by the control system CPU on the basis of mode of operation (record, play, edit/nonedit) and what inputs are available at the I/O connector panel. See paragraph 3-10.

Output of 1U5 is also applied to sync stripper 1U14. Record video composite sync output of 1U14 is applied to the reference video detector on the Reference PWA through connector contact 17.

Reference video input from J10 (normally looped through the TBC) is applied to input amplifier 2U10-8 and low-pass filter 2L10, 2C39, and 2C40. Output of emitter follower 2Q2 is fed back through 2Q4 and 2Q16-6 to 2U10-12. Sampling switch 2Q4 is controlled by sync stripper 2U15-11 and back porch one-shot 2U21-13.

2R34 provides adjustment of 2U10 to ensure a 1.5 Vp-p signal at test point 2TP3. Conditioned reference video input is applied to video select switch 2U4-6.

Record video input at connector contact 15 is applied directly to video select switch 2U5-8. Selected video input (record or reference) is applied to the color/monochrome detector 2U3-8 and 2U26 and Gaussian low-pass filter 2L4—2L8 and 2C15—2C19. Adjustment of coil 2L11 ensures a maximum peak-to-peak color burst at the color/monochrome detector input (2TP23).

3-10 Reference Selector. The control system CPU is interrupted at vertical (field) rate. During this interrupt (INT 0), the control system CPU performs a long list of functions (see paragraph 6-36 in Section 6, Part II). One of the status checks it makes during INT 0 is polling the setting of REF SELECT switch 6S5 on the Control PWA. Settings of the REF SELECT switch are REF (station reference video input), INPUT (record video input), and AUTO (automatic selection depending on mode). Refer back to Table 3-6 in Section 3, Part I.

Selection of reference input by the control system CPU is shown in Table 3-2. If the REF SELECT switch is set to the REF position, and if both record video input and station reference video input are connected at J9 and J10 on the I/O connector panel, respectively, the control system CPU will select station reference input in both play and record modes. If station video reference input is absent (not connected at J10), the control system CPU will use the record video input as an alternate reference in both play and record modes. (SYSTEM indication **01** will be brought up for display in record mode.) If neither record video input nor station reference video input is connected, the CPU uses the oscillator in the reference pulse generator (AST Servo PWA) as reference in play mode. Naturally, with no record video input, record mode is impossible, and SYSTEM indication **03** is brought up for display.

If the REF SELECT switch is set to the INPUT position, and if both record video input and station reference video input are connected at J9 and J10 on the I/O connector panel, respectively, the control system CPU will select record video input in both play and record modes. If record video input is absent (not connected at J9), the control system CPU will use station reference video input as an alternate reference in both play and record modes. (SYSTEM indication **02** will be brought up for display in play mode.) If neither record video input nor station reference video input is connected, the CPU uses the oscillator in the reference pulse generator (AST Servo PWA) as reference in play mode. Naturally, with no record video input, record mode is impossible, and SYSTEM indication **03** is brought up for display.

If the REF SELECT switch is set to the AUTO position, and if both record video input and station reference video input are connected at J9 and J10 on the I/O connector panel, respectively, the control system CPU will select station reference input in play mode and record video input in record mode. If station video reference input is absent (not connected at J10), the control system CPU will use record video input as an alternate reference in play mode. If record video input is absent (not connected at J9), the control system CPU will use station reference video input as an alternate reference in record mode. If neither record video input nor station reference video input is connected, the CPU uses the oscillator in the reference pulse generator (AST Servo PWA) as reference in play mode. Naturally, with no record video input, record mode is impossible, and SYSTEM indication **03** is brought up for display.

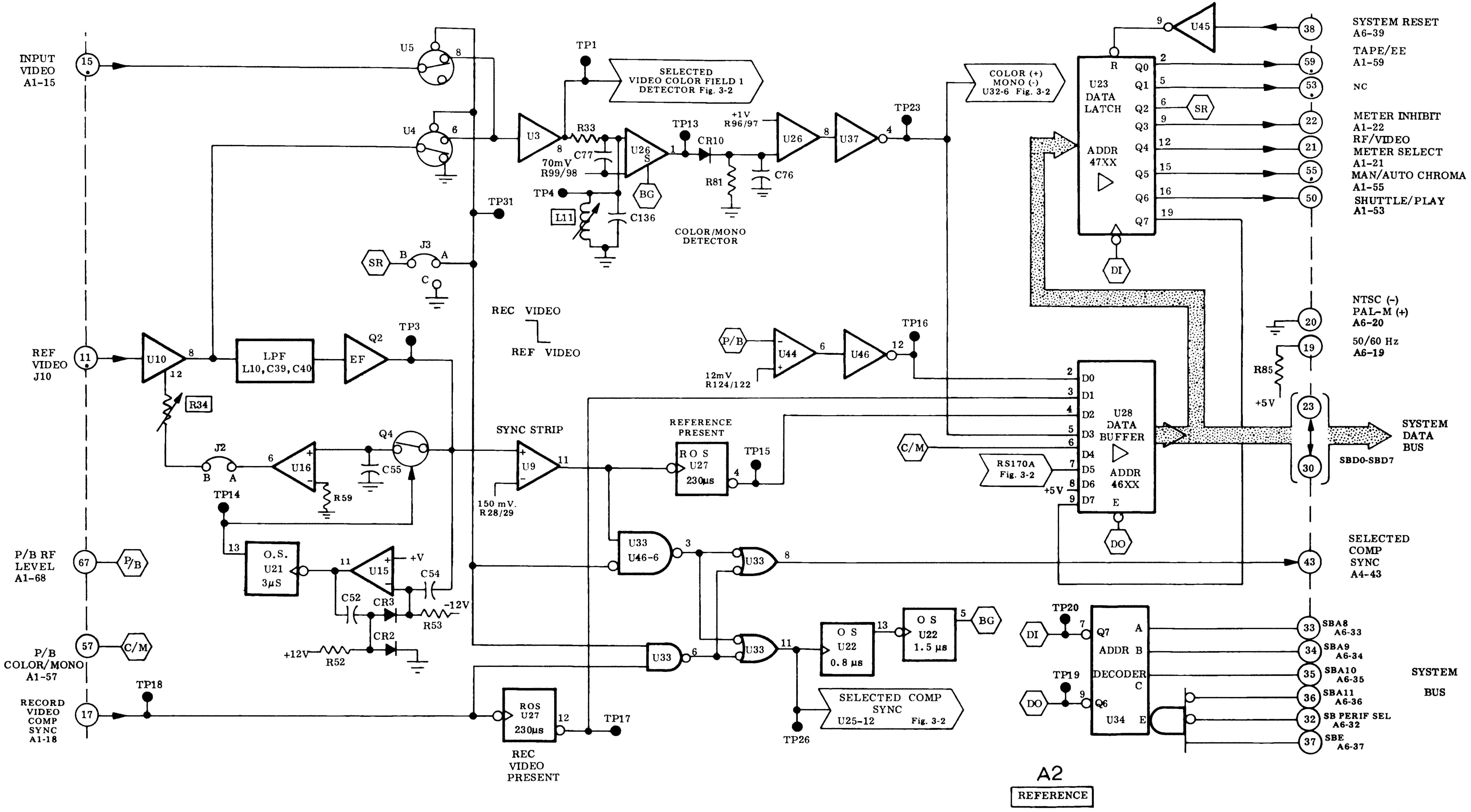


Figure 3-1.
Reference Selector PWA2 (NTSC)

The control system CPU coordinates selection of composite sync reference to be supplied to the reference pulse generator on the AST Servo PWA and to the color frame 1 identifier on the Reference PWA. It first looks at the setting of the REF SELECT switch. The CPU then enables an input data buffer on the Reference PWA so that it can detect which video inputs are present. Then, depending on current mode (play or record), it selects appropriate available reference input as shown in Table 3-2.

NTSC reference selector circuits are shown in Figure 3-1.

Table 3-2. Reference Selection

Ref Select Switch (6S5) Position	Mode	I/O Connector Panel Inputs		
		REF VIDEO IN (J10)	VIDEO IN (J9)	Neither Cable Installed
REF	Play	❶	❷	❸ (Internal Osc)
	Record	❶	❷ SYSTEM 01	Ⓧ SYSTEM 03
INPUT	Play	❷ SYSTEM 02	❶	❸ (Internal Osc)
	Record	❷	❶	Ⓧ SYSTEM 03
Auto	Play	❶	❷	❸ (Internal Osc)
	Record	❷	❶	Ⓧ SYSTEM 03

❶ = Primary Reference
❷ = Secondary Reference
❸ = Tertiary Reference
Ⓧ = Record Mode Aborted

Record video composite sync (2TP18) enters the Reference PWA at connector contact 17 and is applied to detector one-shot 2U27-12. The one-shot output (2TP17) is presented to the D1 input of input data buffer 2U28. The reference video signal from J10 enters the Reference PWA at connector contact 11. It is put through feedback clamp 2U10, low-pass filter 2L10, 2C39, and 2C40, and is applied to sync stripper 2U9. With chroma removed, output of 2U9 triggers detector one-shot 2U27-4. This output (2TP15) is applied to the D2 input of data buffer 2U28.

When the control system CPU enables input data buffer 2U28 on a read cycle (decoded address 46XX), the following information is placed on the system data bus: presence or absence of playback rf, record video composite sync, and reference video, and whether record or playback video is color or monochrome. On the next write cycle the CPU clocks output data latch 2U23 (decoded address 47XX) which routes 5 bits of information to the Mod/Demod PWA (SBD0 and SBD3--SBD6). A 6th bit, SBD2, is the selected reference (SR) bit, and it governs selection of composite sync. The logic level of this bit controls composite sync selector switches 2U5-8 and 2U4-6 according to the setting of the REF SELECT switch, available inputs, and whether machine is in record or play mode.

If record video composite sync at connector contact 17 is selected, SR logic level is high. In this case, switches 2U5-8 and 2U4-6 are set as shown in Figure 3-1. Gate 2U33-6 is enabled, and gate 2U33-3 is inhibited.

Gate 2U33-6 allows record video composite sync to pass through gate 2U33-8 to the reference pulse generator on the AST Servo PWA. Input video at PWA connector contact 15 is applied to color burst detector 2U3, 2U26, and 2U37. The burst detector is controlled by the burst gate (BG) output of tandem one-shots 2U22-13 and 2U22-5. The burst detector output (high = color, low = monochrome) is routed to the D3 input of data buffer 2U28 and to the color field 1 identifier. Amplified input video from 2U3 (2TP1) and output of gate 2U33-11 (2TP26) are also supplied to the color field 1 identifier.

If composite sync is to be derived from reference video input, SR logic level is low. In this case, switches 2U5-8 and 2U4-6 are thrown (opposite to settings shown in Figure 3-1). Gate 2U33-3 is enabled, and gate 2U33-6 is inhibited.

Gate 2U33-3 allows composite sync derived from reference video to pass through gate 2U33-8 to the reference pulse generator on the AST Servo PWA. Amplified reference video at 2U10-8 is applied to color burst detector 2U3, 2U26, and 2U37. The burst detector output is routed to input data buffer 2U28 and to the color field 1 identifier. Amplified reference video from 2U3 (2TP1) and the output of gate 2U33-11 (2TP26) are also supplied to the color field 1 identifier.

3-11 Color Field 1 Identifier. NTSC color field 1 identifier circuits are shown in Figure 3-2.

For minimum interference between line rate (H) and color subcarrier frequency (Fsc), subcarrier frequency is determined by the formula: Fsc = 455/2(H).

H = 15.734 kHz; therefore Fsc = 3.579545 MHz. (H is rounded off to 15.7 kHz, and Fsc is rounded off to 3.58 MHz.)

There are 227.5 cycles of subcarrier on every line (Fsc/H). This causes a half-cycle offset or 180° per line. Therefore, in-phase relation is achieved on every other line or at a H/2 (7.8 kHz) rate. Since there are 262.5 cycles of 7.8 kHz in one frame, only one field in four has 7.8 kHz and the 30-Hz frame rate coincident. The color field 1 identifier detects this coincidence and generates the color field identification pulse which is sent to the control track signal generator in the servo system. Control track logic is covered in Section 5, Part II, of this manual.

The selected composite sync signal from reference selector gate 2U33-11 (Figure 3-1) triggers one-shot 2U25-12. The one-shot output (delayed H-rate edges) clocks divide-by-two flip-flop 2U36-5 which generates the 7.8-kHz (H/2) switching of phase switch 2U18. The phase of color subcarrier alternates 180° on every line with respect to the leading edge of sync. Switch 2U18 is driven by 7.8-kHz (H/2) square waves. This switches the phase of the subcarrier so that it will have the same phase relationship on every line. Sampling of the subcarrier by horizontal sync is done in diode bridge 2U24. The dc-level sample is stored in 2C85.

Selected video from 2U2 is applied to video switches 2U8-13 and 2U8-2. Switch 2U8-13 samples the video blanking level (at back porch time), and switch 2U8-2 samples the video sync level (at sync tip time). The stored dc level of samples taken by these two switches is divided in half and buffered by 2U20. Therefore, the dc level at test point 2TP12 is midway between blanking level and sync tip. This level is fed to H-sync slicer 2U19, pin 2. Selected video is applied to slicer 2U19, pin 13. When the leading edge of sync at pin 13 equals the dc level at pin 2 (leading edge of sync), transformer 2T2 is energized, making a narrow horizontal rate pulse used by 2U24 to sample the color subcarrier.

The resultant detected dc level can vary between ±1.5V at 2C85. This voltage is amplified to ±5V by 2U48 and routed to 2U29-6 which is used as a comparator with hysteresis. Output of 2U48-6 is also routed to the RS-170A window detector circuit (2U50) which is calibrated so that if input ScH phase is within RS-170A specifications, LED indicator 2DS1 will light. This information is also routed to the control system CPU via input data buffer 2U28 (Figure 3-1).

The phase of the 7.8-kHz signal from flip-flop 2U36 is controlled at exclusive OR-gate 2U31-8 by the polarity of the subcarrier wave at the 50% point of the leading edge of horizontal sync. The detected level at 2C85 trips comparator 2U29-6 (via 2U24-8), deciding the phase of the 7.8-kHz output of exclusive OR-gate 2U31-8. This 7.8-kHz output is used to gate every other frame pulse (received at PWA connector contact 40 from the AST Servo PWA), producing the color frame identification pulse at gate 2U32-8. Gate output is routed to the servo system where it is incorporated in control track generation for record video.

Comparator 2U29 has switchable hysteresis which is the dc equivalent of 45° of a subcarrier cycle. For initial color frame recognition this is made inoperative by one-shot 2U45-5 and switch 2U18. One-shot 2U45-5 is triggered one second after any change of status that might affect the video input (ScH) phase relationship. It is also triggered one second after each power-up sequence is completed. Status change is detected by 2U47-1/-7 which monitors the detected ScH phase and 2U55

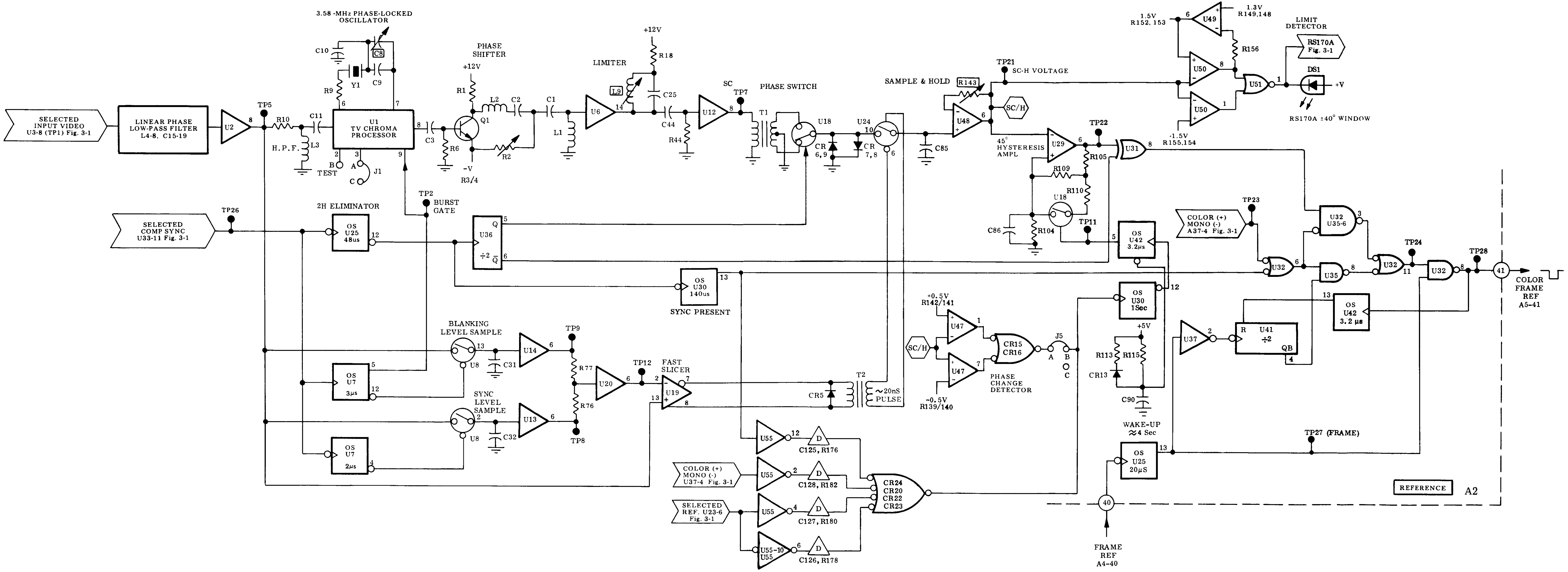


Figure 3-2.
Color Field 1 Identifier—PWA2 (NTSC)

which monitors the reference selector (Figure 3-1). Differentiator outputs trigger a five-input diode OR gate. The OR-gate output triggers the one-second one-shot 2U30-12.

One-shot 2U30-12 is triggered by sync detector one-shot 2U30-13 when video returns from absence, by a color/monochrome signal from 2U37-4 (Figure 3-1) via 2U55-2, by the selected reference level from output data latch 2U23-6 (Figure 3-1) via 2U55-4/-5, or when a change in phase relationship has been detected by 2U47-1/-7.

Divide-by-two counter 2U41-4 is clocked by 20-μs frame rate edges from 2U25-13. The counter provides a flywheeled alternative gate pulse to 2U32-8 used when input video is monochrome.

3-12 Monitor/Auxiliary Video. NTSC monitor/auxiliary video circuits are shown in Figure 3-3.

The monitor video circuit routes demod video to the picture monitor. It samples and holds sync tip level and reinserts sync in the video wave train under timing control of servo vertical and vertical blanking inputs from the servo system and an internal phase-locked loop pulse generator. The auxiliary video circuit routes either demod video (with reinserted sync) or auxiliary video input from the accessory character generator to the picture monitor. Picture monitor video input switching is controlled by input from the Accessory PWA.

Demod video from the Mod/Demod PWA enters the Reference PWA at connector contact 83. It is first applied to the unity gain amplifier composed of 2Q9, 2Q10, and 2Q11. The amplifier provides compensation for frequency response and gain losses. Amplifier output is routed to one side of video switch 2U56-2. It is also routed to one side of sync tip sample-and-hold switch 2Q8.

Demod composite sync (ref) from the Mod/Demod PWA enters the Reference PWA at connector contact 71. It triggers sync tip sample pulse generator one-shot 2U53-13. The one-shot output samples the sync tip level by turning on 2Q8. The dc level is stored in 2C123 and applied to the noninverting input of 2U54-7. The demod sync level output of 2U54-7 is furnished through 2U54-1 and PWA connector contact 79 to the Mod/Demod PWA where it is used in autochroma circuits. The demod sync level output of 2U54-7 is also applied to one side of sync insert switch 2Q7. During the dropout interval video switch 2U56-2 opens, cutting off video to the picture monitor. At the same time switch 2Q7 closes, reinserting vertical sync derived from demod composite sync.

Switch 2U56-2 is driven by output of gate 2U40-11 which will be high (switch open) during the vertical blanking pulse or for 198 μs after the servo vertical pulse is received from the AST Servo PWA.

Sync reinsertion switch 2Q7 is turned on (closed) by a phase-locked loop pulse generator composed of VCO 2U45, dividers 2U43 and 2U36, and one-shot 2U38-13.

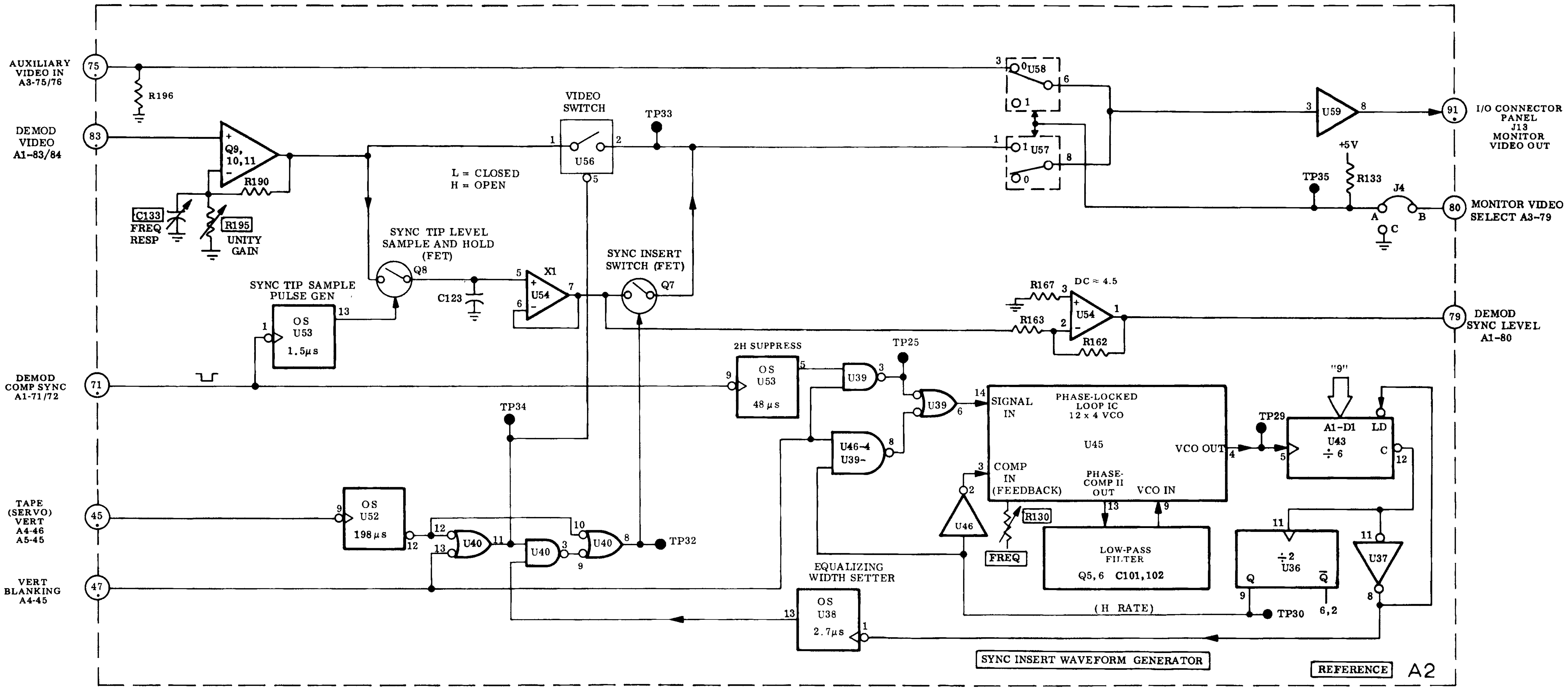


Figure 3-3.
Monitor/Auxiliary Video—PWA2 (NTSC)

Demod composite sync input is applied through 2H eliminator one-shot 2U53-5 to one input of gate 2U39-3. The gate is enabled by the vertical blanking input. Gate output is applied to the signal input of VCO 2U45. The VCO output is 12 x H (2TP29). VCO output is divided-by-6 by counter 2U43-12. Buffered 2H output triggers one-shot 2U38-13. The 2.7-µs one-shot output is an equalizing width setter for driving sync insert switch 2Q7. The 2H output of 2U43-12 is further divided to H by 2U36-3 which is fed back to complete the phase-locked loop.

Sync reinsertion switch 2Q7 is also turned on by the tape (servo) vertical input from the playback sync processor (PWA connector contact 45). The servo vertical input triggers one-shot 2U52-12. The 198-µs one-shot output passes through gates 2U40-11/-3/-8 and closes switch 2Q7. One-shot output is a broad vertical pulse to which the picture monitor can lock.

Auxiliary video input from PWA card cage slot 3 (Auxiliary PWA, i.e., character generator) enters the Reference PWA at connector contact 75. Auxiliary video input is applied to one side of video switch 2U58-6. Demod video (with sync reinserted) is routed through video switch 2U57-8 to the picture monitor via the MONITOR VIDEO OUT connector on the VPR-80 I/O connector panel.

The monitor video select logic level from PWA slot 3 enters the Reference PWA at connector contact 80 and is routed to the driving input of video switches 2U57-8 and 2U58-6. When the select logic level goes low, demod video output is grounded by switch 2U57-8, and auxiliary video input is routed to the picture monitor through video switch 2U58-6 and 2U59-8. When the monitor video select logic level is high, auxiliary video input is grounded and demod video is routed to the picture monitor through 2U59-8.

3-13 PAL-M Standard

3-14 **Input Video Processing.** PAL-M input video processing circuits are shown in Figure 3-4.

Generation of video reference pulses begins with either of two video inputs to the VPR-80: record video at J9 or station reference video at J10 (on the I/O connector panel).

Record video input from J9 is applied to input amplifier 1U5 on the Mod/Demod PWA which clamps blanking level to zero volts. Record video output of 1U5 is routed to video selector switches through connector contact 15 on the Reference PWA. Video selection is made by the control system CPU on the basis of mode of operation (record, play, edit/nonedit) and what inputs are available at the I/O connector panel. Refer to Table 3-2.

The output of 1U5 is also applied to sync stripper 1U14. The record video composite sync output of 1U14 is applied to the reference video detector on the Reference PWA through connector contact 17.

The reference video input from J10 (normally looped through the TBC) is applied to input amplifier 2U11-8 and low-pass filter 2L11, 2C35, and 2C36. Output of

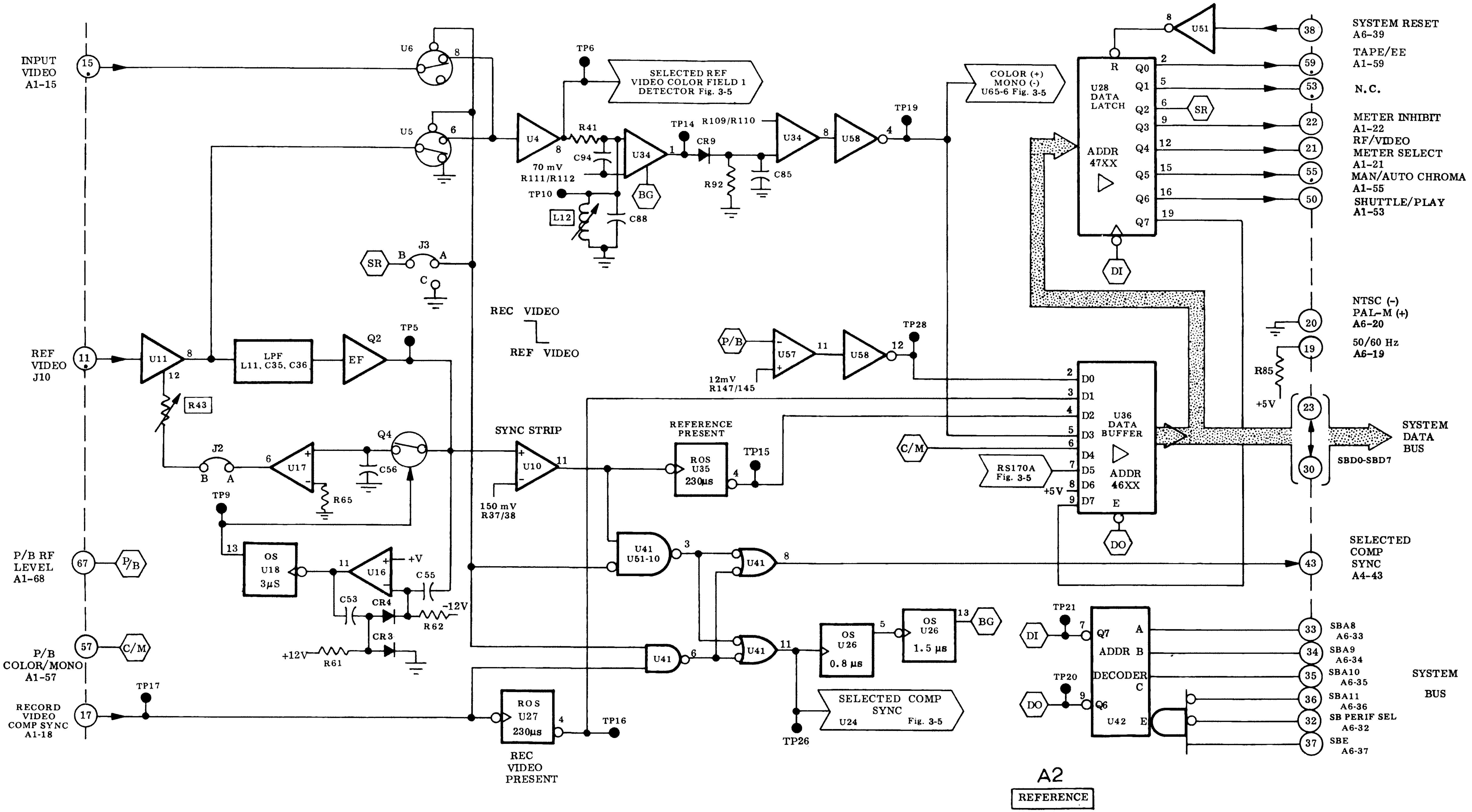


Figure 3-4.
Reference Selector—PWA2 (PAL-M)

emitter follower 2Q2 is fed back through 2Q4 and 2Q17-6 to 2U11-12. Sampling switch 2Q4 is controlled by sync stripper 2U16-11 and back porch one-shot 2U18-13.

2R43 provides adjustment of 2U11 to ensure a zero-volt back porch level output and a 1.5-Vp-p signal at test point 2TP5. Conditioned reference video input is applied to video select switch 2U5-6.

Record video input at connector contact 15 is applied directly to video select switch 2U6-8. Selected video input (record or reference) is applied to the color/monochrome detector 2U4-8 and 2U34 and Gaussian low-pass filter 2L5—2L9 and 2C16—2C20. Adjustment of coil 2L12 ensures a maximum peak-to-peak color burst at the color/monochrome detector input (2TP19).

3-15 **Reference Selector.** PAL-M reference selector circuits are shown in Figure 3-4.

Record video composite sync (2TP17) enters the Reference PWA at connector contact 17 and is applied to detector one-shot 2U27-4. The one-shot output (2TP16) is presented to the D1 input of input data buffer 2U36. The reference video signal from J10 enters the Reference PWA at connector contact 11. It is put through feedback clamp 2U11, low-pass filter 2L10, 2C35, and 2C36, and is applied to sync stripper 2U10. With chroma removed, output of 2U10 triggers detector one-shot 2U35-4. This output (2TP15) is applied to the D2 input of data buffer 2U36.

When the control system CPU enables input data buffer 2U36 on a read cycle (decoded address 46XX), the following information is placed on the system data bus: presence or absence of playback rf, of record video composite sync, and of reference video, and whether record or playback video is color or monochrome. On the next write cycle the CPU clocks output data latch 2U28 (decoded address 47XX) which routes 5 bits of information back to the video system (SBD0 and SBD3—SBD6). A 6th bit, SBD2, is the selected reference (SR) bit, and it governs selection of composite sync. The logic level of this bit controls composite sync selector switches 2U6-8 and 2U5-6 in accordance with the setting of the REF SELECT switch, available inputs, and whether in record or play mode.

If record video composite sync at connector contact 17 is selected, SR logic level is high. In this case, switches 2U5-8 and 2U4-6 are set as shown in Figure 3-4. Gate 2U41-6 is enabled, and gate 2U41-3 is inhibited.

Gate 2U41-6 allows record video composite sync to pass through gate 2U41-8 to the reference pulse generator on the AST Servo PWA. Input video at PWA connector contact 15 is applied to color burst detector 2U4, 2U34, and 2U58. The burst detector is controlled by burst gate (BG) output of tandem one-shots 2U26-5 and 2U26-13. Burst detector output (high = color, low = monochrome) is routed to the D3 input of data buffer 2U36 and to the color field 1 identifier. Amplified input video from 2U4 (2TP6) and the output of gate 2U41-11 (2TP11) are also supplied to the color field 1 identifier.

If composite sync is to be derived from reference video input, SR logic level is low. In this case, switches 2U6-8 and 2U5-6 are thrown (opposite to settings shown in Figure 3-4). Gate 2U41-3 is enabled, and gate 2U41-6 is inhibited.

Gate 2U41-3 allows composite sync derived from reference video to pass through gate 2U41-8 to the reference pulse generator on the AST Servo PWA. Amplified reference video at 2U11-8 is applied to color burst detector 2U4, 2U34, and 2U58. Burst detector output is routed to input data buffer 2U36 and to color field 1 identifier. Amplified reference video from 2U4 (2TP6) and output of gate 2U41-11 (2TP11) are also supplied to the color field 1 identifier.

3-16 Color Field 1 Identifier. PAL-M color field 1 identifier circuits are shown in Figure 3-5.

For minimum interference between line rate (H) and color subcarrier frequency (Fsc), subcarrier frequency is determined by the formula: Fsc = 909/4(H).

H = 15.734 kHz; therefore Fsc = 3.575611 MHz. (H is rounded off to 15.7 kHz, and Fsc is rounded off to 3.58 MHz.)

There are 283.75 cycles of subcarrier on every line (Fsc/H), causing a quarter-cycle offset, or 90° per line. Therefore, in-phase relation is achieved on every fourth line, or at a H/4 (3.9-kHz) rate. Since there are 131.25 cycles of 3.9 kHz in one frame, only one field in eight has 3.9 kHz and the 30-Hz frame rate coincident. The color field 1 identifier detects this coincidence and generates the color field identification pulse which is sent to the control track generator in the servo system. The control track generator is covered in Section 5, Part II.

Selected video from 2U3-8 is applied to TV chroma processor 2U2 and the 3.58-MHz phase-locked oscillator composed of 2Y1, 2C10, 2C11, and 2C12. Selected video is also applied to one side of video switches 2U25-2 and 2U25-13 and to the noninverting input of H-sync slicer 2U30-7/-8.

The selected composite sync signal from reference selector gate 2U41-11 (Figure 3-4) triggers one-shots 2U24-4/-13 and 2U24-12. One-shot outputs (delayed H-rate edges) are routed to the horizontal key input of TV chroma processor 2U2 and to switching inputs of switches 2U25-2 and 2U25-13.

Identification (H) output of chroma processor 2U2 (pin 13) is applied to H/2 filter 2U9. Voltage and phase of the H/2 filter output (2TP3) are calibrated by 2R31 and 2R30. H/2 output of 2U9 is applied to slicer 2U8. Slicer output at 2U8-9 drives 90° phase switch 2U13. H/2 output at 2U8-11 (2TP4) clocks divide-by-two flip-flop 2U20-6/-5. H/4 output at 2U20-6 drives 180° phase switch 2U15. H/4 output at 2U20-5 is applied to gate 2U45-3.

The 3.58-MHz output of chroma processor 2U2 is applied to current source 2Q1. 2R9 at the emitter output provides ScH phase calibration. Adjustment of 2L1 provides maximum peak-to-peak subcarrier signal.

Analog switch 2U13-4/-16 switches between two phases of subcarrier 90° apart. RC network 2R55/2C47 advances the subcarrier phase, and LC network 2L11/2C46 retards the subcarrier phase. Switch 2U13 is driven by the H/2 output of slicer 2U8-9.

Following the 90° correction provided by switch 2U13, the phase of color subcarrier alternates 180° every pair of lines with respect to the leading edge of sync. Switch 2U15-4/-16 is driven by 3.9-kHz (H/4) square waves, switching the phase of the subcarrier so that it will have the same phase relationship on every line. Sampling of the subcarrier by horizontal sync is done in diode bridge 2U22 where a dc voltage is developed and 2C69 charges to this value.

Selected video from 2U3 is applied to video switches 2U25-2 and 2U25-13. Switch 2U25-2 samples the video blanking level (at back porch time), and switch 2U25-13 samples video sync level (at sync tip time). Stored dc level of samples taken by these two switches is divided in half and buffered by 2U32 and 2U33. Therefore, the dc level at test point 2TP13 is midway between blanking level and sync tip. This level is fed to H-sync slicer 2U30, pin 2. Selected video is applied to slicer 2U30, pin 13. When the leading edge of sync at pin 13 equals the dc level at pin 2 (leading edge of sync), transformer 2T2 is energized, making a narrow horizontal rate pulse used by 2U22 to sample the color subcarrier.

The dc sample of subcarrier in 2C69 can vary between ±1.5V. This voltage is amplified to ±5V by 2U61-7. 2R152 provides ScH voltage calibration. Output of 2U61-7 is routed to 2U29-6 which is used as a comparator with hysteresis. Output of 2U61-7 is also routed to the ScH phase window detector circuit (2U63) which is calibrated so that if input ScH phase is within ±40° of specification, LED indicator 2DS1 will light. This information is also routed to the control system CPU via input data buffer 2U36 (Figure 3-4).

The phase of the 3.9-kHz (H/4) signal from flip-flop 2U20 is controlled at exclusive OR-gate 2U44-3 by the polarity of the dc stored in 2C69. Detected level at 2U61-7 trips comparator 2U29-6 deciding the phase of the 3.9-kHz output of exclusive OR-gate 2U44-3. This 3.9-kHz output is used to gate every fourth frame pulse (received at PWA connector contact 40 from the AST Servo PWA), producing the color frame identification pulse at gate 2U45-8. Gate output is routed to the servo system where it is incorporated in control track generation for record video.

Comparator 2U29 has switchable hysteresis which is the dc equivalent of 45° of a subcarrier cycle. For initial color frame recognition this is made inoperative by one-shot 2U69-13 and switch 2U37. One-shot 2U69-13 is triggered one second after any change of status that might affect the video input (ScH) phase relationship. It is also triggered one second after each power-up sequence is completed. Status change is detected by 2U60-1/-7 which monitors detected ScH phase, and 2U68 which monitors the reference selector (Figure 3-4). Differentiator outputs trigger a five-input diode OR gate. OR-gate output triggers one-second one-shot 2U69-12.

One-shot 2U69-12 is triggered by sync detector one-shot 2U43-13 when video returns from absence, by a color/monochrome signal from 2U58-4 (Figure 3-4) via

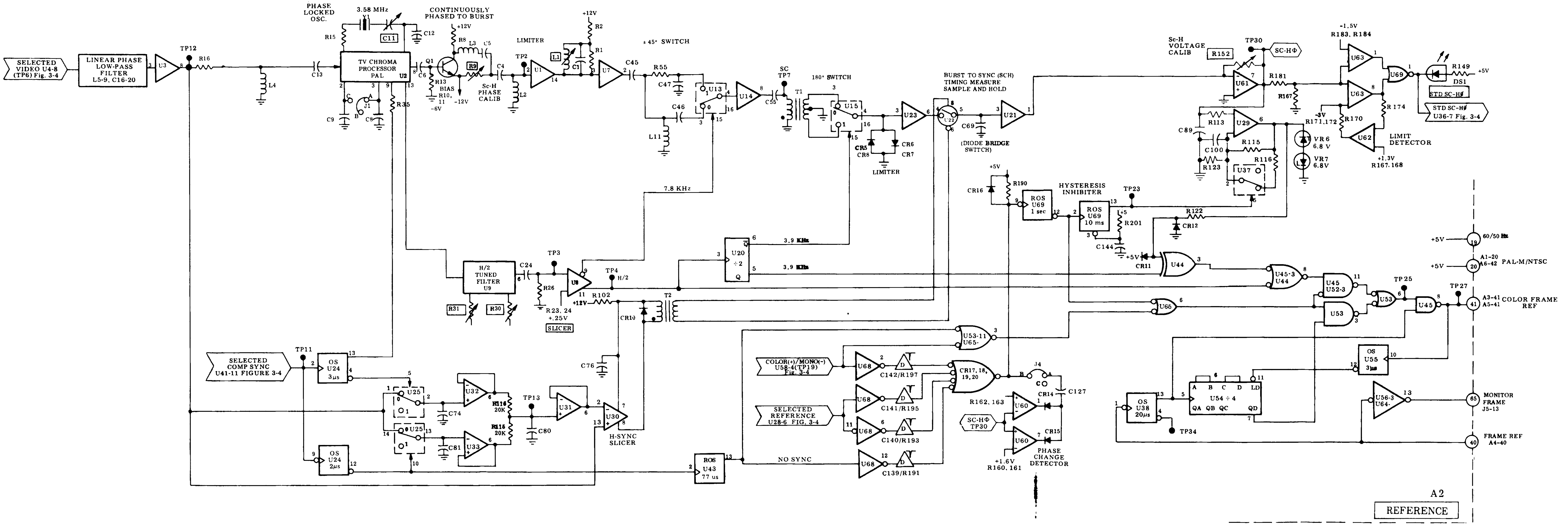


Figure 3-5.
Color Field 1 Identifier—PWA2 (PAL-M)

2U68-2, by the selected reference level from output data latch 2U28-6 (Figure 3-4) via 2U68-4/-6, or when a change in phase relationship has been detected by 2U60-1/-7.

Divide-by-four counter 2U54-7 is clocked by 20-µs frame rate edges from 2U38-13. The counter provides a flywheeled alternative gate pulse to 2U45-8 which is used when input video is monochrome.

3-17 **Monitor/Auxiliary Video.** PAL-M monitor/auxiliary video circuits are shown in Figure 3-6.

The monitor video circuit routes demod video to the picture monitor. It samples and holds sync tip level and reinserts sync in the video wave train under timing control of servo vertical and vertical blanking inputs from the servo system and an internal phase-locked loop pulse generator. The auxiliary video circuit routes either demod video (with reinserted sync) or auxiliary video input from the accessory character generator to the picture monitor. Picture monitor video input switching is controlled by an input from the Accessory PWA.

Demod video from the Mod/Demod PWA enters the Reference PWA at connector contact 83. It is first applied to unity gain amplifier composed of 2Q9, 2Q10, and 2Q11. The amplifier provides compensation for frequency response and gain losses. Amplifier output is routed to one side of video switch 2U66-2. It is also routed to one side of sync tip sample-and-hold switch 2Q7.

Demod composite sync (ref) from the Mod/Demod PWA enters the Reference PWA at connector contact 71. It triggers sync tip sample pulse generator one-shot 2U46-13. The one-shot output samples the sync tip level by turning on 2Q7. The dc level is stored in 2C131 and applied to the noninverting input of 2U67-7. The demod sync level output of 2U67-7 is furnished through 2U67-1 and PWA connector contact 79 to the Mod/Demod PWA where it is used in autochroma circuits. The demod sync level output of 2U67-7 is also applied to one side of sync insert switch 2Q8. During the dropout interval video switch 2U66-2 opens, cutting off video to the picture monitor. At the same time switch 2Q8 closes, reinserting vertical sync derived from demod composite sync.

Switch 2U66-2 is driven by the output of gate 2U59-11 which will be high (switch open) during the vertical blanking pulse or for 164 µs after the servo vertical pulse is received from the AST Servo PWA.

Sync reinsertion switch 2Q8 is turned on (closed) by a phase-locked loop pulse generator composed of VCO 2U39, dividers 2U40 and 2U48, and one-shot 2U49-13.

The demod composite sync input is applied through 2H eliminator one-shot 2U46-5 to one input of gate 2U50-3. The gate is enabled by the vertical blanking input. Gate output is applied to the signal input of VCO 2U39. The VCO output is 12 x H (2TP18). The VCO output is divided by six by counter 2U40-12. Buffered 2H output triggers one-shot 2U49-13. The 2.7-µs one-shot output is an equalizing width setter for driving sync insert switch 2Q8. The 2H output of 2U40-12 is further divided to H by 2U48-3 which is fed back to complete the phase-locked loop.

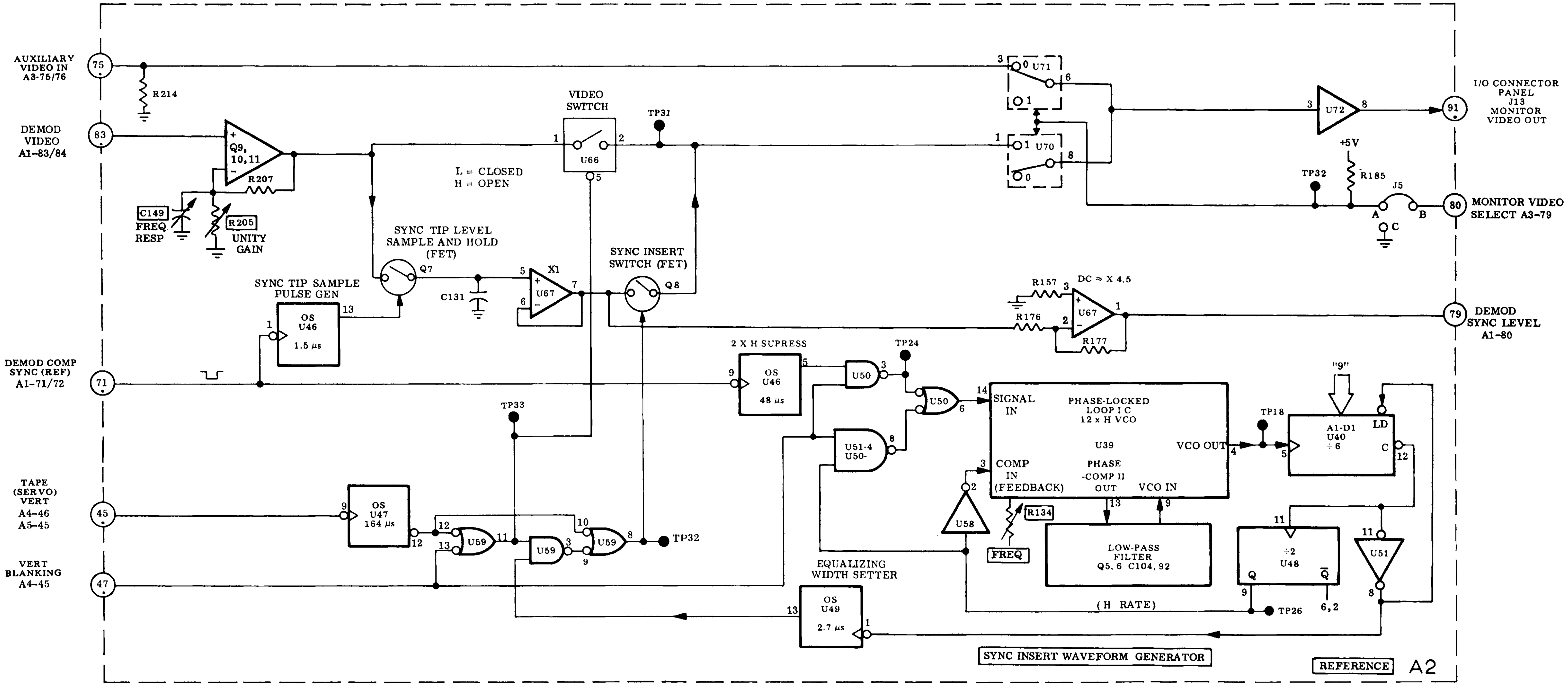


Figure 3-6.
Monitor/Auxiliary Video—PWA2 (PAL-M)

Sync reinsertion switch 2Q8 is also turned on by the tape (servo) vertical input from the playback sync processor (PWA connector contact 45). The servo vertical input triggers one-shot 2U47-12. The 164-µs one-shot output passes through gates 2U59-11/-3/-8 and closes switch 2Q8. The one-shot output is a broad vertical pulse to which the picture monitor can lock.

Auxiliary video input from PWA card cage slot 3 (Auxiliary PWA, i.e., character generator) enters the Reference PWA at connector contact 75. Auxiliary video input is applied to one side of video switch 2U71-6. Demod video (with sync reinserted) is routed through video switch 2U70-8 to the picture monitor via the MONITOR VIDEO OUT connector on the VPR-80 I/O connector panel.

The monitor video select logic level from PWA slot 3 enters the Reference PWA at connector contact 80 and is routed to the driving input of video switches 2U70-8 and 2U71-6. When the select logic level goes low, demod video output is grounded by switch 2U70-8, and auxiliary video input is routed to the picture monitor through video switch 2U71-6 and 2U72-8. When the monitor video select logic level is high, auxiliary video input is grounded and demod video is routed to the picture monitor through 2U72-8.

3-18 PAL/SECAM Standards

3-19 **Input Video Processing.** PAL/SECAM input video processing circuits are shown in Figure 3-7.

Generation of video reference pulses begins with either of two video inputs to the VPR-80: record video at J9 or station reference video at J10 (on the I/O connector panel).

Record video input from J9 is applied to input amplifier 1U5 on the Mod/Demod PWA which clamps the blanking level to zero volts. Record video output of 1U5 is routed to video selector switches through connector contact 15 on the Reference PWA. Video selection is made by the control system CPU on the basis of mode of operation (record, play, edit/nonedit) and what inputs are available at the I/O connector panel. Refer to Table 3-2.

The output of 1U5 is also applied to sync stripper 1U14. The record video composite sync output of 1U14 is applied to the reference video detector on the Reference PWA through connector contact 17.

The reference video input from J10 (normally looped through the TBC) is applied to input amplifier 2U12-8 and low-pass filter 2L11, 2C42, and 2C43. The output of emitter follower 2Q2 is fed back through 2Q4 and 2Q18-6 to 2U12-12. Sampling switch 2Q4 is controlled by sync stripper 2U17-11 and back porch one-shot 2U19-13.

2R45 provides adjustment of 2U12 to ensure a zero-volt back porch level output and a 1.5 Vp-p signal at test point 2TP7. Conditioned reference video input is applied to video select switch 2U5-6.

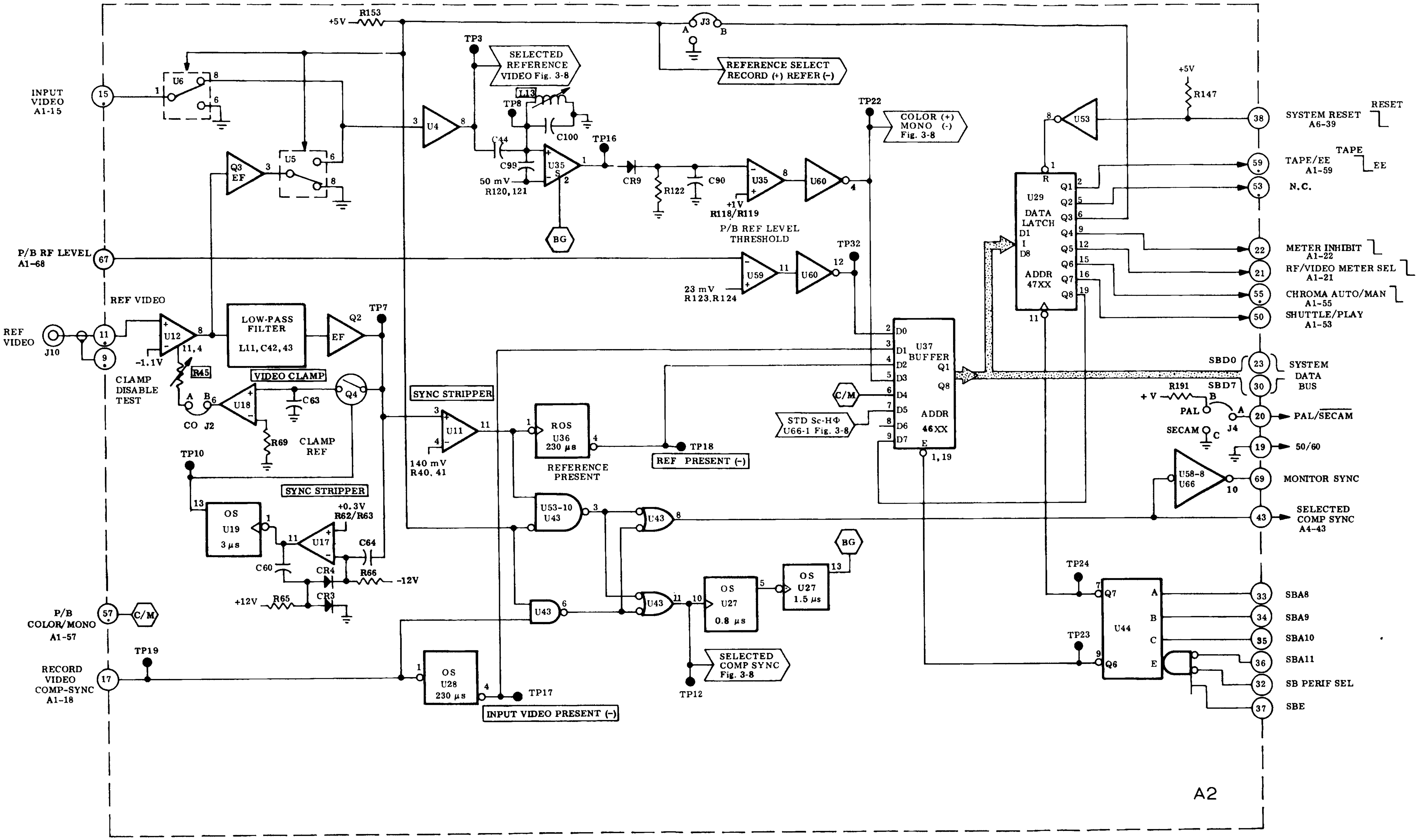


Figure 3-7.
Reference Selector—PWA2 (PAL/SECAM)

Record video input at connector contact 15 is applied directly to video select switch 2U6-8. Selected video input (record or reference) is applied to the color/monochrome detector 2U4-8 and 2U35 and Gaussian low-pass filter 2L5—2L9 and 2C17—2C21. Adjustment of coil 2L13 ensures a maximum peak-to-peak color burst at color/monochrome detector input (2TP22).

3-20 **Reference Selector.** PAL/SECAM reference selector circuits are shown in Figure 3-7.

Record video composite sync (2TP19) enters the Reference PWA at connector contact 17 and is applied to detector one-shot 2U28-4. One-shot output (2TP17) is presented to the D1 input of input data buffer 2U37. The reference video signal from J10 enters the Reference PWA at connector contact 11. It is put through feedback clamp 2U12, low-pass filter 2L11, 2C42, and 2C43, and applied to sync stripper 2U11. With chroma removed, output of 2U11 triggers detector one-shot 2U36-4. This output (2TP18) is applied to the D2 input of data buffer 2U37.

When the control system CPU enables input data buffer 2U37 on a read cycle (decoded address 46XX), the following information is placed on the system data bus: presence or absence of playback rf, of record video composite sync, and of reference video, and whether record or playback video is color or monochrome. On the next write cycle the CPU clocks output data latch 2U29 (decoded address 47XX) which routes 5 bits of information back to the video system (SBD0 and SBD3—SBD6). A 6th bit, SBD2, is the selected reference (SR) bit, and it governs the selection of composite sync. The logic level of this bit controls composite sync selector switches 2U6-8 and 2U5-6 in accordance with the setting of the REF SELECT switch, available inputs, and whether in record or play mode.

If record video composite sync at connector contact 17 is selected, the SR logic level is high. In this case, switches 2U6-8 and 2U5-6 are set as shown in Figure 3-7. Gate 2U43-6 is enabled, and gate 2U43-3 is inhibited.

Gate 2U43-6 allows record video composite sync to pass through gate 2U43-8 to the reference pulse generator on the AST Servo PWA. Input video at PWA connector contact 15 is applied to color burst detector 2U4, 2U35, and 2U60. The burst detector is controlled by the burst gate (BG) output of tandem one-shots 2U27-5 and 2U27-13. The burst detector output (high = color, low = monochrome) is routed to the D3 input of data buffer 2U37 and to the color field 1 identifier. Amplified input video from 2U4 (2TP3) and output of gate 2U43-11 (2TP12) are also supplied to the color field 1 identifier.

If composite sync is to be derived from the reference video input, the SR logic level is low. In this case, switches 2U6-8 and 2U5-6 are thrown (opposite to settings shown in Figure 3-7). Gate 2U43-3 is enabled, and gate 2U43-6 is inhibited.

Gate 2U43-3 allows composite sync derived from reference video to pass through gate 2U43-8 to the reference pulse generator on the AST Servo PWA. Amplified reference video at 2U12-8 is applied to color burst detector 2U4, 2U35, and 2U60. Burst detector output is routed to input data buffer 2U37 and to the color field 1 identifier. Amplified reference video from 2U4 (2TP3) and output of gate 2U43-11 (2TP12) are also supplied to the color field 1 identifier.

3-21 Color Field 1 Identifier. PAL/SECAM color field 1 identifier circuits are shown in Figure 3-8. The following explanation first covers PAL operation. Then differences in SECAM operation are covered.

Placement of jumper 2J4 determines the PAL (PAL-I) or SECAM configuration of the Reference PWA. When jumper 2J4 is placed in the A-B position, the PWA is in PAL configuration. The high logic level from the jumper connection throws analog switch 2U14-5/-9. The switch disconnects the output of SECAM frequency detector 2U10 and connects the identification (H) output of TV chroma processor 2U2 to H/2 filter 2U9.

For minimum interference between line rate (H) and PAL color subcarrier frequency (Fsc), subcarrier frequency is determined by the formula: Fsc = (1135/4 + 1/625)H.

H = 15.625 kHz; therefore Fsc = 4.433618 MHz. (H is rounded off to 15.6 kHz, and Fsc is rounded off to 4.43 MHz.)

There are 283.75 cycles of subcarrier on every line (Fsc/H), causing a quarter-cycle offset or 90° per line. Therefore, in-phase relation is achieved on every fourth line or at a H/4 (3.9-kHz) rate. Since there are 156.25 cycles of 3.9 kHz in one frame, only one field in eight has 3.9 kHz and the 25-Hz frame rate coincident. The color field 1 identifier detects this coincidence and generates the color field identification pulse which is sent to the control track generator in the servo system. The control track generator is covered in Section 5, Part II, of this manual.

Selected video from 2U4-8 is applied to TV chroma processor 2U2 and the 4.43-MHz phase-locked oscillator composed of 2Y1, 2C10, 2C11, and 2C12. Selected video is also applied to one side of video switches 2U26-2 and 2U26-13 and to noninverting input of H-sync slicer 2U31-7/-8.

The selected composite sync signal from reference selector gate 2U43-11 (Figure 3-7) triggers one-shots 2U25-4/-13 and 2U25-12. One-shot outputs (delayed H-rate edges) are routed to the horizontal key input of TV chroma processor 2U2 and to switching inputs of switches 2U26-2 and 2U26-13.

When the Reference PWA is in PAL configuration, the identification (H) output of chroma processor 2U2 (pin 13) is applied to H/2 filter 2U9 through analog switch 2U14-5/-9. Voltage and phase of the H/2 filter output (2TP4) are calibrated by 2R31 and 2R30. The H/2 output of 2U9 is applied to slicer 2U8. The H/2 slicer output at 2U8-9 drives 90° phase switch 2U14 and it also clocks divide-by-two flip-flop 2U21-6/-5. The H/2 output at 2U8-11 (2TP5) is applied to gate 2U47-3. The H/4 output at 2U21-5 drives 180° phase switch 2U16. The H/4 output at 2U21-6 is applied to gate 2U46-3.

The 4.43-MHz output of chroma processor 2U2 is applied to current source 2Q1. 2R9 at the emitter output provides ScH phase calibration. Adjustment of 2L1 provides maximum peak-to-peak subcarrier signal.

Analog switch 2U14-4/-16 switches between two phases of subcarrier 90° apart. RC network 2R58/2C53 advances the phase of subcarrier, and LC network 2L12/2C54 retards the subcarrier phase. Switch 2U14 is driven by the H/2 output of slicer 2U8-9.

Following the 90° correction provided by switch 2U14, the phase of color subcarrier alternates 180° every pair of lines with respect to the leading edge of sync. Switch 2U16-4/-16 is driven by 3.9-kHz (H/4) square waves. This switches the phase of the subcarrier so that it will have the same phase relationship on every line. Sampling of the subcarrier by horizontal sync is done in diode bridge 2U23. A 25-Hz sine wave is developed across 2C77. The sine wave is amplified and filtered by 2U30-1 and associated components so that a 10 Vp-p sine wave can be observed at test point 2TP20. 2R100 provides amplitude calibration of the sine wave.

The reference frame pulse from the AST Servo PWA enters the Reference PWA at connector contact 40. The reference frame pulse triggers one-shot 2U40. The 20-µs one-shot output at 2U40-4 closes switch 2U38-4, sampling the 25-Hz sine wave. 2C103 charges to the dc level of the 25-Hz sine wave at the time of the frame pulse.

Selected video from 2U3 is applied to video switches 2U26-2 and 2U26-13. Switch 2U26-2 samples video blanking level (at back porch time), and switch 2U26-13 samples the video sync level (at sync tip time). Stored dc level of the samples taken by these two switches is divided in half and buffered by 2U33 and 2U34. Therefore, the dc level at test point 2TP15 is midway between blanking level and sync tip. This level is fed to H-sync slicer 2U31, pin 2. Selected video is applied to slicer 2U31, pin 13. When the leading edge of sync at pin 13 equals the dc level at pin 2 (leading edge of sync), transformer 2T2 is energized, making a narrow horizontal rate pulse used by 2U23 to sample the color subcarrier.

The dc sample of subcarrier in 2C103 is applied to 2U30-7 which is used as a comparator with hysteresis. The dc voltage in 2C103 is also routed to the ScH phase window detector circuit (2U65) which is calibrated so that if input ScH phase is within ±40° of specification, LED indicator 2DS1 will light. This information is also routed to the control system CPU via input data buffer 2U37 (Figure 3-7).

The phase of the 3.9-kHz (H/4) signal from flip-flop 2U21 is controlled at exclusive OR-gate 2U46-3 by the polarity of the dc stored in 2C103. The stored level trips comparator 2U30-7, deciding the phase of the 3.9-kHz output of exclusive OR-gate 2U46-3. This 3.9-kHz output is used to gate every fourth frame pulse (received at PWA connector contact 40 from the AST Servo PWA), producing the color frame identification pulse at gate 2U47-8. Gate output is routed to the servo system where it is incorporated in control track generation for record video.

Comparator 2U30-7 has switchable hysteresis which is the dc equivalent of 45° of a subcarrier cycle. For initial color frame recognition this is made inoperative by one-shot 2U71-13 and switch 2U39. One-shot 2U71-13 is triggered one second after any change of status that might affect the video input (ScH) phase relationship. It is also triggered one second after each power-up sequence is

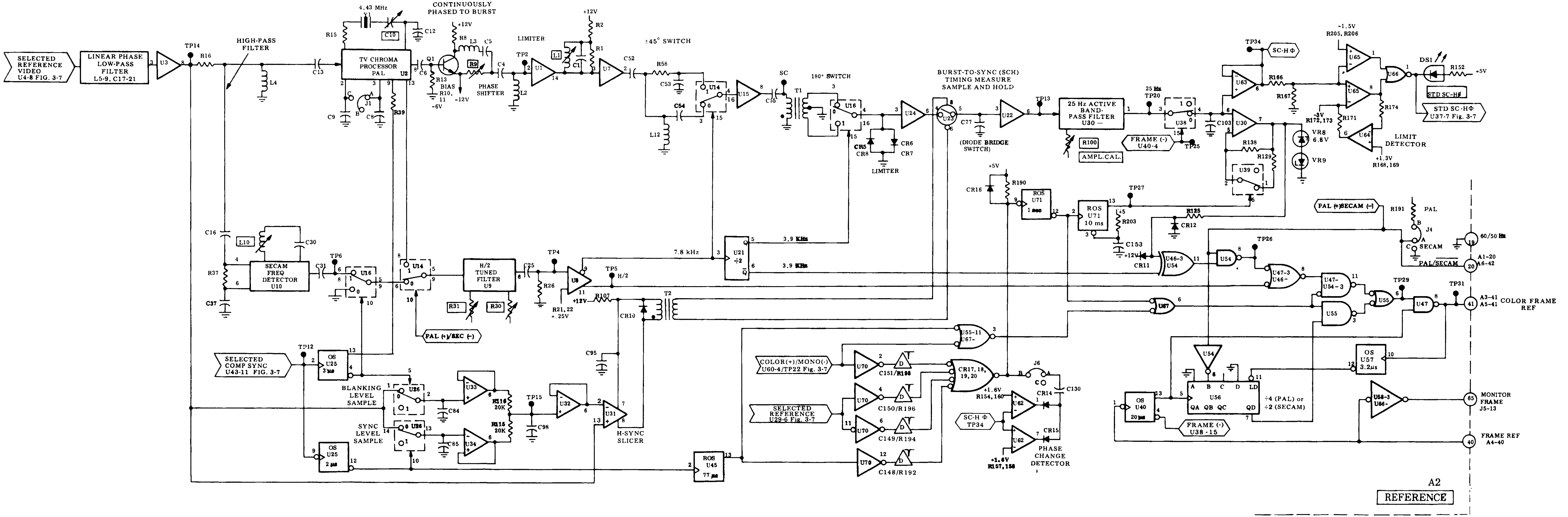


Figure 3-8. Color Field 1 Identifier— PWA2 (PAL/SECAM)

completed. Status change is detected by 2U62-1/-7 which monitors detected ScH phase and 2U70 which monitors the reference selector (Figure 3-7). Differentiator outputs trigger a five-input diode OR gate. OR-gate output triggers the one-second one-shot 2U71-12.

One-shot 2U71-12 is triggered by sync detector one-shot 2U45-13 when video returns from absence, by a color/monochrome signal from 2U60-4 (Figure 3-7) via 2U70-2, by the selected reference level from output data latch 2U29-6 (Figure 3-7) via 2U70-4/-6, or when a change in phase relationship has been detected by 2U62-1/-7.

In PAL operation, 2U56-7 is a divide-by-four counter, clocked by 20-µs frame rate edges from 2U40-13. The counter provides a flywheeled alternative gate pulse to 2U47-8 which is used when input video is monochrome.

When jumper 2J4 is placed in the A-C position, the PWA is in SECAM configuration. Logic level from the jumper is low, the H output of TV chroma processor 2U2 to 2U9 is disconnected, and the output of SECAM frequency detector 2U10 is applied through analog switch 2U16-5/-9 to H/2 filter 2U9.

Detector 2U10 produces color signals (R-Y) and (B-Y) on alternating lines. A 7.8-kHz (H/2) signal based on SECAM subcarrier is applied to H/2 filter 2U9 through analog switch 2U16-5/-9. The switch is driven by the blanking sample pulse from one-shot 2U25-4. The 7.8-kHz signal gates every other frame pulse at 2U47-8, producing the SECAM color frame identification pulse.

In SECAM operation the low logic level from jumper 2J4 causes buffer/inverter 2U54-6 to insert a count of 2 in 2U56-7. 2U56-7 thus becomes a divide-by-two counter which provides the flywheeled alternative gate pulse to 2U47-8.

3-22 **Monitor/Auxiliary Video.** PAL/SECAM monitor/auxiliary video circuits are shown in Figure 3-9.

The monitor video circuit routes demod video to the picture monitor. It samples and holds sync tip level and reinserts sync in the video wave train under timing control of servo vertical and vertical blanking inputs from the servo system and an internal phase-locked loop pulse generator. The auxiliary video circuit routes either demod video (with reinserted sync) or auxiliary video input from the accessory character generator to the picture monitor. Picture monitor video input switching is controlled by an input from the Accessory PWA.

Demod video from the Mod/Demod PWA enters the Reference PWA at connector contact 83. It is first applied to the unity gain amplifier composed of 2Q9, 2Q10, and 2Q11. The amplifier provides compensation for frequency response and gain losses. The amplifier output is routed to one side of video switch 2U68-2. It is also routed to one side of sync tip sample-and-hold switch 2Q7.

Demod composite sync (ref) from the Mod/Demod PWA enters the Reference PWA at connector contact 71. It triggers sync tip sample pulse generator one-shot 2U48-13. The one-shot output samples the sync tip level by turning on 2Q7. The dc level

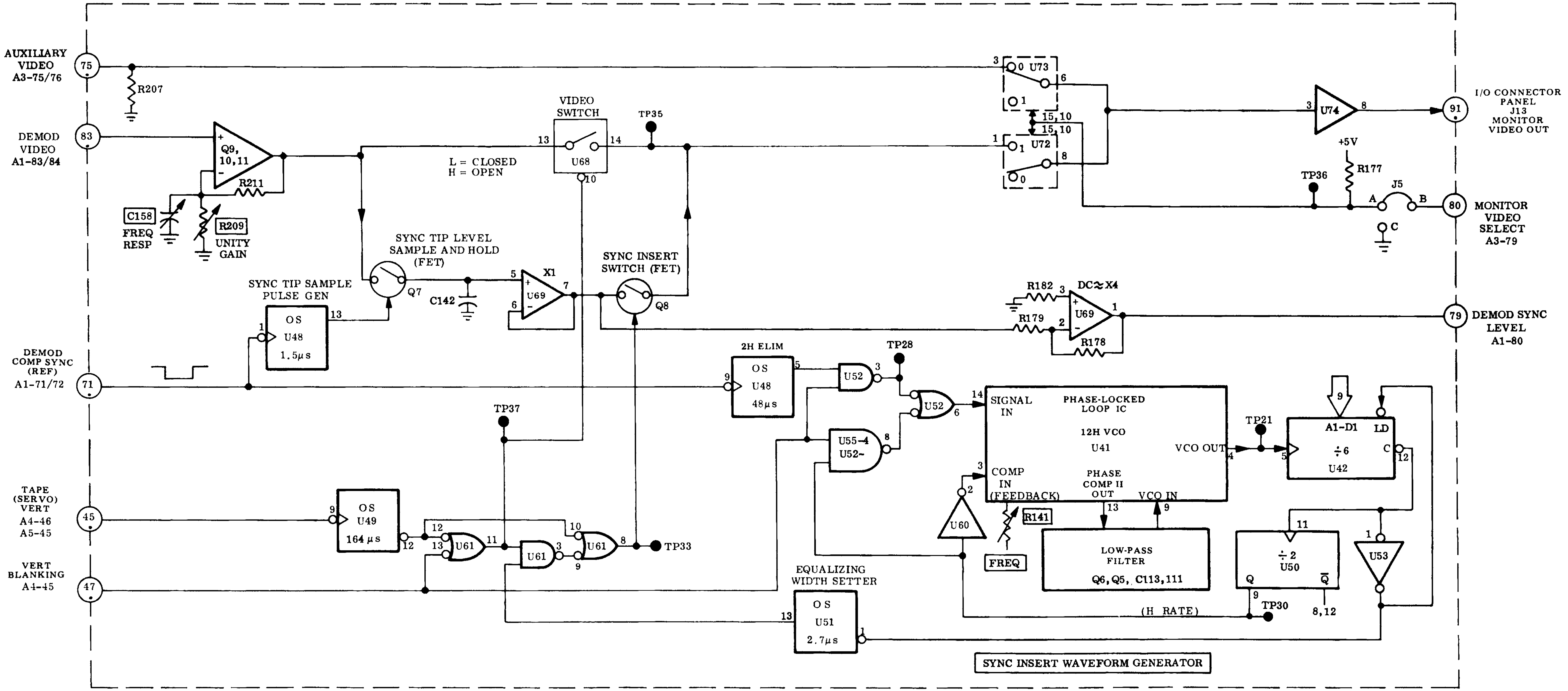


Figure 3-9.
Monitor/Auxiliary Video—PWA2 (PAL/SECAM)

is stored in 2C142 and applied to the noninverting input of 2U69-7. The demod sync level output of 2U69-7 is furnished through 2U69-1 and PWA connector contact 79 to the Mod/Demod PWA where it is used in autochroma circuits. The demod sync level output of 2U69-7 is also applied to one side of sync insert switch 2Q8. During the dropout interval video switch 2U68-2 opens, cutting off video to the picture monitor. At the same time switch 2Q8 closes, reinserting the vertical sync derived from demod composite sync.

Switch 2U68-2 is driven by the output of gate 2U61-11 which will be high (switch open) during the vertical blanking pulse or for 164 µs after the servo vertical pulse is received from the AST Servo PWA.

Sync reinsertion switch 2Q8 is turned on (closed) by a phase-locked loop pulse generator composed of VCO 2U41, dividers 2U42 and 2U50, and one-shot 2U51-13.

The demod composite sync input is applied through 2H eliminator one-shot 2U48-5 to one input of gate 2U52-3. The gate is enabled by the vertical blanking input. Gate output is applied to the signal input of VCO 2U41. The VCO output is 12 x H (2TP21). VCO output is divided by six by counter 2U42-12, and buffered 2H output triggers one-shot 2U51-13. The 2.7-µs one-shot output is an equalizing width-setter for driving sync insert switch 2Q8. The 2H output of 2U42-12 is further divided to H by 2U50-3 which is fed back to complete the phase-locked loop.

Sync reinsertion switch 2Q8 is also turned on by the tape (servo) vertical input from the playback sync processor (PWA connector contact 45). The servo vertical input triggers one-shot 2U49-12. The 164-µs one-shot output passes through gates 2U61-11/-3/-8 and closes switch 2Q8. The one-shot output is a broad vertical pulse to which the picture monitor can lock.

Auxiliary video input from PWA card cage slot 3 (Auxiliary PWA, i.e., character generator) enters the Reference PWA at connector contact 75. Auxiliary video input is applied to one side of video switch 2U73-6. Demod video (with sync reinserted) is routed through video switch 2U72-8 to the picture monitor via the MONITOR VIDEO OUT connector on the VPR-80 I/O connector panel.

The monitor video select logic level from PWA slot 3 enters the Reference PWA at connector contact 80 and is routed to the driving input of video switches 2U72-8 and 2U73-6. When the select logic level goes low, demod video output is grounded by switch 2U72-8, and auxiliary video input is routed to the picture monitor through video switch 2U73-6 and 2U74-8. When the monitor video select logic level is high, auxiliary video input is grounded and demod video is routed to the picture monitor through 2U74-8.

3-23 Jumpers

The Reference PWA is equipped with jumpers as aids to testing and troubleshooting. Also, a jumper on the PAL/SECAM Reference PWA determines PAL or SECAM configuration.

3-24 NTSC Reference PWA. Jumpers on the NTSC Reference PWA are listed in Table 3-3. Jumper locations on the PWA are shown in Figure 3-67 at the end of this section.

3-25 **PAL-M Reference PWA.** Jumpers on the PAL-M Reference PWA are listed in Table 3-4. Jumper locations on the PWA are shown in Figure 3-68 at the end of this section.

3-26 **PAL/SECAM Reference PWA.** Jumpers on the PAL/SECAM Reference PWA are listed in Table 3-5. Jumper locations on the PWA are shown in Figure 3-69 at the end of this section.

Table 3-3. NTSC Reference PWA Jumpers

Jumper	Position	Function
J1	A-B	Used in setup of color frame 3.58-MHz phase-locked oscillator. See paragraph 3-53.
	A-C	Normal. Refer to Figure 3-2.
J2	A-B	Normal. Refer to Figure 3-1.
	A-C	Disconnects clamp voltage from reference video input amplifier 2U10 for test.
J3	A-B	Normal. Control system CPU selects station reference video or record (input) video as servo video reference. Refer to Figure 3-1.
	A-C	Forces selection of station reference video as servo video reference.
	Removed	Forces selection of record (input) video as servo video reference.
J4	A-B	Normal. Connects monitor video select input to monitor video select switches (H = demod video, L = auxiliary video). Refer to Figure 3-3.
	A-C	Forces selection of demod video for monitor video output.
J5	A-B	Normal. Refer to Figure 3-2.
	A-C	Disconnects ScH error output of color frame detector from window detector for hysteresis inhibitor pulse former.

Table 3-4. PAL-M Reference PWA Jumpers

Jumper	Position	Function
J1	A-B	Used in setup of color frame 3.58-MHz phase-locked oscillator. See paragraph 3-62.
	A-C	Normal. Refer to Figure 3-5.
J2	A-B	Normal. Refer to Figure 3-4.

(Continued next page)

Table 3-4. PAL-M Reference Jumpers (Continued)

Jumper	Position	Function
J2	A-C	Disconnects clamp voltage from reference video input amplifier 2U11 for test.
		Disconnects clamp voltage from reference video input amplifier 2U11 for test.
J3	A-B	Normal. Control system CPU selects station reference video or record (input) video as servo video reference. Refer to Figure 3-4.
	A-C	Forces selection of station reference video as servo video reference.
	Removed	Forces selection of record (input) video as servo video reference.
J4	A-B	Normal. Refer to Figure 3-5.
	A-C	Disconnects ScH error output of color frame detector from the window detector for hysteresis inhibitor pulse former.
J5	A-B	Normal. Connects monitor video select input to monitor video select switches (H = demod video, L = auxiliary video). Refer to Figure 3-6.
	A-C	Forces selection of demod video for monitor video output.

Table 3-5. PAL/SECAM Reference PWA Jumpers

Jumper	Position	Function
J1	A-B	Normal. Refer to Figure 3-8.
	A-C	Used in setup of color frame 4.43-MHz phase-locked oscillator. See paragraph 3-72.
J2	A-B	Normal. Refer to Figure 3-7.
	A-C	Disconnects clamp voltage from reference video input amplifier 2U12 for test.
J3	A-B	Normal. Control system CPU selects station reference video or record (input) video as servo video reference. Refer to Figure 3-7.
	A-C	Forces selection of station reference video as servo video reference.
	Removed	Forces selection of record (input) video as servo video reference.
J4	A-B	PAL color standard. Refer to Figure 3-7.
	A-C	SECAM color standard. Refer to Figure 3-7.

(Continued next page)

Table 3-5. PAL/SECAM Reference PWA Jumpers (Continued)

Jumper	Position	Function
J5	A-B	Normal. Connects monitor video select input to the monitor video select switches (H = demod video, L = auxiliary video). Refer to Figure 3-9.
	A-C	Forces selection of demod video for monitor video output.
J6	A-B	Normal. Refer to Figure 3-8.
	A-C	Disconnects ScH error output of color frame detector from window detector for hysteresis inhibitor pulse former.

3-27 Mod/Demod PWA

There are two configurations of the Modulator/Demodulator (Mod/Demod) PWA: one for NTSC/PAL-M video standards (PWA No. 1450206) and one for PAL/SECAM standards (PWA No. 1450216). The primary difference between PWAs is in component values. One schematic diagram (1450208) serves both PWAs. All communication with the control system microprocessor is via the control system interface on the Reference PWA. Refer to Figure 3-1, 3-4, or 3-7.

The Mod/Demod PWA can be functionally divided into modulator, demodulator, and playback equalizer.

3-28 Modulator

The modulator portion of the PWA accepts the incoming composite video signal and converts the signal to a frequency-modulated carrier for recording on tape. Associated circuits include functions of clamping, preemphasis, and automatic frequency control (AFC). These circuits are diagrammed in Figure 3-10.

The signal to be recorded is routed from VIDEO IN connector J9 on the I/O connector panel to the Mod/Demod PWA. The input connector is isolated from chassis ground, and signal ground is connected to ground on the PWA. If desired, video input circuitry can be configured for differential balanced input by placement of jumpers on the PWA.

The video input signal is applied through PWA pin contacts 11 and 12 to a balanced/unbalanced select network. The signal is then applied to dc-controlled variable gain differential FET amplifier 1Q7. The amplifier gain is controlled by the setting of the VIDEO RECORD level potentiometer on the primary control panel. This control provides a dc level that is routed through buffer/translator 1Q14/1Q13 to amplifier 1Q7. The gain-controlled video signal is further amplified to 1.5 Vp-p, converted to single-ended, and back-porch-clamped by amplifier 1U6-8.

The output from 1U6-8 is routed into three paths. One path is through buffer 1Q8 to PWA contacts 15/16 where the signal is routed to the record video input of the

Reference PWA. The second path is to the back porch clamp circuits, and the third path is through emitter follower 1Q5 to the preemphasis networks.

3-29 **Back Porch Clamp.** The output of video amplifier 1U6-8 is applied through low-pass filter 1C34/1L2/1C56, buffer 1Q11, and ac-coupled to sync separator 1U12-7/1U14-13 which generates a gate pulse during back porch time. This pulse is applied to FET switches 1Q9 and 1Q12. During back porch time, video from buffer 1Q11 is gated by 1Q12 and compared to ground by 1U15-7. Comparator 1U15-7 provides an error signal back to amplifier 1U6-8 to clamp video to ground during back porch time.

Filtered video from 1Q11 is also applied to sync separator 1U13-7 which feeds pulse former 1U14-13 to generate a switch pulse for burst switch driver 1U9. The drive pulse from 1U9 closes switch 1U5 during the burst interval. Stripped record composite sync from 1U13-7 is also routed via PWA contacts 17/18 to the Reference PWA.

The 2X burst circuit is disabled when the PAL/SECAM Mod/Demod PWA is in SECAM configuration. Low SECAM logic level at PWA contact 20 and low 50-Hz logic level at contact 19 cause the output of gate 1U20-10 to be high. This high, inverted by gate 1U20-13, disables pulse-former one-shot 1U14-12, thus disabling switch driver 1U9 and 2X burst switch 1U5.

3-30 **Preemphasis.** The output of emitter follower 1Q5 is applied to fixed preemphasis network 1R20/1R19/1C5 which boosts the high frequencies (8 dB for 525-line video, or 10 dB for 625-line video). The output of 1Q5 is also applied to switch 1U5 which closes during burst time to route the signal to preemphasis network 1R18/1R17/1C3. This provides an additional 6 dB of gain (2X burst) for the burst portion of the signal and results in improved signal-to-noise ratio of the reproduced burst. Switched and nonswitched signals are combined at the emitter of 1Q3 and routed to the fm modulator.

3-31 **FM Modulator.** The fm modulator is composed of 1Q1, 1Q6, 1U2, 1U3, and associated components. The video modulates an fm carrier that varies linearly with the video signal. For 525-line video, deviation frequencies are 7.9 MHz at blanking and 10.0 MHz at peak white. For 625-line video, blanking is at 7.68 MHz, and peak white is at 8.9 MHz.

Preemphasized video from amplifier 1Q3 is applied through emitter follower 1Q2 to current source transistors 1Q1 and 1Q6. Capacitors 1C1 and 1C10 are linearly discharged by this current, then recharged by RS flip-flop 1U2-14/15, thereby providing a frequency-modulated signal. The modulator operates at twice the desired frequency and when divided, reduces second harmonic components. Potentiometer 1R28 provides a linearity adjustment. The fm signal from 1U2-3 is limited by both sections of 1U1 and transformer coupled by 1T1 to provide balanced outputs at PWA contacts 37/38 and 39/40. These outputs are routed through balanced line cables to the record amplifier on the Record Amplifier and Edit Erase PWA. There, the signal is divided by two prior to recording.

The fm signal from 1U2-7 is also divided by two by flip-flop 1U11 to provide an EE signal for the EE/off-tape selector on the demodulator portion of the PWA.

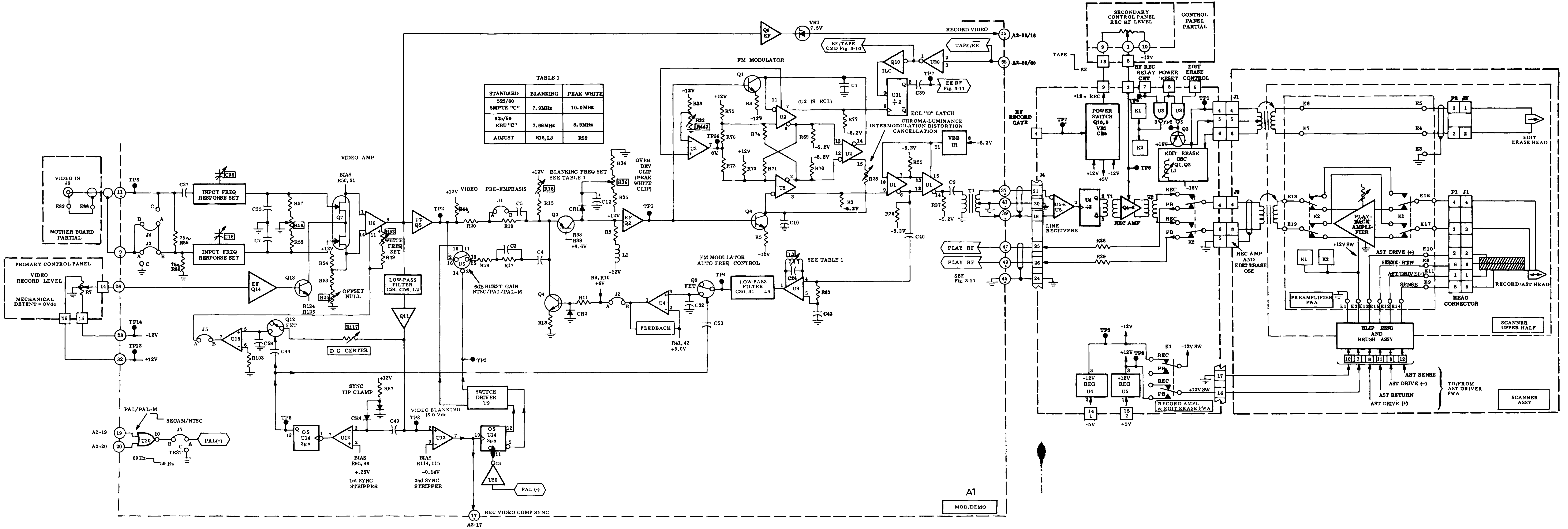


TABLE 1

STANDARD	BLANKING	PEAK WHITE
525/60 SMPTE "C"	7.9MHz	10.0MHz
625/50 EBU "C"	7.68MHz	8.9MHz
ADJUST	R16, L3	R52

Figure 3-10.
Modulator (PWA1), Record Amplifier and Edit Erase PWA, and Scanner

3-32 Automatic Frequency Control. The automatic frequency control (AFC) loop is composed of 1U8, 1U4, 1Q4, and 1Q9. It maintains the fm oscillator at the proper blanking frequency during back porch time. Tuned demodulator 1U8-1 and low-pass filter 1C30/1L4/1C31 produce demodulated video from rf sampled at 1U1-6. During back porch time a pulse from pulse former 1U14-13 closes FET switch 1Q9 to sample the demodulated dc level. This dc level is compared to a fixed voltage by comparator 1U4-1 which provides a dc error voltage. Error voltage is converted to an error current by 1Q4 to control modulator frequency. Inductor 1L3 is adjusted to establish desired blanking (back porch) frequency.

3-33 Demodulator

The demodulator provides two parallel video line outputs to the I/O connector panel. Demod video is also routed to the picture monitor via demod/auxiliary video switches on the Reference PWA. The demodulator section also detects rf dropouts, attenuates the burst signal, and generates demod composite sync and a color/monochrome signal.

The off-tape/EE logic level, initiated by the EE switch on the primary control panel, enters the Mod/Demod PWA at connector contacts 59/60 (Figure 3-10). Normal and inverted off-tape/EE commands are applied to two diode bridge switches, 1U36-5/-7 and 1U36-13/-15. These switches, shown in Figure 3-11, select either tape rf or EE rf for application to input buffer 1Q48. The rf signal is transformer-coupled by 1T5 to limiters 1U40, 1U45, and 1U44 to remove any playback amplitude variations. Limiter balance adjustment 1R398 is provided to balance out even harmonic components of the signal.

The limiter output is applied to pulse former circuit 1Q55/1Q54/1Q60 which produces pulses of a uniform width for each transition of the limited rf signal, thereby doubling carrier frequency components. Residual carrier components are minimized by detector balance control 1R399. Pulses are routed through limiter 1U46 to current mode switch 1U61.

Switch 1U61, shown in Figure 3-12, drives a low-pass filter followed by a phase equalizer. Current is controlled by a feedback clamp loop maintaining the blanking level of the output video signal at zero volts. Unwanted frequency components are removed by the low-pass filter composed of 1L23, 1L24, and 1L25. The phase equalizer (1L26/1L27/1T6/1T7) compensates for group delay distortion introduced by the low-pass filter which reconstructs the composite video signal by integrating constant width pulses from the pulse former.

Phase equalizer output is de-emphasized by the network composed of 1Q62/1Q59/1R433/1R414/1C225, amplified by 1Q53 and 1Q52, and applied to an output driver via FET switching configuration 1Q45/1Q46. FET switches are controlled by the dropout detector circuit to apply ground level to the output driver during a dropout. Also, video applied to the output driver is attenuated by 6.0 dB during burst, thereby restoring original burst level boosted in the modulator section.

The demodulated trailing edge of sync triggers one-shot 1U42-5 that switches in attenuator circuit 1Q38. The attenuation is adjustable by a potentiometer 1R310

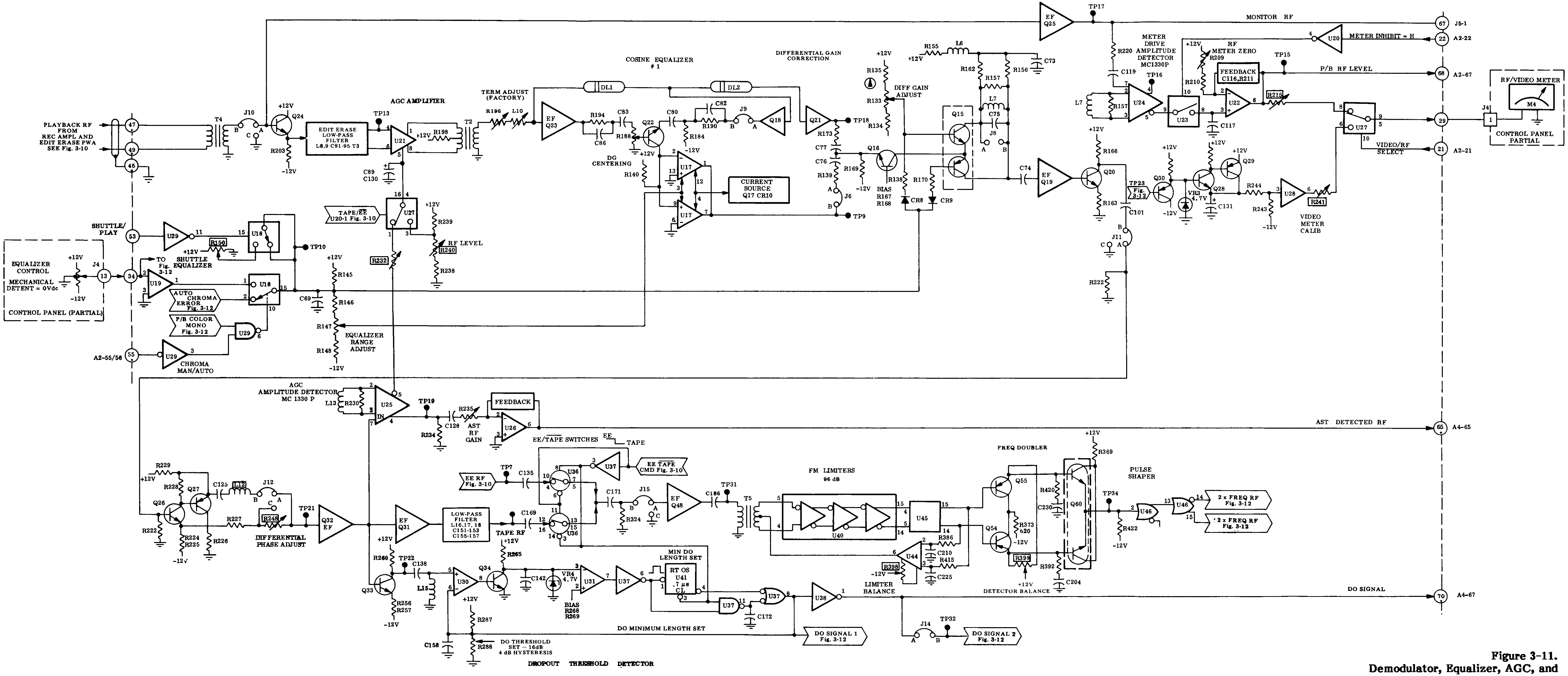


Figure 3-11.
Demodulator, Equalizer, AGC, and Dropout Detector (PWA1)

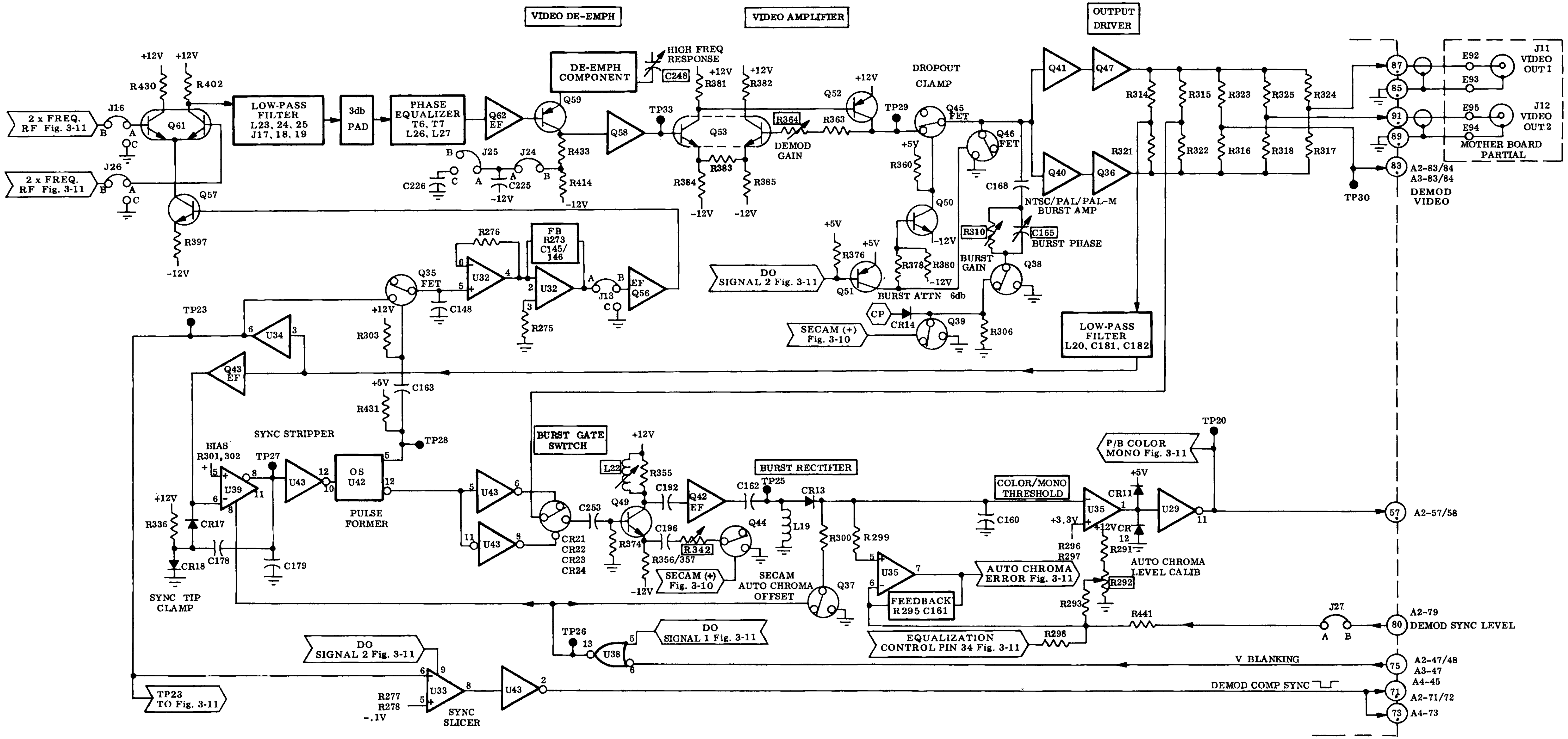


Figure 3-12.
Demodulator, Sync Stripper, and Auto Chroma (PWA1)

which provides correct burst amplitude. Capacitor 1C165 is adjusted for correct burst phase. This attenuation circuit is disabled in SECAM configuration by the PAL/SECAM logic level from the Reference PWA (Figure 3-10). Output drivers 1Q47 and 1Q36 provide line video outputs at the VIDEO 1 OUT and VIDEO 2 OUT connectors on the I/O connector panel.

3-34 **Dropout Detector.** The dropout detector is shown in Figure 3-11. Dropout detector 1Q33/1Q34/1U30/1U31/1U37/1U41 detects the occurrence and duration of off-tape video dropouts. The resulting dropout pulse is routed to the time-base corrector and is also used to control video amplifier FET switches 1Q45 and 1Q46 (Figure 3-12) that clamp video to ground during a dropout. 1U30-8 compares an rf signal from the equalizer with the dropout threshold level. Precision (1%) resistors 1R287 and 1R288 establish the dropout threshold at -16dB with 4dB hysteresis.

3-35 **Feedback Clamp.** Demodulated video output is low-pass-filtered by 1L20/1C181/1C182 (Figure 3-12) to remove burst, and then routed into two paths. One path is through translator 1Q43 to sync stripper 1U39-8. Stripped sync triggers one-shot 1U42 which provides a gate pulse at 1U42-5 for FET switch 1Q35 in the feedback clamp circuit and an output from 1U42-12 for switching on burst gate 1CR21—1CR24.

Filtered video from 1L20 is sampled by switch 1Q35 during back porch time. Sampled dc voltage is applied to feedback clamp 1U32/1Q56/1Q57/1Q61. Current through 1Q61 is controlled to cause the video output back porch level to be at zero volts. Filtered video from 1L20 fed through sync slicer 1U33-8 is also supplied as demodulated composite sync to Reference and AST Servo PWAs.

3-36 **Auto Chroma and Color/Monochrome.** The back porch pulse from one-shot 1U42-12 (Figure 3-12) gates the burst through diode switch 1CR21—1CR24. Gated burst is applied through 1Q49 and 1Q42 to peak detector circuitry 1L19/1CR13/1C160. Any difference between sync amplitude and peak-selected burst level produces an auto chroma error signal at 1U35-7 which is fed to the equalizer circuitry (Figure 3-11).

Peak-detected burst from 1U35-1 is used for color/monochrome status denoting presence or absence of burst. In the SECAM configuration, the high SECAM logic level enables 1Q44 and potentiometer 1R342 to set chroma amplitude.

3-37 Equalizer

Equalizer circuits control rf playback response to compensate for losses caused by head/tape interface. Refer to Figure 3-11.

3-38 **Input Circuitry.** Balanced line playback rf from the Record Amplifier and Edit Erase PWA enters the Mod/Demod PWA at contacts 47/49 and is converted to single-ended by transformer 1T4. The signal is routed to two paths. One path is to rf detector 1U24 for application to the VIDEO/RF meter on the primary control panel. The rf is also applied via buffer 1Q24 to edit erase low-pass filter 1L9/1L8/1C91—1C95/1T3. The filtered signal is routed to cosine equalizer 1DL1 and 1DL2 via AGC amplifier 1U21-1/-8.

3-39 Cosine Equalizer. The cosine equalizer compensates for record/playback losses without introducing phase shift. The frequency response characteristic of the cosine equalizers is dc-voltage-controllable. The cosine equalizer consists of delay lines 1DL1 and 1DL2 in series and associated components. Compensation is accomplished by tapping signals from the front, junction, and terminations of the delay lines and summing the signals as follows:

The signal at the front of 1DL1 at 1C114 is added to the signal at the junction of the delay lines through 1R191 in transistor 1Q22. Differential gain centering control 1R188 selects the amplitude of the 1C114 signal. The result is routed to both halves of amplifier 1U17. Amplifier 1U17 gain can be controlled by the front panel EQUALIZATION control or automatically by auto chroma circuitry.

3-40 Differential Phase and Gain. Reflected output signals from 1U17 are added to delayed output of 1DL2 in differential gain amplifier 1Q15. Components 1C75/1R157/1L7 form a differential gain compensation network. The amount of compensation is controlled by the setting of differential gain control 1R133. The differential gain amplifier output is routed through 1Q19 and 1Q20 to differential phase adjust circuit 1Q26/1Q27/1R248. The signal is then routed through straight line filter 1L16—1L18 and diode bridge switch 1U36-13/-15 to limiter circuits discussed in paragraph 3-33.

3-41 Jumpers

The Mod/Demod PWA is equipped with jumpers as aids to testing and troubleshooting. Jumpers on the Mod/Demod PWA are listed in Table 3-6. Locations of jumpers which are called out in test procedures are shown in Figure 3-65 at the end of this section.

Table 3-6. Mod/Demod PWA Jumpers

Jumper	Position	Function
J1	A-B	Normal. Refer to Figure 3-10.
	Removed	Disconnects modulator preemphasis network for test.
J2	A-B	Normal. Refer to Figure 3-10.
	Removed	Disconnects AFC loop from the modulator for blanking frequency setup. See paragraphs 3-86 and 3-87.
J3	A-B	Normal. Refer to Figure 3-10.
	A-C	Grounds shield of video input from connector J9 providing single-ended (unbalanced) video input. See paragraph 3-84.
J4	A-B	Normal. Refer to Figure 3-10.
	A-C	Shorts video input from connector J9 for adjustment of differential video input amplifier. See paragraph 3-84.

(Continued next page)

Table 3-6. Mod/Demod PWA Jumpers (Continued)

Jumper	Position	Function
J5	A-B	Normal. Refer to Figure 3-10.
	Removed	Disconnects input video amplifier clamp circuit for test. See paragraphs 3-84 and 3-88.
J6	A-B	Normal. Refer to Figure 3-11.
	Removed	Disconnects rf equalizer circuits for test.
J7	A-B	Normal. Refer to Figure 3-10.
	A-C	Forces NTSC/PAL-M Mod/Demod PWA to PAL-M configuration. Forces PAL/SECAM Mod/Demod PWA to PAL configuration.
	Removed	Forces NTSC/PAL-M Mod/Demod PWA to NTSC configuration. Forces PAL/SECAM Mod/Demod PWA to SECAM configuration.
J8	Removed	Normal. Refer to Figure 3-11.
	A-B	Bypasses differential gain circuits in the playback rf equalizer for test.
J9	A-B	Normal. Refer to Figure 3-11.
	Removed	Disconnects rf equalizer echo adder for test.
J10	A-B	Normal. Refer to Figure 3-11.
	A-C	Grounds the input of the rf equalizer.
J11	A-B	Normal. Refer to Figure 3-11.
	A-C	Grounds input to rf equalizer differential phase network for test.
J12	A-B	Normal. Refer to Figure 3-11.
	A-C	Bypasses rf equalizer differential phase network.
J13	A-B	Normal. Refer to Figure 3-12.
	A-C	Disconnects and grounds demodulator feedback clamp (dc restorer). Used in modulator frequency setup. See paragraph 3-87.
J14	A-B	Normal. Refer to Figure 3-11.
	Removed	Disconnects dropout signal from demodulator video output clamp.

(Continued next page)

Table 3-6. Mod/Demod PWA Jumpers (Continued)

Jumper	Position	Function
J15	A-B	Normal. Refer to Figure 3-11.
	A-C	Disconnects and grounds selected (tape/EE) rf signal input to demodulator limiter for factory test.
J16	A-B	Normal. Refer to Figure 3-12.
	A-C	Disconnects and grounds pulse counter detector output to demodulator low-pass filter. Used with jumper J26 for factory test.

Note

Jumpers J17 through J23 are used in factory setup of the demodulator low-pass filter and phase equalizer. Only their normal positions are listed below.

Jumper	Position	Function
J17	A-B	Normal. Refer to Figure 3-12.
J18	A-B	Normal. Refer to Figure 3-12.
J19	A-B	Normal. Refer to Figure 3-12.
J20	Removed	Normal. Refer to Figure 3-12.
J21	A-B	Normal. Refer to Figure 3-12.
J22	Removed	Normal. Refer to Figure 3-12.
J23	A-B	Normal. Refer to Figure 3-12.
J24	A-B	Normal. Refer to Figure 3-12.
	Removed	Disconnects demodulator deemphasis network (1C225).
J25	A-B	Normal Refer to Figure 3-12.
	A-C	Adds 1C226 to demodulator deemphasis network. See jumper J24 above.
J26	A-B	Normal. Refer to Figure 3-12.
	A-C	Disconnects and grounds demodulator pulse counter detector output to clamp amplifier and low-pass filter. Used with jumper J16 for factory test.
J27	A-B	Normal. Refer to Figure 3-12.
	A-C	Disconnects demodulator video sync level from autochroma.

3-42 Record Amplifier and Edit Erase PWA

In edit and nonedit record modes, this PWA amplifies the video rf signal from the modulator and applies it to the video record/playback head on the scanner. In play modes, the playback signal from the Preamplifier PWA (in the scanner assembly) is routed straight through this PWA to the equalizer on the Mod/Demod PWA. In record modes, edit erase oscillator output is routed straight through the Preamplifer PWA to the edit erase head.

Timing and control of both edit and nonedit record/playback switching is exercised by the control system microprocessor (CPU) and programmable interval timers on the Control PWA. See paragraph 6-20 in section 6 of this manual.

The Record Amplifier and Edit Erase PWA is mounted on the front of the transport base casting directly above the scanner assembly. I/O signals exchanged between this PWA and heads on the rotating drum of the scanner are coupled through rotary transformers in the scanner assembly. The Record Amplifier and Edit Erase PWA is shown in Figure 3-10.

3-43 Nonedit Record Mode

The record rf signal is applied to the Record Amplifier and Edit Erase PWA through balanced cables. The rf input is at twice the carrier frequency to eliminate second harmonic effects. The signal is first buffered by line receivers U5-6 and U5-2 which square the signal for application to divide-by-two circuit U4-2/-3. The divided-by-two output is transformer-coupled by T1 to the grounded-base record amplifier composed of Q6, Q7, and Q8. The amplifier current is controlled by the REC RF LEVEL control which is a screwdriver adjustment on the secondary control panel. Record amplifier output is transformer-coupled by T2 to record/play relay K2.

Relay K2 routes record video to connector J2, contacts 1/4 and 3/6. Record video is coupled by the video rotary transformer, through two relays on the Preamplifier PWA, to the record/play head on the scanner. At the same time, relay K1 routes regulated -12Vdc to record amplifier and record level adjustment circuits.

The video edit interrupt (INT 4) to the control system CPU provides precise timing for on/off control of record video and video erase current when entering and exiting both nonedit and edit record modes. INT 4 is asserted three times with very precise timing between assertions. (See paragraph 6-40 in Section 6 for details.) On/off switching of record video and erase current is a three-step procedure. Each step is initiated by an assertion of INT 4. The three-step sequence, which is completed within one vertical interval (one field), is as follows.

On the first assertion of INT 4, video edit erase control input at J4-6 goes high. (The video reset input at J4 is high, or not asserted, when the CPU is in a write cycle through video port 6U36.) The low output of gate U3-5 turns on the edit erase oscillator composed of Q1/Q2/L1 and associated components. The edit erase (flying erase) head on the scanner then begins erasing any video which may be recorded on the tape.

On the second assertion of INT 4, the video record relay input at J4-7 goes high. (The video reset input at J4-5 is high.) The low output of gate U3-3 energizes relays K1 and K2. Thus, the record signal path is established, and power is supplied to the record amplifier.

On the third assertion of INT 4, the video record command input at J4-4 goes high. Q9 and Q10 turn off, thus supplying +12 Vdc to the record amplifier rf level control (REC RF LEVEL control on the secondary control panel) and the record amplifier is biased on.

After the start of the recording has traveled off the scanner, video edit erase control input at J4-6 goes low. This turns off the edit erase oscillator (and the flying erase head) and the longitudinal (bulk) video erase head stack is turned on. (See paragraph 4-12 in Section 4 for details of bulk video erasing.)

When record mode is exited, reverse switching of video erase and then record/play relays and record command is timed and executed by the control system in the same fashion.

3-44 Edit Record Modes

Manually entered edit entrance and exit points, which are held in RAM storage on the Control PWA, provide only coarse timing for implementation of the video switching involved in editing. Precise timing is provided by programmable interval timers which time assertions of the video edit interrupt (INT 4). CPU switches the video input path from tape to EE on the vertical interval interrupt (INT 0) prior to the entrance point. Edit recording begins with field 2 of the selected entrance point frame. Switching sequences of video and erase current are generally the same for assemble edits as for nonedit recordings.

When making assemble edit recordings (as in nonedit recordings) the longitudinal video erase head stack is also switched on. After enough time has elapsed in record mode to allow the start of the recording to travel off the scanner, the edit erase (flying erase) head is turned off and the longitudinal (bulk) video erase head stack is turned on. When making insert edits, this switching operation is not done, and all video erasing is accomplished by the flying erase head.

The edit erase drive to the flying erase head is a 25-MHz, 40 Vp-p signal. L1 is used to adjust signal amplitude.

At the exit point, the record command is switched off, record/play relays are switched to play, and video edit erase is switched off (in that order) by the control system. The CPU then switches video from EE back to tape.

3-45 Playback Modes

In playback modes, the video record relay input at J4-7 and the video edit erase control input at J4-6 are both low. Thus, gates U3-3 and U3-5 are inhibited, the record amplifier is not switched on, and relays K1 and K2 are not energized. Playback video from the Preamplifier PWA in the scanner assembly is routed straight through contacts of relay K2 to equalizer circuits on the Mod/Demod PWA. (Refer to Figure 3-11.) Regulated +12 Vdc is routed to the Preamplifier PWA in the scanner assembly through contacts of relay K1.

3-46 Preamplifier PWA

Note

Simple circuits on the Preamplifier PWA are explained here as part of the video system. However, inasmuch as the Preamplifier PWA is located in the upper (rotating) drum of the scanner assembly, and the scanner assembly is considered part of the servo system, instructions for replacement of components on the Preamplifier PWA are given in the servo section of this manual (Section 5, Part II).

The Preamplifier PWA is shown in Figure 3-10. In playback modes, relay K1 on the Record Amplifier and Edit Erase PWA switches regulated +12 Vdc to the Preamplifier PWA. The switched +12 Vdc is applied to preamplifer circuits and it energizes relays K1 and K2 which route the playback video through preamplifier circuitry and through the video rotary transformer to equalizer circuits on the Mod/Demod PWA.

Differential video input from the video record/playback head is applied through relay K1 to step-up transformer T1. Transformer T1 feeds the high-gain differential amplifier composed of Q1—Q4. The output of this amplifier is applied to differential input amplifier U1. The gain of amplifier U1 is preset at the factory.

Output of amplifier U1 is fed through transformer T2 and through contacts of relay K2 to the video rotary transformer. Playback video is subsequently routed straight across the Record Amplifier and Edit Erase PWA and through balanced cables to the equalizer on the Mod/Demod PWA.

In record mode, preamplifier circuits are without power, and record video is routed from the video rotary transformer, through the contacts of de-energized relays K2 and K1, to the video record/playback head.

The Preamplifier PWA also contains noise filter components for four lines between the AST flexure element on the record/playback head and the scanner slip-ring and brush connection to the AST Driver PWA. These filters (not shown in Figure 3-10) are for the (+) AST drive, (-) AST drive, AST sense, and AST sense return lines.

Two lines are also provided on the Preamplifier PWA for erase current from the Record Amplifier and Edit Erase PWA to the edit erase (flying erase) head on the scanner.

3-47 REMOVAL/INSTALLATION

Mod/Demod and Reference PWAs are mounted in the card cage, and no removal/reinstallation instructions are necessary. Instructions for removal and reinstallation of the Preamplifier PWA (located within the scanner assembly) are given in Section 5. The Record Amplifier and Edit Erase PWA is removed and reinstalled on the transport as follows.

STEP 1 Remove transport trim as described in Part I, paragraph 4-12.

STEP 2 Remove three no. 4 screws and washers securing shield over Record Amplifier and Edit Erase PWA, and detach shield. See Figure 3-13.

STEP 3 Disconnect four connectors (J1 through J4) from Record Amplifier and Edit Erase PWA. See Figure 3-14.

STEP 4 Remove four no. 8 screws and washers securing Record Amplifier and Edit Erase PWA transport casting, and remove PWA.

STEP 5 Reinstall Record Amplifier and Edit Erase PWA, its connectors, and shield in reverse order of removal.

STEP 6 Reinstall transport trim removed in step 1.

3-48 REFERENCE PWA ADJUSTMENTS

3-49 General

The following adjustment procedures are grouped by Reference PWA type: NTSC (1450346), PAL-M (1450363), and PAL/SECAM (1450356). Components and test points are identified with the card cage PWA number preceding the control or test point reference designation. For example, 2TP4 indicates test point 4 on PWA2, the Reference PWA.

3-50 NTSC Reference PWA

Checks and adjustments covered in the following paragraphs are as follows:

- Voltage regulation
- Input video processing
- Color frame generation
- ScH voltage calibration
- ScH phase calibration
- Color frame identification
- Monitor video processing

Locations of jumpers, test points, and adjustment controls on the NTSC Reference PWA (1450346) are shown in Figure 3-67 at the end of this section of the manual.

Before starting, connect NTSC Insertion Test Signal Generator (Tektronix Model No. 147), NTSC Gen Lock Test Signal Generator (Tektronix Model No. 146), color

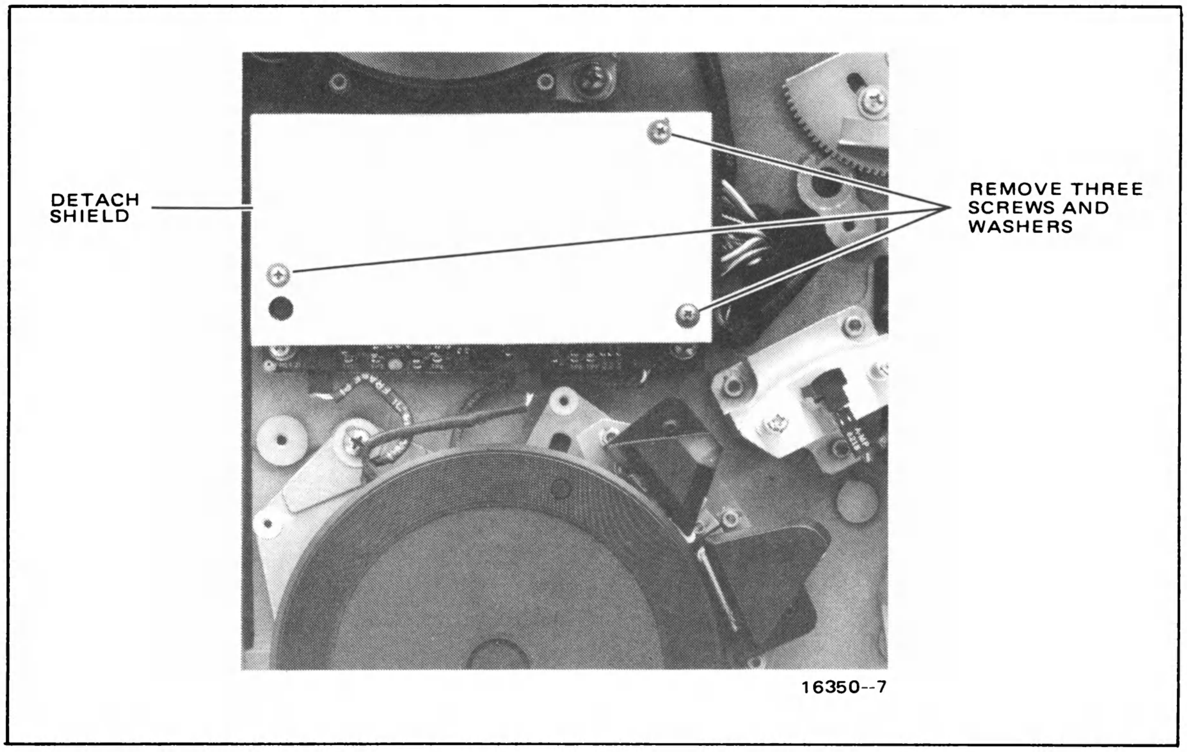


Figure 3-13. Removing Shield Over Record Amplifier and Edit Erase PWA

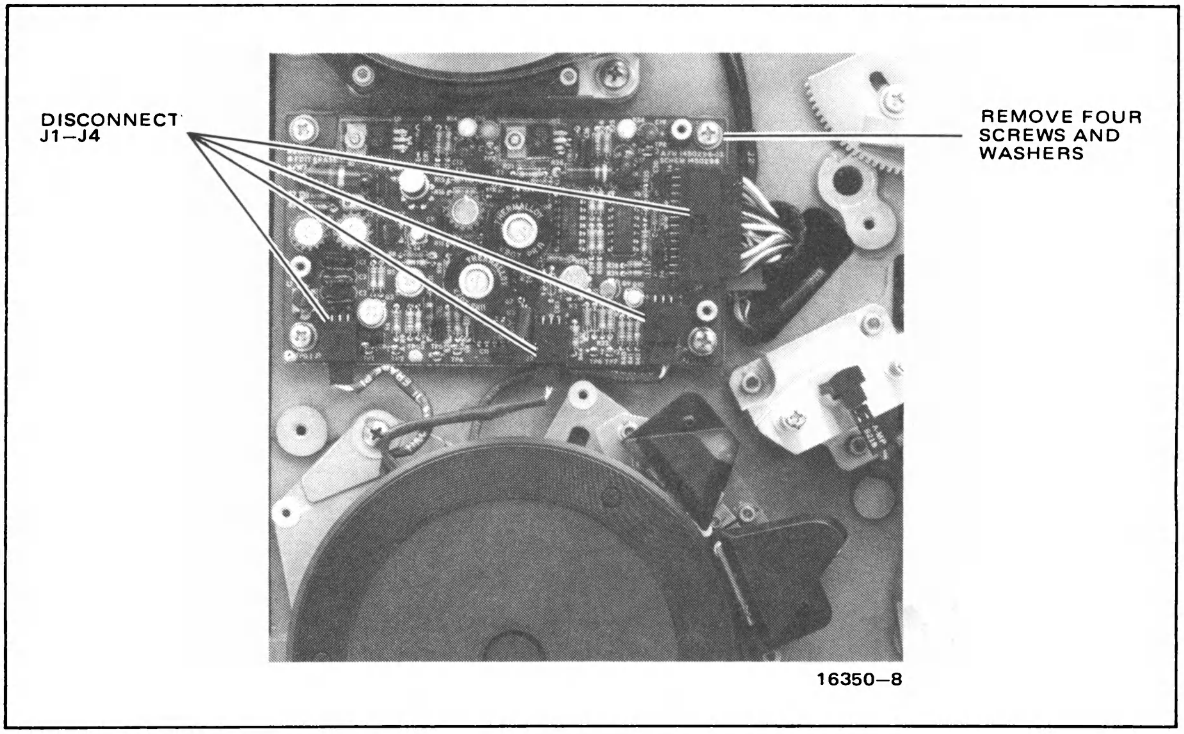


Figure 3-14. Removing Record Amplifier and Edit Erase PWA

field identifier (Ampex Part No. DT1392863, or equivalent), the VPR-80, TBC Time-Base Corrector, and picture monitor as shown in Figure 3-15. Set the insertion test signal generator for color bar output. Calibrate the test signal generator to RS-170A specifications for ScH phase. ScH phase relationship is displayed in degrees on the front panel of the color field identifier.

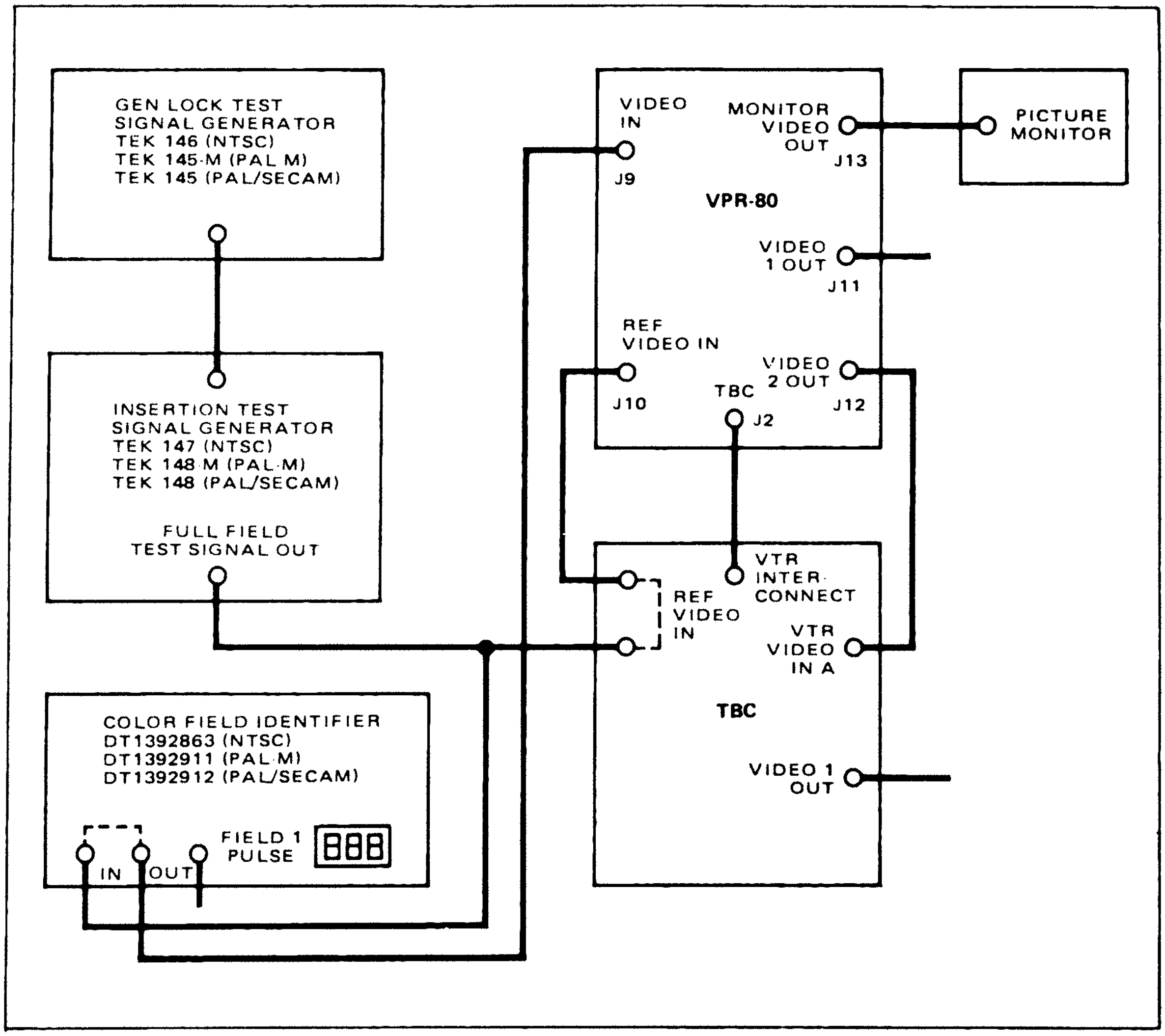


Figure 3-15. Reference PWA Test Equipment Setup

3-51 Voltage Regulation

Voltage regulation must be ensured before making any adjustments on Reference PWA. Check and adjust regulation of ±12 Vdc on Reference PWA as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and, using a digital voltmeter, measure +12 Vdc at test point 2TP10.

STEP 3 If necessary, adjust 2R42 for an indication of +12 Vdc ±0.020 Vdc.

STEP 4 Measure -12 Vdc at test point 2TP6. If necessary, adjust 2R68 for an indication of -12 Vdc ±0.020 Vdc.

3-52 Input Video Processing

Check and, if necessary, adjust video input circuits as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and press EE switch. EE indicator should be lighted.

STEP 3 Open VPR-80 top access door and place REF SELECT switch 6S5 on Control PWA in the INPUT position. See Table 3-6 in Part I of this manual.

STEP 4 Place scope probe on test point 2TP1 (SELECTED VIDEO). Verify the 1.0 Vp-p signal.

STEP 5 Move scope probe to test point 2TP3.

STEP 6 Adjust 2R34 as necessary for an indication of 1.5 Vp-p.

STEP 7 Return REF SELECT switch 6S5 to AUTO position.

STEP 8 Move scope probe to test point 2TP4.

STEP 9 Adjust 2L11 as necessary for maximum peak-to-peak burst amplitude.

3-53 Color Frame Generation

Check and, if necessary, adjust color subcarrier frequency and amplitude as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Set jumper 2J1 to the A-B (TEST) position.

STEP 3 Turn VPR-80 power on, and connect scope probe to test point 2TP7 (SC).

STEP 4 Adjust subcarrier frequency with 2C8 as carefully as possible (subcarrier frequency = 3.579545 MHz ±10 Hz).

STEP 5 Return jumper 2J1 to A-C position.

STEP 6 Verify that signal at test point 2TP7 is locked to burst at test point 2TP1 (SELECTED VIDEO).

STEP 7 Connect scope probe to test point 2TP7 (SC).

STEP 8 Adjust 2L9 for maximum peak-to-peak subcarrier signal.

3-54 ScH Voltage Calibration

Calibrate ScH voltage as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and connect scope probe to test point 2TP21 (ScH).

STEP 3 Adjust 2R145 for a dc level of +5 Vdc or -5 Vdc (either is correct).

3-55 ScH Phase Calibration

Note

When calibrating ScH phase, the video input signal must be standard ScH.

Calibrate ScH phase as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and connect scope probe to test point 2TP21 (ScH).

STEP 3 Adjust 2R2 for a peak dc level of +5 Vdc or -5 Vdc (either is correct).

3-56 Color Frame Identification

Verify color frame identification as follows:

STEP 1 Connect scope channel 1 probe to test point 2TP28 (REF CF).

STEP 2 Connect scope channel 2 probe to test point 2TP1 (SELECTED VIDEO).

STEP 3 Turn on VPR-80 power and trigger scope externally on test point 2TP28 (REF CF).

STEP 4 Verify that the pulse on scope channel 1 (REF CF) occurs in every fourth field (field 1 of frame A). A white bar appears on line 20 of field 1 of frame A (scope channel 2).

3-57 Monitor Video Processing

Check and, if necessary, adjust monitor video circuits as follows:

STEP 1 With VPR-80 power off, connect scope to MONITOR VIDEO OUT connector on VPR-80 I/O connector panel. Terminate with 75 ohms.

STEP 2 Connect multiburst video signal to VIDEO IN connector.

STEP 3 Place Reference PWA on an extender.

STEP 4 Turn on VPR-80 power and press EE switch. EE indicator should be lighted.

STEP 5 Adjust 2C133 for flat frequency response.

STEP 6 Adjust 2R195 for unity gain.

STEP 7 Set picture monitor to display vertical interval.

STEP 8 Thread a work tape on the transport and make a short recording. Rewind tape.

STEP 9 Play recording made in step 8 and verify that vertical interval is re-inserted into picture monitor.

STEP 10 Adjust 2R130 until 2H pulses are aligned.

3-58 PAL-M Reference PWA

Checks and adjustments covered in the following paragraphs are as follows:

- Voltage regulation
- Input video processing
- Color frame generation
    Phase-locked oscillator
    H/2 gain and phase
- ScH voltage calibration
- ScH phase calibration
- Color frame identification
- Monitor video processing

Locations of jumpers, test points, and adjustment controls on the PAL-M Reference PWA (1450363) are shown in Figure 3-68 at the end of this section of the manual.

Before starting, connect PAL-M Insertion Test Signal Generator (Tektronix Model No. 148-M), PAL-M Gen Lock Test Signal Generator (Tektronix Model No. 145-M), color field identifier (Ampex Part No. DT1392911, or equivalent), the VPR-80, TBC Time-Base Corrector, and picture monitor as shown in Figure 3-15. Set the insertion test signal generator for color-bar output. Calibrate the test signal generator to CCIR specifications for ScH phase. ScH phase relationship is displayed in degrees on front panel of the color field identifier.

3-59 Voltage Regulation

Voltage regulation must be ensured before making any adjustments on the Reference PWA. Check and adjust the regulation of ±12 Vdc on the Reference PWA as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and, using a digital voltmeter, measure +12 Vdc at test point 2TP8.

STEP 3 If necessary, adjust 2R54 for an indication of +12 Vdc ±0.020 Vdc.

STEP 4 Measure -12 Vdc at test point 2TP1. If necessary, adjust 2R77 for an indication of -12 Vdc ±0.020 Vdc.

3-60 Input Video Processing

Check and, if necessary, adjust video input circuits as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and press EE switch. EE indicator should be lighted.

STEP 3 Open VPR-80 top access door and place REF SELECT switch 6S5 on the Control PWA in the INPUT position. See Table 3-6 in Part I of this manual.

STEP 4 Place scope probe on test point 2TP6 (SELECTED VIDEO). Verify the 1.0 Vp-p signal.

STEP 5 Move scope probe to test point 2TP5.

STEP 6 Adjust 2R43 as necessary for an indication of 1.5 Vp-p.

STEP 7 Return REF SELECT switch 6S5 to the AUTO position.

STEP 8 Move the scope probe to test point 2TP10.

STEP 9 Adjust 2L12 as necessary for maximum peak-to-peak burst amplitude.

3-61 Color Frame Generation

3-62 **Phase-Locked Oscillator.** Check and, if necessary, adjust color subcarrier frequency and amplitude as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Set jumper 2J1 to the A-C (TEST) position.

STEP 3 Turn VPR-80 power on, and connect scope probe to test point 2TP2.

STEP 4 Adjust subcarrier frequency with 2C10 as carefully as possible (subcarrier frequency = 3.57561149 MHz ±10 Hz).

STEP 5 Return jumper 2J1 to A-B position.

STEP 6 Verify that signal at test point 2TP2 is locked to burst at test point 2TP6 (SELECTED VIDEO).

STEP 7 Connect scope probe to test point 2TP7.

STEP 8 Adjust 2L1 for maximum peak-to-peak subcarrier signal.

3-63 H/2 Gain and Phase. Check and, if necessary, adjust H/2 (7.8 kHz) gain and phase as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and connect scope channel A probe to test point 2TP3 and connect scope channel B probe to test point 2TP6 (SELECTED VIDEO).

Note

Gain and phase adjustment controls 2R30 and 2R31 are interactive.

STEP 3 Adjust 2R30 and 2R31 for 5 Vp-p signal with peaks that coincide with the burst.

3-64 ScH Voltage Calibration

Calibrate ScH voltage as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and connect scope probe to test point 2TP30 (ScH).

STEP 3 Adjust 2R152 for a dc level of +5 Vdc or −5 Vdc (either is correct).

3-65 ScH Phase Calibration

Note

When calibrating ScH phase, the video input signal must be standard ScH.

Calibrate ScH phase as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and connect scope probe to test point 2TP30 (ScH).

STEP 3 Adjust 2R9 for a peak dc level of +5 Vdc or -5 Vdc (either is correct).

3-66 Color Frame Identification

Verify color frame identification as follows:

STEP 1 Connect scope channel 1 probe to test point 2TP27 (REF CF).

STEP 2 Connect scope channel 2 probe to test point 2TP6 (SELECTED VIDEO).

STEP 3 Turn on VPR-80 power and trigger scope externally on test point 2TP27 (REF CF).

STEP 4 Verify that pulse on scope channel 1 (REF CF) occurs in every eighth field (field 1 of frame A). A white bar appears on line 20 of field 1 of frame A (scope channel 2).

3-67 Monitor Video Processing

Check and, if necessary, adjust monitor video circuits as follows:

STEP 1 With VPR-80 power off, connect scope to MONITOR VIDEO OUT connector on the VPR-80 I/O connector panel. Terminate with 75 ohms.

STEP 2 Connect multiburst video signal to VIDEO IN connector.

STEP 3 Place Reference PWA on an extender.

STEP 4 Turn on VPR-80 power and press EE switch. EE indicator should be lighted.

STEP 5 Adjust 2C149 for flat frequency response.

STEP 6 Adjust 2R205 for unity gain.

STEP 7 Set picture monitor to display vertical interval.

STEP 8 Thread a work tape on the transport and make a short recording. Rewind the tape.

STEP 9 Play recording made in step 8 and verify that the vertical interval is reinserted into the picture monitor.

STEP 10 Adjust 2R134 until 2H pulses are aligned.

3-68 PAL/SECAM Reference PWA

Checks and adjustments covered in the following paragraphs are as follows:

- Voltage regulation
- Input video processing
- Color frame generation
    - Phase-locked oscillator (PAL only)
    - Chroma detector (SECAM only)
    - H/2 Gain and phase
- 25-Hz amplitude calibration
- ScH phase calibration
- Color frame identification
- Monitor video processing

Locations of jumpers, test points, and adjustment controls on the PAL/SECAM Reference PWA (1450356) are shown in Figure 3-69 at the end of this section of the manual.

Before starting, connect PAL Insertion Test Signal Generator (Tektronix Model No. 148), PAL Gen Lock Test Signal Generator (Tektronix Model No. 145), color field identifier (Ampex Part No. DT1392912, or equivalent), the VPR-80, TBC Time-Base Corrector, and picture monitor as shown in Figure 3-15. Set PAL/SECAM switch on color field identifier as appropriate. Set insertion test signal generator for color bar output. Calibrate test signal generator to CCIR specifications for ScH phase. ScH phase relationship is displayed in degrees on front panel of the color field identifier.

3-69 Voltage Regulation

Voltage regulation must be ensured before making any adjustments on the Reference PWA. Check and adjust the regulation of ±12 Vdc on the Reference PWA as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on. Using a digital voltmeter, measure +12 Vdc at test point 2TP11.

STEP 3 If necessary, adjust 2R57 for an indication of +12 Vdc ±0.020 Vdc.

STEP 4 Measure -12 Vdc at test point 2TP1. If necessary, adjust 2R75 for an indication of -12 Vdc ±0.020 Vdc.

3-70 Input Video Processing

Check and, if necessary, adjust video input circuits as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and press EE switch. EE indicator should be lighted.

STEP 3 Open VPR-80 top access door and place REF SELECT switch 6S5 on Control PWA in INPUT position. See Table 3-6 in Part I of this manual.

STEP 4 Place scope probe on test point 2TP3 (SELECTED VIDEO). Verify 1.0 Vp-p signal.

STEP 5 Move scope probe to test point 2TP7.

STEP 6 Adjust 2R45 as necessary for an indication of 1.5 Vp-p.

STEP 7 Return REF SELECT switch 6S5 to AUTO position.

STEP 8 Move scope probe to test point 2TP8.

STEP 9 Adjust 2L13 as necessary for maximum peak-to-peak burst amplitude.

3-71 Color Frame Generation

For SECAM systems (jumper 2J4 in A-C position), omit procedure in paragraph 3-72. For PAL systems (jumper 2J4 in A-B position), omit procedure in paragraph 3-73.

3-72 Phase-Locked Oscillator (PAL Only). Check and, if necessary, adjust color subcarrier frequency and amplitude as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Set jumper 2J1 to A-C (TEST) position.

STEP 3 Turn VPR-80 power on, and connect scope probe to test point 2TP2.

STEP 4 Adjust subcarrier frequency with 2C10 as carefully as possible (subcarrier frequency = 4.43361875 MHz ±5 Hz).

STEP 5 Return jumper 2J1 to A-B position.

STEP 6 Verify that signal at test point 2TP2 is locked to burst at test point 2TP3 (SELECTED VIDEO).

STEP 7 Connect scope probe to test point 2TP9 (SC).

STEP 8 Adjust 2L1 for maximum peak-to-peak subcarrier signal.

3-73 Chroma Detector (SECAM Only). Check and, if necessary, adjust chroma detector output as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Connect SECAM video sync generator to VIDEO IN and REF VIDEO IN connectors on the VPR-80 I/O connector panel. (Use color field identifier DT1392912, or equivalent.)

STEP 3 Turn on VPR-80 power and connect scope probe to test point 2TP4.

STEP 4 Adjust 2L10 for maximum peak-to-peak H/2 (7.8 kHz) signal.

3-74 H/2 Gain and Phase. Check and, if necessary, adjust H/2 (7.8 KHz) gain and phase as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and connect scope channel A probe to test point 2TP4 and connect scope channel B probe to test point 2TP3 (SELECTED VIDEO).

Note

Gain and phase adjustment controls 2R30 and 2R31 are interactive.

STEP 3 Adjust 2R30 and 2R31 for 5 Vp-p signal with peaks that coincide with burst.

3-75 Color Frame Pulse (SECAM Only). Check and, if necessary, adjust color frame pulse as follows:

Step 1 Turn VPR-80 power off, place Reference PWA on an extender.

Step 2 Turn VPR-80 power on, and connect scope channel A probe to test point 2TP4.

Step 3 Adjust L10 for maximum signal.

Step 4 Adjust R31 so peak of the 7.8-kHz sine wave is coincident with unmodulated subcarrier at beginning of each line (burst time).

Step 5 Adjust R30 for a level of 10 Vp-p. Clipping of the positive peak is normal.

Step 6 Readjust R31 and R30 until specifications in steps 4 and 5 are met.

Step 7 Readjust L10 if necessary, per step 3, then connect scope channel B probe to test point 2TP34 and fine tune L10 for minimum dc level change. This will be a dc level changing once per frame and should not exceed 0V ±0.5V.

Step 8 Connect scope channel A probe to test point 2TP29 and verify this signal is a 7.8-kHz square wave. If not, repeat above adjustments.

Step 9 Connect scope channel A probe to 2TP31 and verify the Reference Color Frame pulse is a negative-going 20 S pulse occurring every four fields. Make sure there are no ghost pulses every two fields. The Reference

Color Frame pulse should occur on the field preceded by a half line of video and line seven containing a red color sync signal. The red color sync signal is slightly higher in amplitude than the blue.

3-76 25-Hz Amplitude Calibration

Calibrate amplitude of 25-Hz sine wave as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on. Connect scope probe to test point 2TP20 (25 Hz).

STEP 3 Verify 25-Hz sine wave and, if necessary, adjust 2R100 for 10 Vp-p amplitude.

3-77 ScH Phase Calibration

Note

When calibrating ScH phase, the video input signal must be standard ScH.

Calibrate ScH phase as follows:

STEP 1 With VPR-80 power off, place Reference PWA on an extender.

STEP 2 Turn VPR-80 power on, and connect scope probe to test point 2TP34 (ScH).

STEP 3 Adjust 2R9 for a peak dc level of +5 Vdc or −5 Vdc (either is correct).

3-78 Color Frame Identification

Verify color frame identification as follows:

STEP 1 Set PAL/SECAM switch on front panel of the color field identifier as appropriate.

STEP 2 Connect scope channel 1 probe to test point 2TP31 (REF CF).

STEP 3 Connect scope channel 2 probe to test point 2TP3 (SELECTED VIDEO).

STEP 4 Turn on VPR-80 power and trigger scope externally on test point 2TP31 (REF CF).

STEP 5 Verify that pulse on scope channel 1 (REF CF) occurs in every eighth field in PAL systems or in every fourth field in SECAM systems (field 1 of frame A). A white bar appears on line 20 of field 1 of frame A (scope channel 2).

3-79 Monitor Video Processing

Check and, if necessary, adjust monitor video circuits as follows:

STEP 1 With VPR-80 power off, connect scope to MONITOR VIDEO OUT connector on the VPR-80 I/O connector panel. Terminate with 75 ohms.

STEP 2 Connect multiburst video signal to VIDEO IN connector.

STEP 3 Place Reference PWA on an extender.

STEP 4 Turn on VPR-80 power and press EE switch. EE indicator should be lighted.

STEP 5 Adjust 2C158 for flat frequency response.

STEP 6 Adjust 2R209 for unity gain.

STEP 7 Set picture monitor to display vertical interval.

STEP 8 Thread a work tape on the transport and make a short recording. Rewind tape.

STEP 9 Play recording made in step 8 and verify that vertical interval is reinserted into picture monitor.

STEP 10 Adjust 2R141 until 2H pulses are aligned.

3-80 VIDEO SIGNAL SYSTEM ALIGNMENT

3-81 General

Signal system alignment covers all controls in the VPR-80 video signal system which do not require special factory test fixtures. Most of the following alignment procedures are not done as routine maintenance and are required only if:

- components have been replaced,
- indications of degraded performance are noted (particularly on an interchange basis), or
- an adjustment has been accidentally altered.

Capstan pinch roller pressure, tape tensions, and scanner tape guiding must be verified before evaluating signal system performance. Refer to Part I, paragraph 4-21. Unless specified otherwise, AST should be off, and manual tracking peaked (Part I, paragraph 4-27). Some servo faults can be misinterpreted as signal system problems.

Adjustments should not be attempted until the VPR-80 is at a temperature similar to its normal environment. Apply power for at least 15 minutes with no PWAs on an extender before making adjustments.

CAUTION

TO PREVENT POSSIBLE DAMAGE TO ELECTRICAL COMPONENTS, ALWAYS TURN POWER OFF BEFORE REMOVING OR INSTALLING A PRINTED WIRING ASSEMBLY (PWA) IN THE VTR.

In general, it is not necessary to compensate for the short time needed to turn power off, put a PWA on an extender, and restore power.

Calibration of television monitoring equipment and special test equipment should be checked before making any adjustments. Also, verify that input video level is correct. See Figure 3-16. All adjustments should be made while observing either VPR-80 DEMOD OUT (1TP30) output or the TBC VIDEO OUT.

Response should be adjusted to match input level, particularly in the case of the modulator, or in any adjustment using the input video signal. If, for example, the input signal has some differential gain, then setting adjustments for minimum differential gain at the signal system output could introduce differential gain into future recordings.

Playback performance of the VPR-80 is evaluated using appropriate Type C format high-band carrier video reference tape listed in Section 4, Part I, Table 4-4.

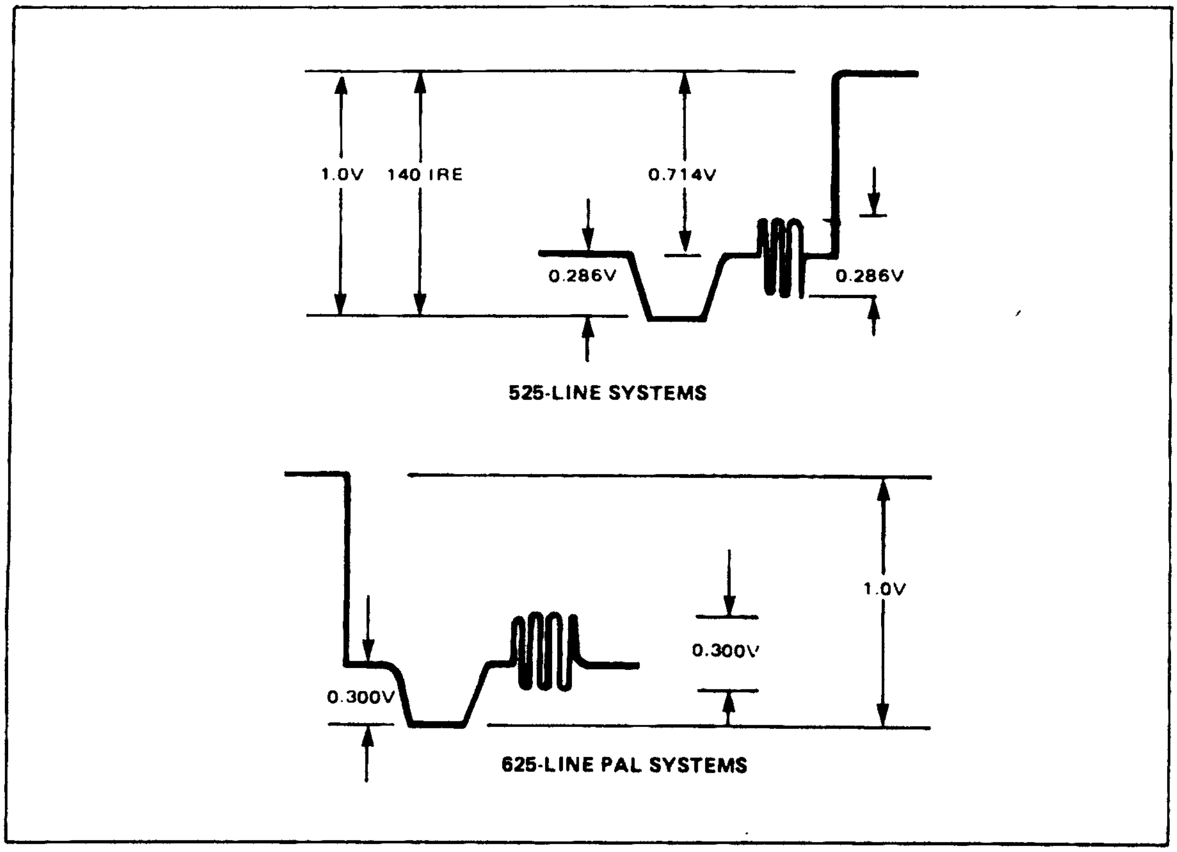


Figure 3-16. Input Video Levels

Components and test points in the following procedures are identified with the card cage PWA number preceding control or test point reference designation. For example, 1TP4 indicates that the test point is located on PWA 1, the Mod/Demod PWA.

Locations of jumpers, test points, and adjustment controls referenced in the following procedures are shown in figures at the end of this section of the manual.

Adjustments covered in the following paragraphs are as follows:

- Voltage regulation
- Modulator input amplifier
- Modulator frequencies
- Modulator linearity
- Demodulator gain and frequency response
- K-factor and chrominance/luminance delay
- Demodulator limiter and detector balance
- Rf equalizer automatic gain control
- Rf equalizer alignment and centering
- Video erase drive

3-82 Voltage Regulation

3-83 Mod/Demod PWA

Check and adjust regulation of ±12 Vdc and -5.2 Vdc on the Mod/Demod PWA as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Turn VPR-80 power on. Using a digital voltmeter, measure +12 Vdc at test point 1TP12.

STEP 3 If necessary, adjust 1R65 for an indication of +12 Vdc ±0.010 Vdc.

STEP 4 Measure -12 Vdc at test point 1TP14. If necessary, adjust 1R132 for an indication of -12 Vdc ±0.010 Vdc.

STEP 5 Measure -5.2 Vdc at test point 1TP35. If necessary, adjust 1R68 for an indication of -5.200 Vdc ±0.010 Vdc.

3-84 Record Amplifier and Edit Erase PWA

Check and adjust regulation of ±12 Vdc on the Record Amplifier and Edit Erase PWA as follows:

STEP 1 Remove transport trim as described in Part I, paragraph 4-12.

STEP 2 Remove three no. 4 screws and washers securing shield over the Record Amplifier and Edit Erase PWA, and detach the shield. Refer to Figure 3-13.

STEP 3 Turn VPR-80 power on, and, using a digital voltmeter, measure +12 Vdc at test point TP3.

STEP 4 If necessary, adjust R14 for an indication of +12 Vdc ±0.050 Vdc.

STEP 5 Measure -12 Vdc at test point TP8. If necessary, adjust R34 for an indication of -12 Vdc ±0.050 Vdc.

3-85 Modulator Input Amplifier Adjustment

The Mod/Demod PWA input differential noise cancellation and frequency response controls (1C36, 1C16, and 1R56) should need adjustment only if components are replaced. Adjust modulator input amplifier as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Connect a sine-squared pulse and bar signal to VIDEO IN connector on I/O connector panel.

STEP 3 Adjust 1R36 (OVER DEVIATION CLIP) fully counterclockwise.

STEP 4 Move jumper 1J3 from position A-B to position A-C.

STEP 5 Move jumper 1J4 from position A-B to position A-C.

STEP 6 Remove brass caps from 1C36 and 1C16.

STEP 7 Turn VPR-80 power on, and connect scope channel 1 probe to 1TP2, ac-coupled.

STEP 8 Adjust 1C16, and then 1R56 for null at 1TP2. See Figures 3-17 and 3-18.

STEP 9 Return jumpers 1J3 and 1J4 to their normal position, A-B.

STEP 10 Move scope channel 1 probe to 1TP30 (DEMOD VIDEO).

STEP 11 Adjust 1C36 for minimum tilt on white bar. It should not be distorted with respect to input signal. See Figures 3-19 and 3-20.

STEP 12 Repeat steps 4 through 11.

STEP 13 Replace brass caps on 1C36 and 1C16.

STEP 14 To check operation of input video clamp, change scope to dc-coupled, and connect channel 1 probe to 1TP8.

STEP 15 Remove and reinstall jumper 1J5. Observe that video blanking is at 0V when 1J5 is installed. This verifies clamp operation.

STEP 16 Rotate VIDEO RECORD level control fully clockwise.

STEP 17 Place scope probe on test point 1TP1, and adjust 1R36 until clipping of pulse *just occurs.*

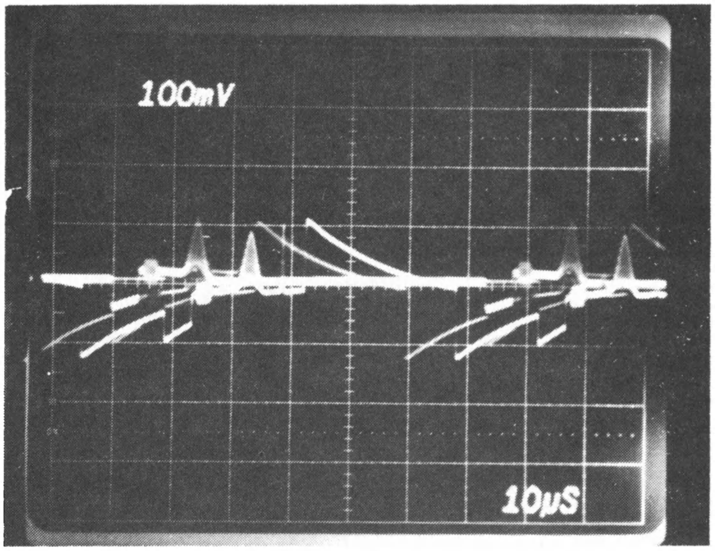


Figure 3-17. Modulator Input Amplifier Null Misadjusted

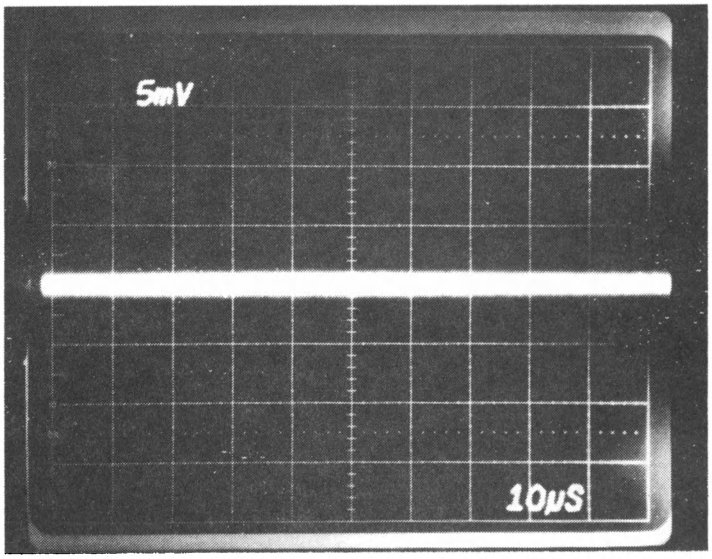


Figure 3-18. Modulator Input Amplifier Null Correctly Adjusted

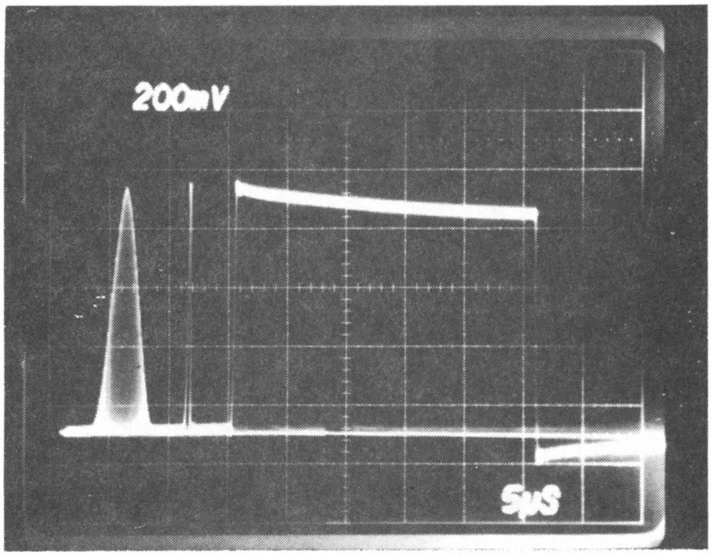


Figure 3-19. Modulator Input Amplifier Misadjusted

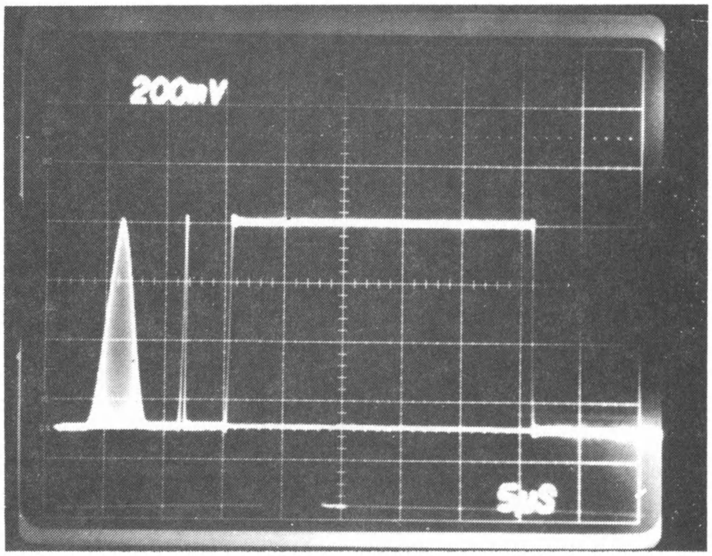


Figure 3-20. Modulator Input Amplifier Correctly Adjusted

3-86 Modulator Frequency Adjustment

There are two methods of setting modulator frequencies. The preferred method employs a spectrum analyzer, and the alternate method employs appropriate high-band carrier video reference tape.

3-87 Preferred Method

The preferred method is performed as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Connect a sine-squared pulse and bar signal with zero setup (no pedestal) to VIDEO IN connector on I/O connector panel.

STEP 3 Remove jumper 1J2 (AFC loop).

STEP 4 Adjust 1R36 fully counterclockwise.

STEP 5 Connect spectrum analyzer to 1TP7 (EE RF).

STEP 6 Turn VPR-80 power on, and connect scope channel 1 probe to 1TP36, dc-coupled.

STEP 7 Ensure that EE indicator on primary control panel is lighted.

STEP 8 Rotate VIDEO RECORD level control to center detent (unity) position.

STEP 9 Observing scope, adjust 1R443 (ZERO ADJUST) for 0.00 Vdc ±0.05 Vdc. Remove scope probe.

STEP 10 Using 1R16 (FREQUENCY), adjust blanking frequency to 7.90 MHz ±0.05 MHz for 525-line systems, or to 7.68 MHz ±0.05 MHz for 625-line systems.

STEP 11 Using 1R52 (DEVIATION), adjust peak white frequency to 10.00 MHz ±0.05 MHz for 525-line systems, or to 8.90 MHz ±0.05 MHz for 625-line systems.

STEP 12 Return jumper 1J2 to A-B position to reconnect AFC loop.

STEP 13 If necessary, use 1L3 to adjust blanking frequency to 7.90 MHz ±0.05 MHz for 525-line systems, or to 7.68 MHz ±0.05 MHz for 625-line systems.

STEP 14 After adjusting 1L3 for correct blanking frequency, recheck peak white frequency, and readjust 1R52, if necessary.

STEP 15 Rotate VIDEO RECORD level control to maximum clockwise position.

STEP 16 Connect scope probe to test point 1TP1. Trigger scope at test point 4TP2 (HORIZ) on AST Servo PWA. See Figure 5-66.

STEP 17 Adjust 1R36 (OVER DEVIATION CLIP) until clipping at pre-emphasized pulse *just occurs*.

STEP 18 Rotate VIDEO RECORD level control to center detent (unity) position.

3-88 Alternate Method

The alternate method is performed as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Connect a video input of sine-squared pulse and bar signal, 1 Vp-p with zero setup (no pedestal) to the VIDEO IN connector on I/O connector panel.

STEP 3 Remove jumper 1J2 to disable modulator AFC loop, and adjust 1R36 fully counterclockwise.

STEP 4 Turn VPR-80 power on, and establish the following operating conditions on the control panel:

a. Editor off: neither INSERT nor ASSEM indicator is lighted.

b. EE operation: EE indicator lighted.

c. Video record level is unity: VIDEO RECORD level control in detent position.

STEP 5 Connect scope probe to test point 1TP36 (BLANKING FREQ). If necessary, adjust 1R443 (ZERO ADJUST) for indication of 0.00 Vdc ±0.05 Vdc. Remove scope probe.

STEP 6 Install appropriate high-band carrier video reference tape on transport. Refer to Section 4, Part I, Table 4-4.

STEP 7 Shuttle reference tape to long section with sine-squared pulse and bar. This recording is about 16 minutes into the tape. Enter an entrance cue for convenience.

STEP 8 Move jumper 1J13 from position A-B to position A-C to disable output clamp.

STEP 9 Connect scope probe to VIDEO 2 OUT connector on I/O connector panel using coax cable and 75Ω termination. Sync scope on test point 4TP6 (HORIZ) on AST Servo PWA. (See Figure 5-66.) Scope must be dc-coupled.

STEP 10 Press PLAY and adjust scope vertical to place video blanking at a convenient graticule marking on the scope.

Note

If clipping occurs, move scope probe to test point 1TP33 (instead of VIDEO 2 OUT connector).

STEP 11 Press STOP and adjust 1R16 (FREQUENCY) to put EE video blanking at same graticule marking.

STEP 12 Cue reference tape to entrance point which was set in step 7.

STEP 13 Play back reference tape, and adjust scope vertical control to place peak white bar at a convenient graticule marking on scope.

STEP 14 Press STOP and adjust 1R52 (DEVIATION) to put EE white bar at same graticule marking.

STEP 15 Move jumper 1J2 to A-B position to reconnect modulator AFC loop.

STEP 16 Cue tape to entrance point.

STEP 17 Press PLAY and adjust scope vertical to place video blanking at a convenient graticule marking on the scope.

STEP 18 Press STOP and while in EE operation, adjust 1L3 to place EE blanking on same graticule marking.

STEP 19 Adjust 1R52 (DEVIATION), if necessary, to put EE white bar at same graticule marking. See Figure 3-21 which shows reference tape playback and Figure 3-22 which shows EE signal with 1R16 and 1R52 misadjusted.

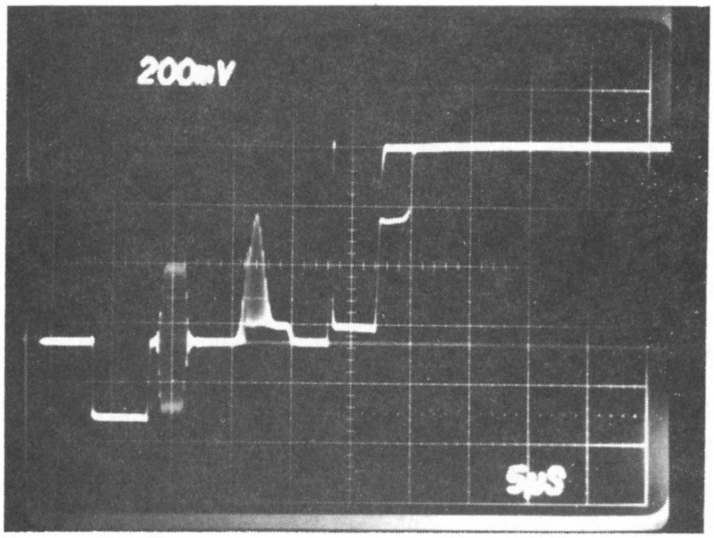


Figure 3-21. Video Reference Tape Playback

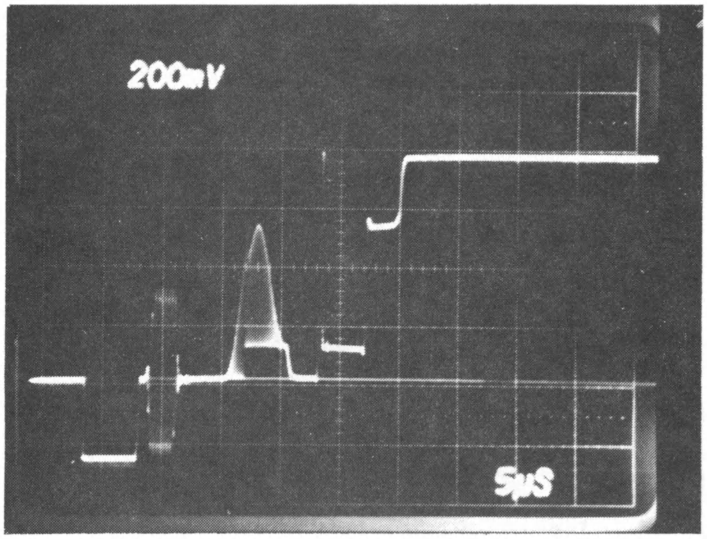


Figure 3-22. EE Signal with 1R16 and 1R52 Misadjusted

Amplitude of signal is greater, and levels of blanking and peak white are shifted downward with respect to playback.

STEP 20 Return jumper 1J13 to A-B position to restore output clamp.

STEP 21 Connect scope to test point 1TP1, and trigger scope on test point 4TP2 (HORIZ).

STEP 22 Rotate VIDEO RECORD level control on control panel to maximum clockwise position.

STEP 23 Adjust 1R36 (OVER DEVIATION CLIP) until clipping of preemphasized pulse *just occurs*. See Figures 3-23 and 3-24.

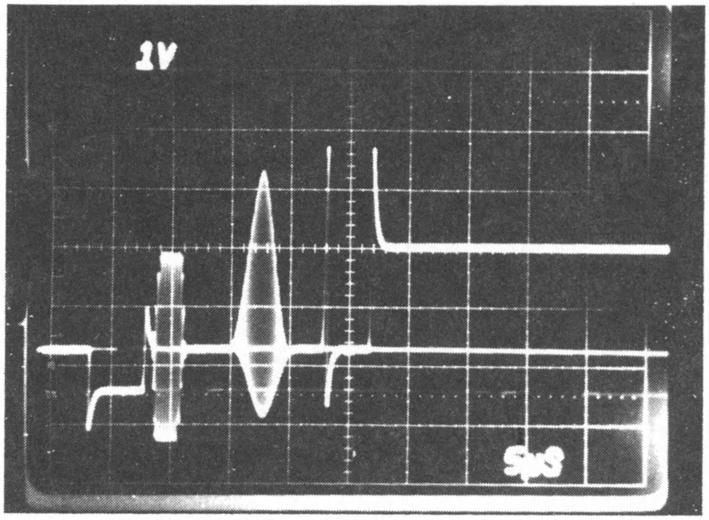


Figure 3-23. Blanking Frequency Misadjusted Full Counterclockwise

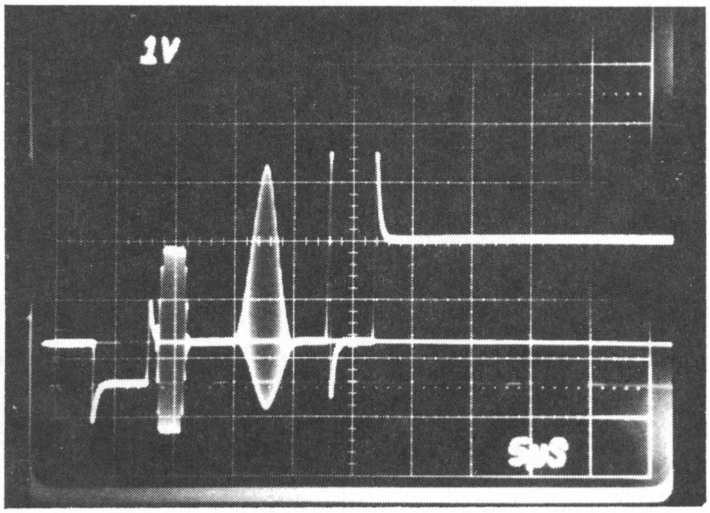


Figure 3-24. Blanking Frequency Correctly Adjusted

STEP 24 Return VIDEO RECORD level control to detent (unity) position.

3-89 Modulator Linearity

It should not be necessary to adjust modulator linearity control unless components in the modulator, primarily 1U2 or 1R28, have been replaced. If linearity is readjusted, it will be necessary to check modulator frequencies as outlined in either paragraph 3-87 or 3-88. Adjust modulator linearity as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Turn VPR-80 power on, and establish the following operating conditions on control panel:

a. Editor off: neither INSERT nor ASSEM indicator is lighted.

b. EE operation: EE indicator lighted.

c. Video record level is unity: VIDEO RECORD level control in detent position.

STEP 3 Connect a modulated pedestal video input to VIDEO IN connector on I/O connector panel. See Figure 3-25.

STEP 4 Connect a waveform monitor to the VIDEO 2 OUT connector. Also, connect the VIDEO 2 OUT to a vectorscope as loop-through from the waveform monitor, and terminate in 75Ω.

STEP 5 With waveform monitor in the low pass (IRE) position, adjust 1R28 (LINEARITY) for flattest pedestal. See Figures 3-26 and 3-27. Use maximum vertical gain on waveform monitor to improve alignment resolution.

STEP 6 There is interaction between LINEARITY control 1R28, the FREQUENCY control 1R16, · and the DEVIATION control 1R52. After adjustment of 1R28, check modulator frequencies as outlined in paragraph 3-87 or 3-88.

STEP 7 Change video input signal to modulated ramp or stairstep.

STEP 8 Remove jumper 1J5, and adjust 1R24 (OFFSET NULL) for minimum differential gain. See Figures 3-28 and 3-29. These waveforms are shown on a Tektronix 520 vectorscope.

STEP 9 Reinstall jumper 1J5 in the A-B (normal) position, and adjust 1R117 (DG CONT) for minimum differential gain. It should be 2% or less. See Figures 3-30 and 3-31. These waveforms are also shown on a Tektronix 520 vectorscope.

Note

Misadjustment of 1R28 (LINEARITY) will increase EE differential phase and gain.

3-90 Demodulator Gain and Frequency Response

Demodulator video gain and frequency response adjustments are made as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Connect a sine-squared pulse and bar, multiburst, 75% color bar video input to the VIDEO IN connector on the I/O connector panel.

STEP 3 Install appropriate high-band carrier video reference tape on transport. Refer to Section 4, Part I, Table 4-4.

STEP 4 Turn VPR-80 power on, and shuttle reference tape to the long section with sine-squared pulse and bar. This recording is about 16 minutes into the tape. Note tape time where this recording begins. Enter an entrance cue for convenience.

STEP 5 Connect a waveform monitor to the VIDEO 2 OUT connector. Also, connect VIDEO 2 OUT to a vectorscope as loop-through from the waveform monitor, and terminate in 75Ω.

STEP 6 Establish the following operating conditions on the control panel:

a. Editor off: neither INSERT nor ASSEM indicator is lighted.

b. EE operation: EE indicator lighted.

c. Video record level is unity: VIDEO RECORD level control in detent position.

d. Ready condition: READY indicator is lighted.

STEP 7 Connect scope probe to test point 1TP30 (DEM VIDEO).

STEP 8 Press PLAY and adjust 1R364 (DEM VID GAIN) for 1 Vp-p from sync tip to peak white.

STEP 9 Press STOP. If the bar is not 1 Vp-p, with the VPR-80 in EE operation, and with sine-squared pulse and bar video input, check modulator frequencies in accordance with paragraph 3-87 or 3-88. Verify that jumper 1J13 is in the A-B position.

STEP 10 With VPR-80 in stop mode/ready condition and EE operation, and multiburst or modulated 12-1/2T (525-line systems) or 20T (625-line systems) pulse and bar as the video input, adjust 1C248 (FREQUENCY RESPONSE) for flat frequency response. See Figures 3-32 and 3-33.

Note

Steps 11 and 12 do not apply to SECAM systems.

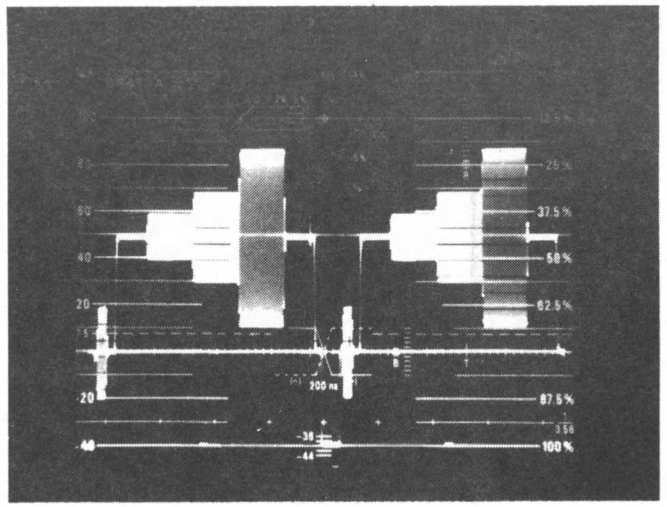


Figure 3-25. Modulated Pedestal Signal

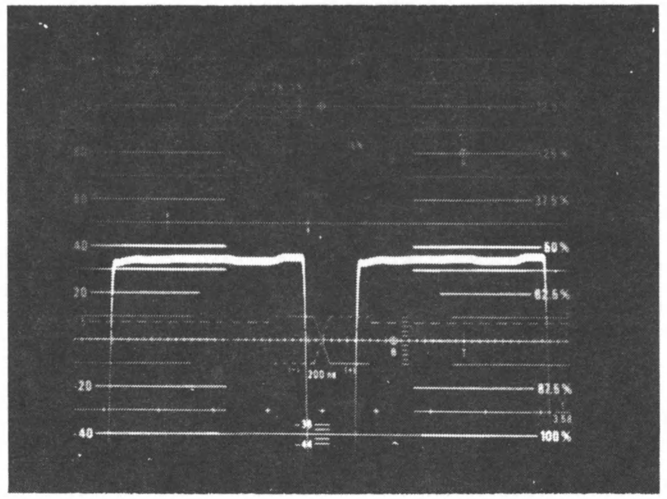


Figure 3-26. Linearity Control (1R28) Misadjusted

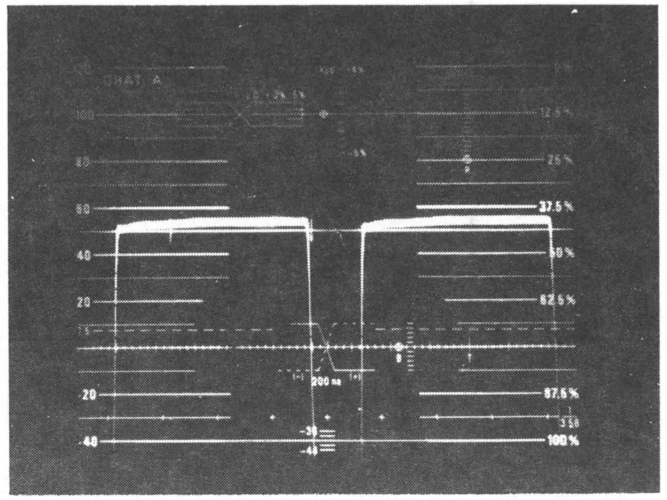


Figure 3-27. Linearity Control (1R28) Correctly Adjusted

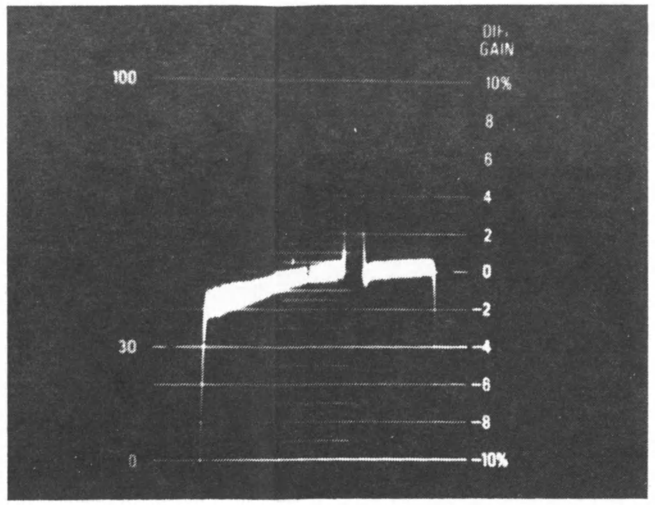


Figure 3-28. Offset Null Control (1R24) Misadjusted

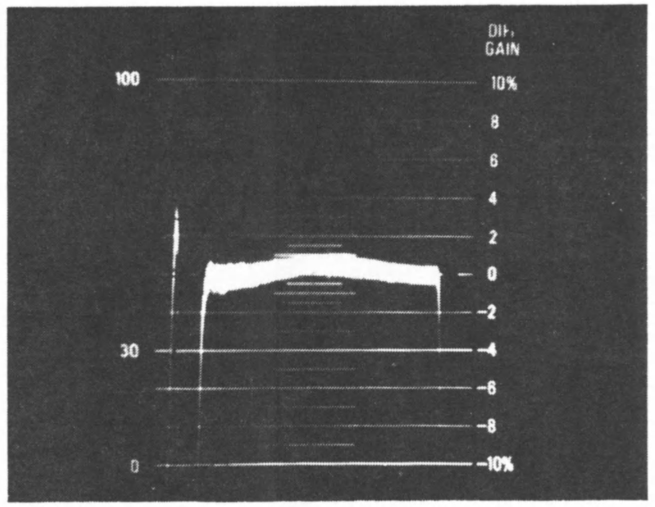


Figure 3-29. Offset Null Control (1R24) Correctly Adjusted

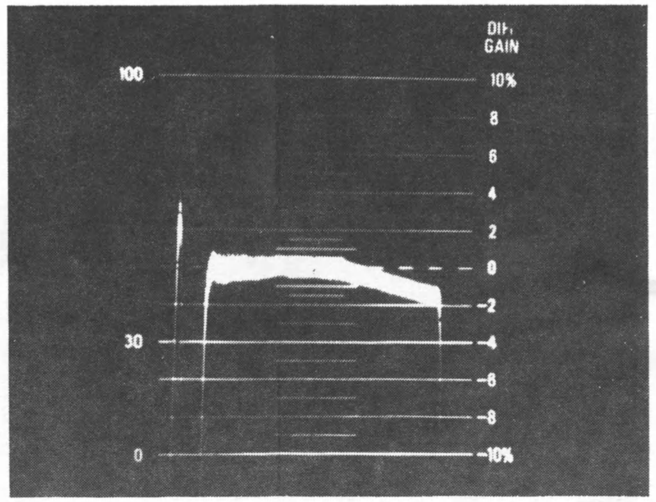


Figure 3-30. Differential Gain Control (1R117) Misadjusted

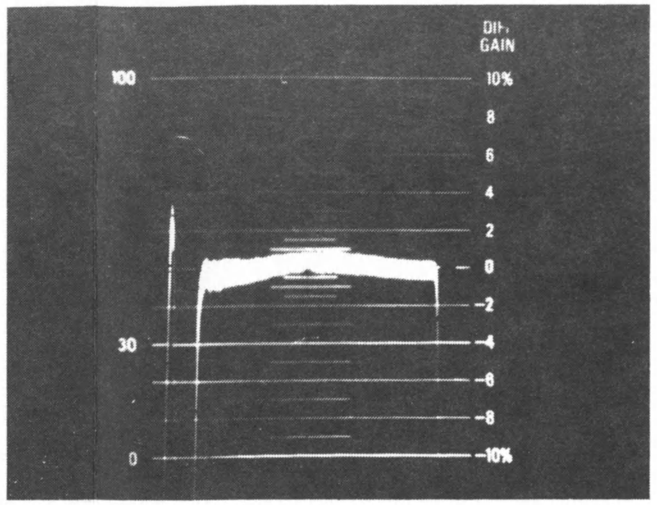


Figure 3-31. Differential Gain Control (1R117) Correctly Adjusted

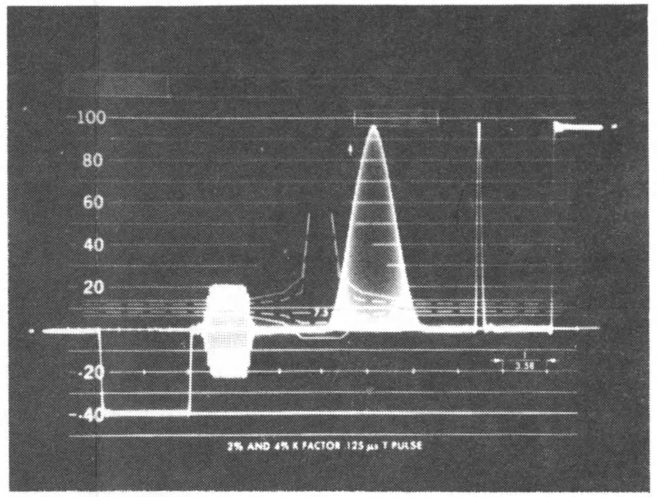


Figure 3-32. Frequency Response Test (12-1/2T Pulse and Bar) With 1C248 Correctly Adjusted

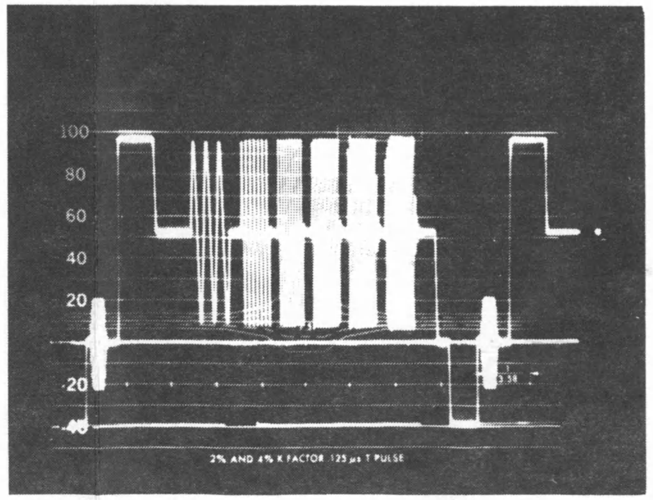


Figure 3-33. Frequency Response Test (Multiburst) With 1C248 Correctly Adjusted

STEP 11 With VPR-80 in stop mode/standby condition and EE operation, and observing 75% color bars, adjust 1R310 to make output burst the same peak-to-peak level as input burst.

STEP 12 Observing vectorscope, adjust 1C165 so that burst-to-chroma phase relationship at demodulator output is the same as input signal. For PAL systems, use vectorscope NTSC vector position. See Figures 3-34 and 3-35 (for NTSC) or Figures 3-36 and 3-37 (for PAL).

STEP 13 Observe on the waveform monitor (or on the scope with probe on test point 1TP30) that video blanking is at 0.0 Vdc.

STEP 14 If VIDEO/RF meter on the VPR-80 control panel is correctly calibrated, it can be used to indicate when demod video level is incorrect. When modulator frequencies have been checked and demod video gain control setting verified, check meter calibration as follows:

a. Press EE: EE indicator is not lighted (tape operation).

b. Press READY: ready indicator is not lighted. Wait for scanner motor to stop.

c. If necessary, adjust 1R209 (RF METER ZERO) so that VIDEO/RF meter indication is as shown in Figure 3-38(A).

d. Press EE: EE indicator lights (EE operation).

e. Press READY: READY indicator lights. Wait for scanner to reach lock speed (SERVO indicator goes off).

f. Adjust 1R241 (VIDEO CALIB) so that VIDEO/RF meter indication is as shown in Figure 3-38(B) (in the center of green area).

3-91 K Factor and Chrominance/Luminance Delay

K factor, as observed on the pulse base line, should be 1% or less. Chroma-to-luminance delay, measured on the modulated pulse, should be 20 ns or less. Adjustment for K factor and chrominance/luminance delay is done as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Turn VPR-80 power on, and establish the following operating conditions on control panel:

a. Editor off: neither INSERT nor ASSEM indicator is lighted.

b. EE operation: EE indicator lighted.

c. Video record level is unity: VIDEO RECORD level control in detent position.

STEP 3 Connect a waveform monitor to the VIDEO 2 OUT connector. Use a K factor graticule.

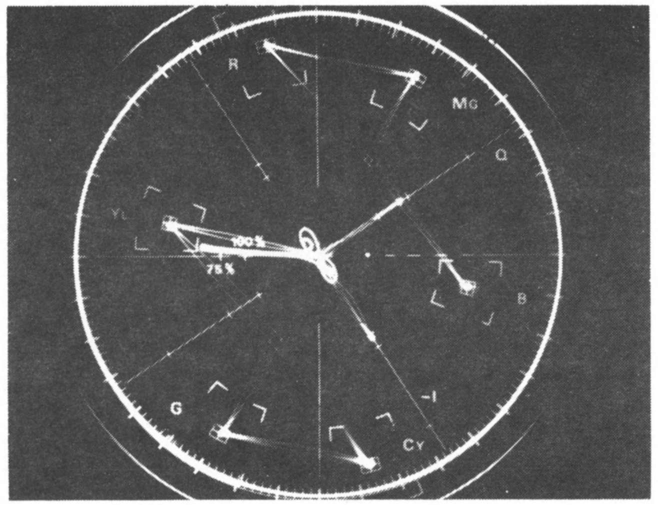


Figure 3-34. Burst-to-Chroma Phase Relationship With 1R310/1C165 Misadjusted (NTSC)

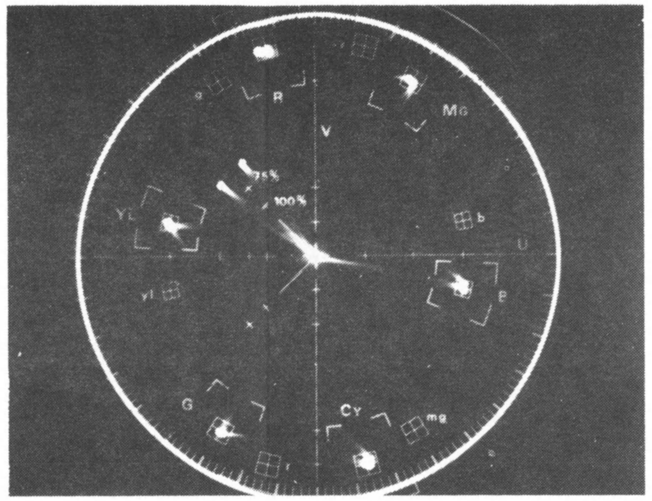


Figure 3-36. Burst-to-Chroma Phase Relationship With 1R310/1C165 Misadjusted (PAL)

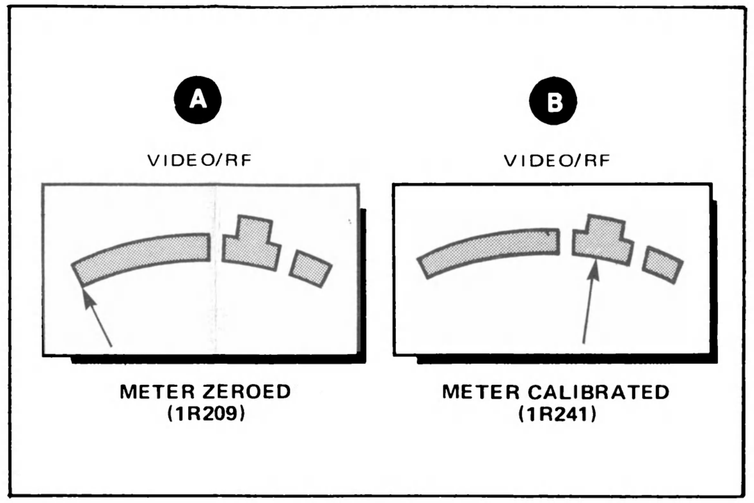


Figure 3-38. VIDEO/RF Meter Calibration

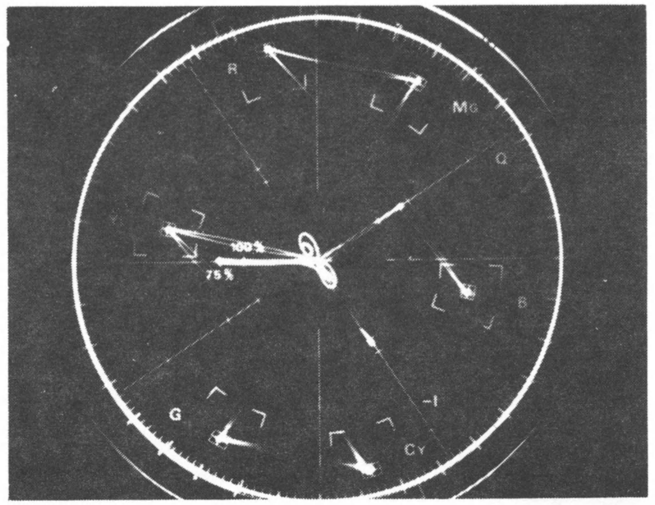


Figure 3-35. Burst-to-Chroma Phase Relationship With 1R310/1C165 Correctly Adjusted (NTSC)

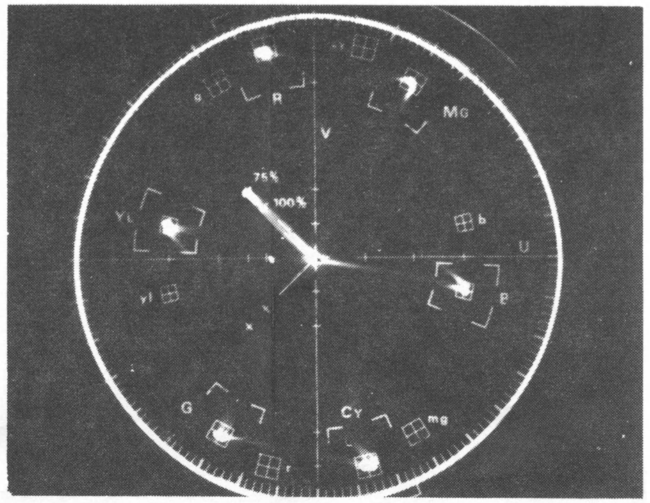


Figure 3-37. Burst-to-Chroma Phase Relationship With 1R310/1C165 Correctly Adjusted (PAL)

STEP 4 Connect a 2T pulse and bar, and 12-1/2T (525-line systems) or 20T (625-line systems) with modulated stairstep or ramp video input to VIDEO IN connector on I/O connector panel.

Note

Some test signal generators have a composite test signal which combines these two signals. See Figures 3-39 and 3-40.

STEP 5 Observe waveform monitor, and, if necessary, adjust 1T6 and 1T7 together for best K factor and chrominance/luminance delay. Do not sacrifice one parameter for the other. See Figures 3-41, 3-42, 3-43 and 3-44. Figure 3-43 shows positive chroma delay.

Delay distortion can be calculated by multiplying peak-to-peak amplitude of the baseline aberration in IRE units (dimension H in Figure 3-45) by the appropriate factor shown in Figure 3-45 for pulse width and frequency being used. Be certain that pulse height is 100 IRE units as shown in Figure 3-45. Otherwise, measurement will be incorrect. If pulse height is incorrect, refer to paragraph 3-90.

3-92 Demodulator Limiter and Detector Balance

Demodulator limiter balance (1R398) and detector balance (1R399) should be adjusted only if a fault, such as increase in moiré, is observed. There are two methods of adjusting these balances. The preferred method employs a spectrum analyzer, and alternate method uses vectorscope indications.

3-93 Preferred Method

The preferred (and more accurate) method is performed as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Connect a moiré test signal (flat red field for NTSC) to VIDEO IN connector on the I/O connector panel. See Figure 3-46.

STEP 3 Connect a spectrum analyzer to the VIDEO 2 OUT connector. Terminate in 75Ω.

STEP 4 Establish the following operating conditions on the control panel:

a. Editor off: neither INSERT nor ASSEM indicator is lighted.

b. EE operation: EE indicator lighted.

c. Video record level is unity: VIDEO RECORD level control in detent position.

d. Standby condition: READY indicator not lighted.

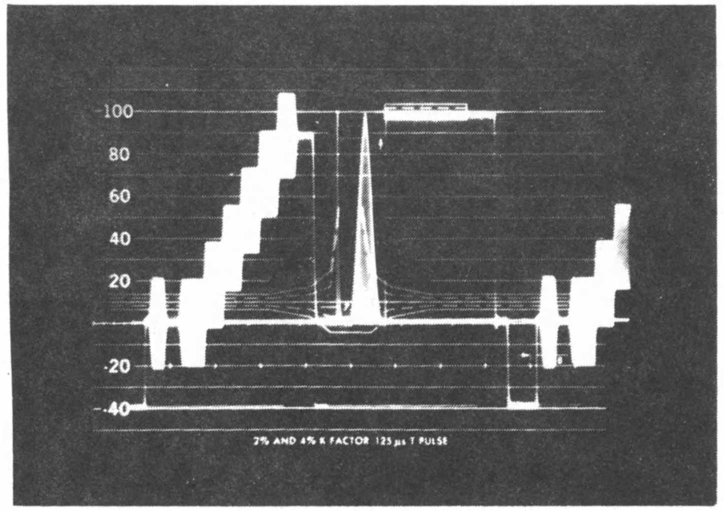


Figure 3-39. NTSC Composite Signal

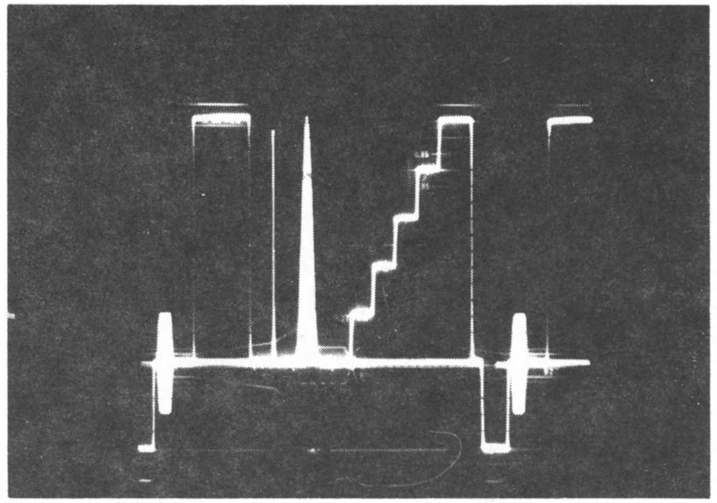


Figure 3-40. PAL Composite Signal

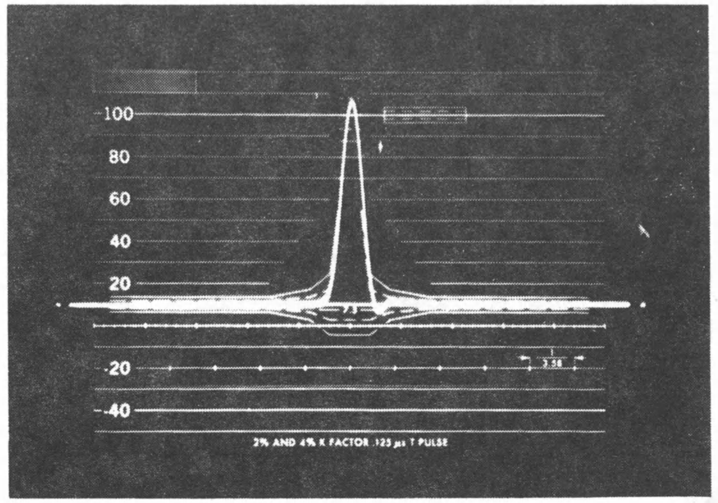


Figure 3-41. NTSC K Factor Misadjusted

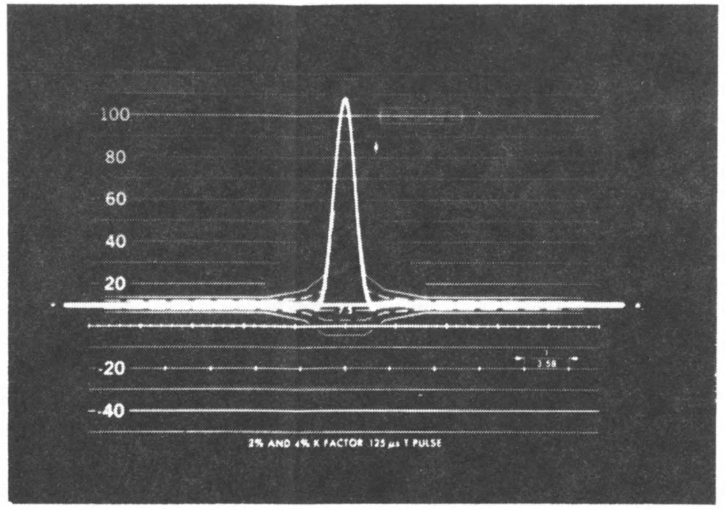


Figure 3-42. NTSC K Factor Correctly Adjusted

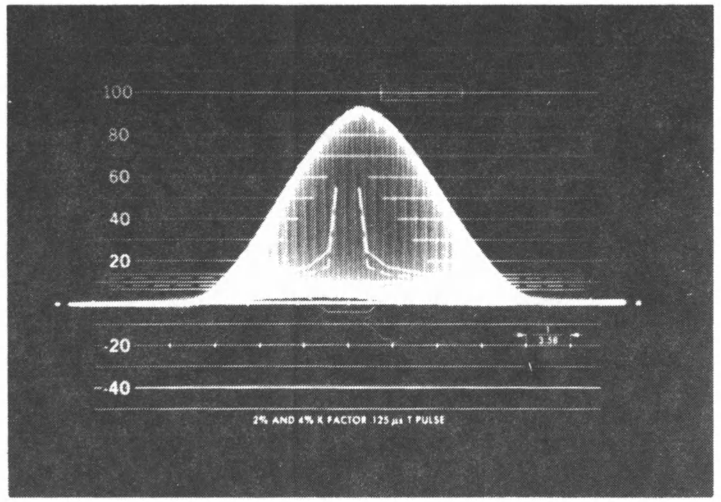


Figure 3-43. NTSC Chrominance/Luminance Delay Misadjusted (12.5T Example)

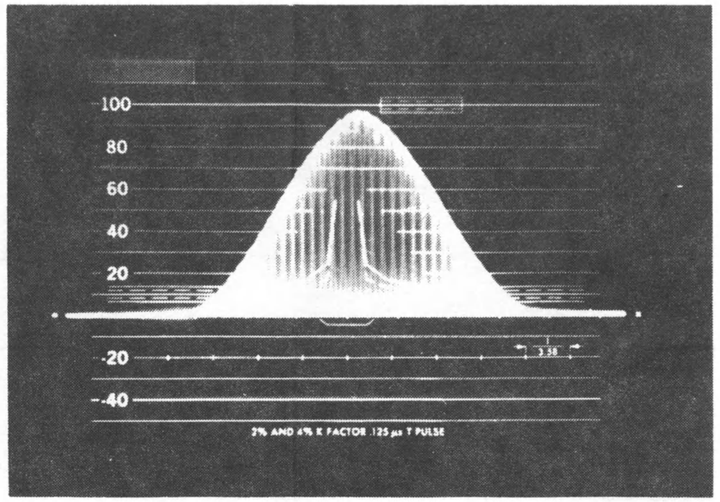
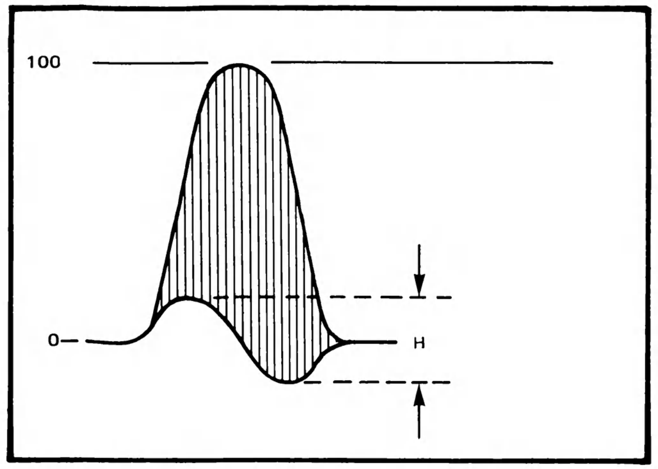


Figure 3-44. NTSC Chrominance/Luminance Delay Correctly Adjusted (12.5T Example)



SUBCARRIER, MHz	3.58	3.58	4.43	4.43
PULSE WIDTH	12.5T	20T	20T	10T
DELAY, ns/IRE	10	15.9	12.7	6.4

Figure 3-45. Chrominance/Luminance Delay Measurement Technique

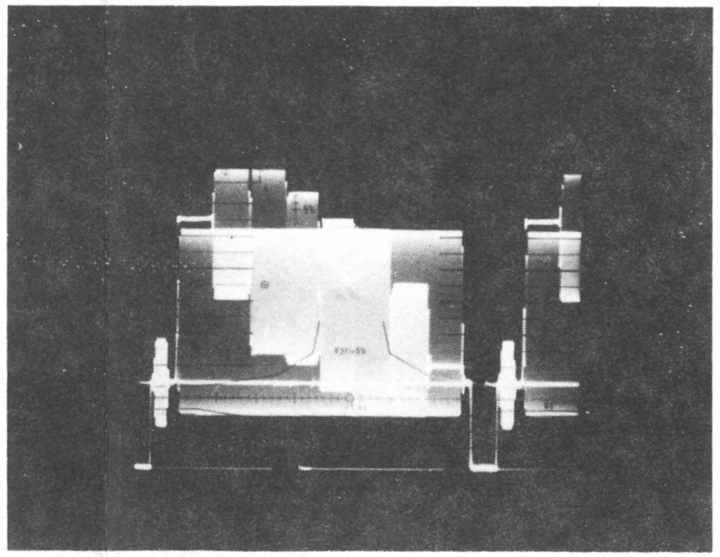


Figure 3-46. Moiré Test Signal

STEP 5 Adjust 1R398 (LIMITER BAL) and 1R399 (DETECTOR BAL) for minimum second harmonic moiré component. See Figures 3-47 and 3-48.

Video System	**Second Harmonic**	**Third Harmonic**
NTSC	4.8 MHz	2.7 MHz
PAL (625)	3.5 MHz	2.6 and 7.1 MHz

The third harmonic moiré component cannot be removed by adjustment.

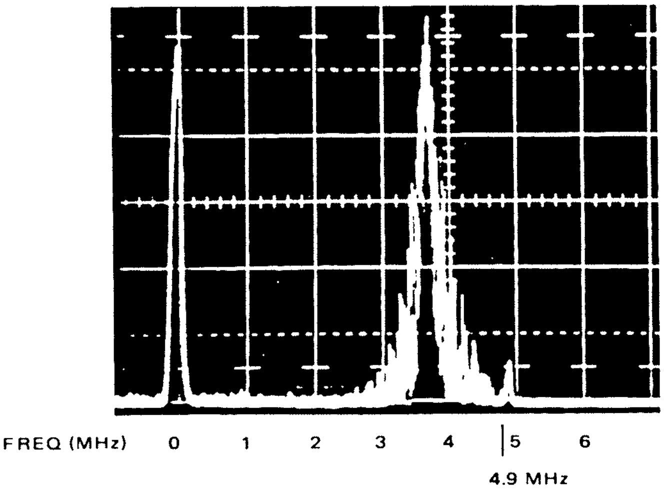


Figure 3-47. Demodulator Limiter Balance (1R398) and Demodulator Detector Balance (1R399) Misadjusted—Spectrum Analyzer

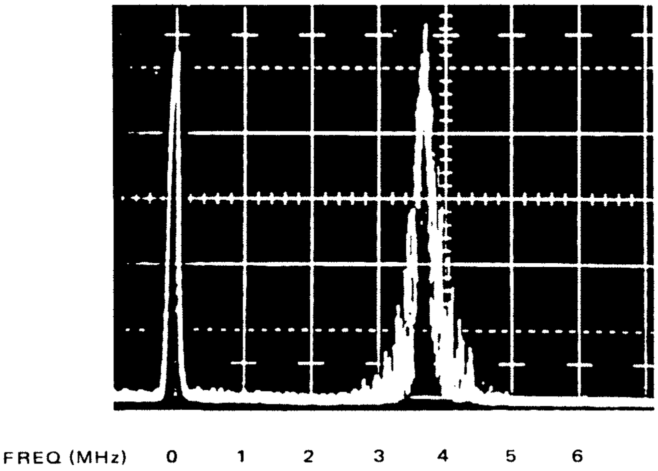


Figure 3-48. Demodulator Limiter Balance (1R398) and Demodulator Detector Balance (1R399) Correctly Adjusted—Spectrum Analyzer

3-94 Alternate Method

The alternate (and less accurate) method is performed as follows:

STEP 1 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 2 Connect a color bar test signal to VIDEO IN connector on I/O connector panel.

STEP 3 Connect a vectorscope to the VIDEO 2 OUT connector. Terminate in 75Ω.

STEP 4 Establish the following operating conditions on control panel:

a. Editor off: neither INSERT nor ASSEM indicator is lighted.

b. EE operation: EE indicator lighted.

c. Video record level is unity: VIDEO RECORD level control in detent position.

d. Standby condition: READY indicator not lighted.

STEP 5 Observe blue dot (NTSC) or cyan dot (PAL). To increase accuracy, increase gain of the vector display and shift center position to left to better observe blue or cyan dot. See Figures 3-49 and 3-50 (NTSC) or 3-51 and 3-52 (PAL) which show vector display on a Tektronix 520 Vectorscope.

STEP 6 Adjust 1R398 (LIMITER BAL) and 1R399 (DETECTOR BAL) for smallest vector dot.

Note

1R398 (LIMITER BAL) and 1R399 (DETECTOR BAL) are interactive. It may be easier to first align 1R398, and then 1R399. 1R398 has a broad range while 1R399 has a sharp null.

The cyan vector, used on PAL 625 for the adjustment of 1R398, will have two smoke rings, as shown in Figure 3-53. These are second and third harmonic moiré. The second harmonic is adjustable, whereas the third is not. Therefore, the cyan dot will always have one smoke ring (the third harmonic moiré).

3-95 RF Equalizer Automatic Gain Control

The setup of the automatic gain control (AGC) in the rf equalizer portion of the Mod/Demod PWA establishes the correct level into the dropout detector. Dropout starts at a threshold of -12 dB. Set up rf equalizer AGC as follows:

STEP 1 Connect a color-bar test signal to the VIDEO IN connector on the I/O connector panel.

STEP 2 Set VIDEO RECORD level control to unity (detent) position.

STEP 3 Thread a work tape on the transport, and make a short recording (2 minutes minimum) of 75% color bars. Rewind the tape.

STEP 4 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 5 Turn on VPR-80 power, and connect scope probe to test point 1TP17 (INPUT RF). Trigger scope on test point 4TP12 (REF VERT) on AST Servo PWA. See Figure 5-66.

STEP 6 Press PLAY, and observe scope. Rf level at 1TP17 should be 250 mVp-p ±40 mV (for 525-line systems) or 200 mVp-p ±40 mV (for 625-line systems). This verifies proper operation of the rotary transformer, video record/playback head, and the Preamplifier PWA in the scanner assembly.

Note

Scanner preamplifier gain (R3) is aligned at the factory on a special test fixture.

STEP 7 To set AGC gains, turn off VPR-80 power, and place Mod/Demod PWA on an extender.

STEP 8 Turn on VPR-80 power, and move scope probe to test point 1TP21. Enter play mode, and adjust 1R232 (AGC RF LEVEL) for 300 mVp-p.

STEP 9 Move scope probe to Mod/Demod PWA edge connector pin 65. Adjust 1R235 (AST RF GAIN) for a 3.5-Vp-p signal. See Figure 3-54.

STEP 10 Press STOP and then press READY. Allow scanner motor to come to a stop.

STEP 11 Press EE switch: EE indicator should be off.

STEP 12 Observe VIDEO/RF meter on control panel, and, if necessary, adjust 1R209 (METER ZERO) so that meter needle points to *left edge* of white bar on meter face. Refer to Figure 3-38.

STEP 13 Place VPR-80 in normal (nonedit) record mode, and make a one-minute recording. Rewind tape.

STEP 14 Place VPR-80 in normal playback of recording made in step 13, and observe VIDEO/RF meter.

STEP 15 Adjust 1R215 (RF METER CALIBRATE) to set meter needle to the black strip after green area for normal playback rf levels.

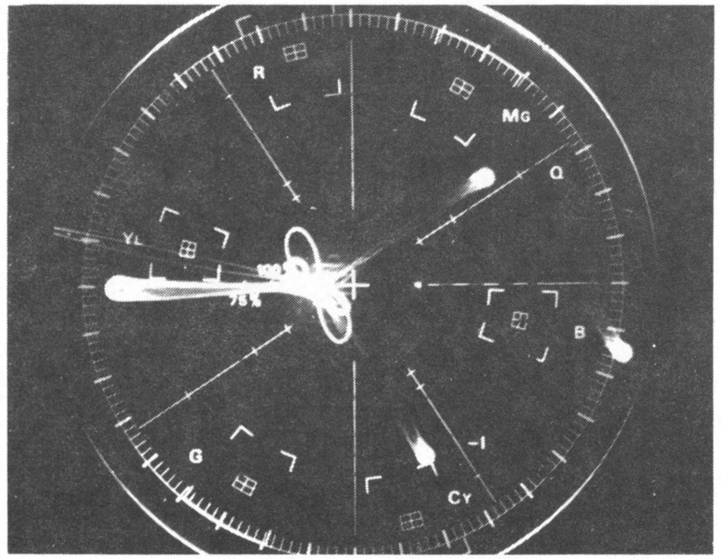


Figure 3-49. Demodulator Detector Balance Misadjusted (NTSC)

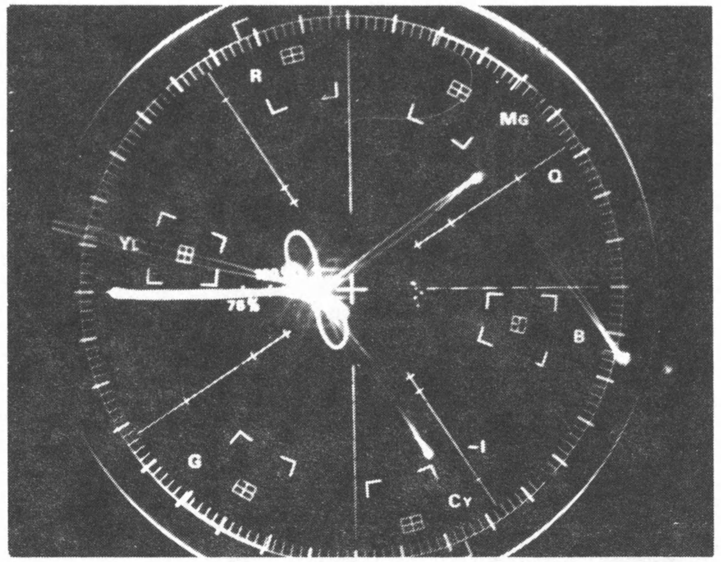


Figure 3-50. Demodulator Limiter Balance and Demodulator Detector Balance Correctly Adjusted (NTSC)—Vectorscope

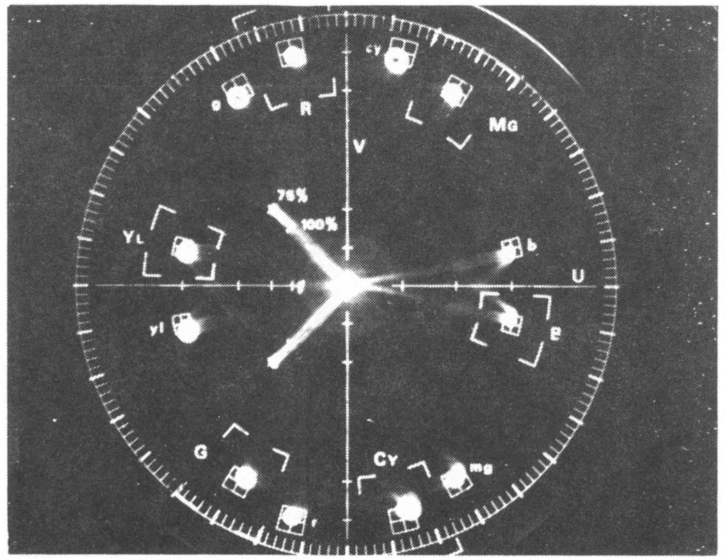


Figure 3-51. Demodulator Limiter Balance and Demodulator Detector Balance Misadjusted (PAL)—Vectorscope

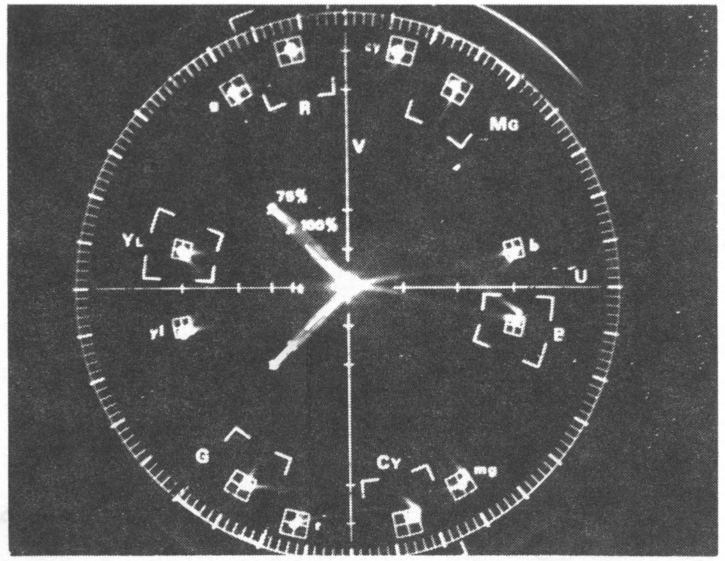


Figure 3-52. Demodulator Limiter Balance and Demodulator Detector Balance Correctly Adjusted (PAL)—Vectorscope

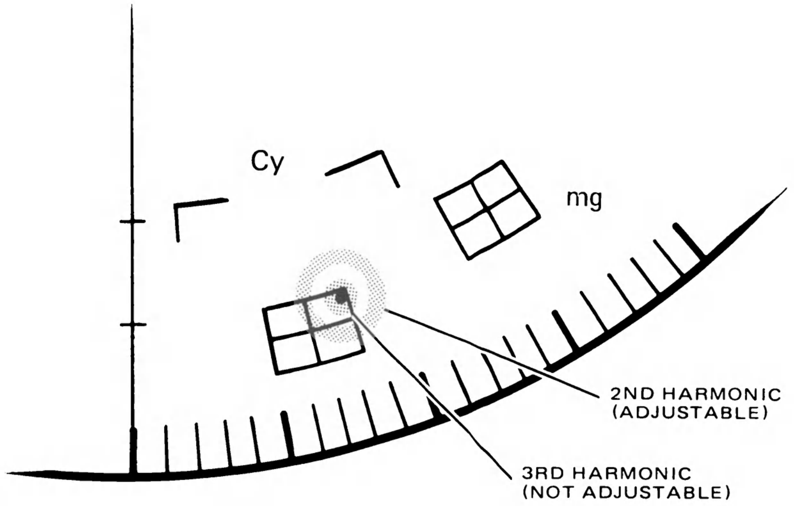


Figure 3-53. Cyan Vector Dot and Smoke Rings

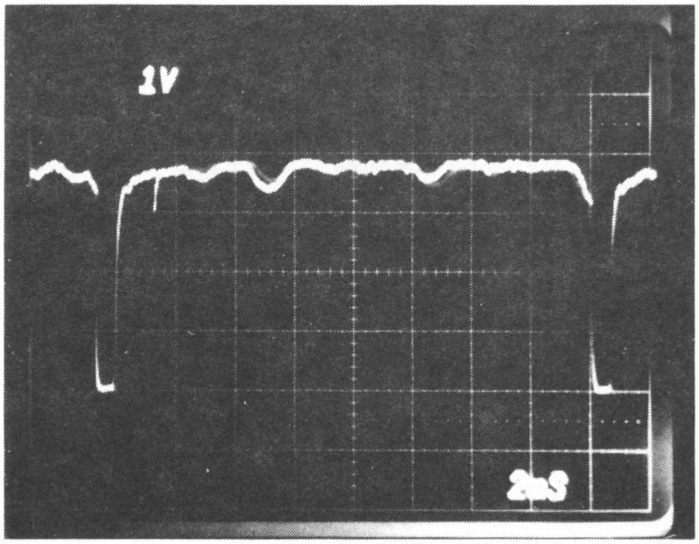


Figure 3-54. AST Detected RF Signal—PWA1, Pin 65

3-96 RF Equalizer Alignment and Centering

Alignment of the rf equalizer is not a routine maintenance procedure. It is required only when there are indications that the equalizer range is incorrect. Figures 3-55, 3-56, and 3-57 show the range of the EQUALIZATION control on the primary control panel. This control is operable only when in manual equalization mode which is indicated by the lighted CHROMA EQUAL indicator (on secondary control panel). A similar range can be expected when chroma equalization is done automatically (CHROMA EQUAL indicator not lighted). Automatic operation, of course, assumes that the sync burst ratio of the off-tape signal is correct.

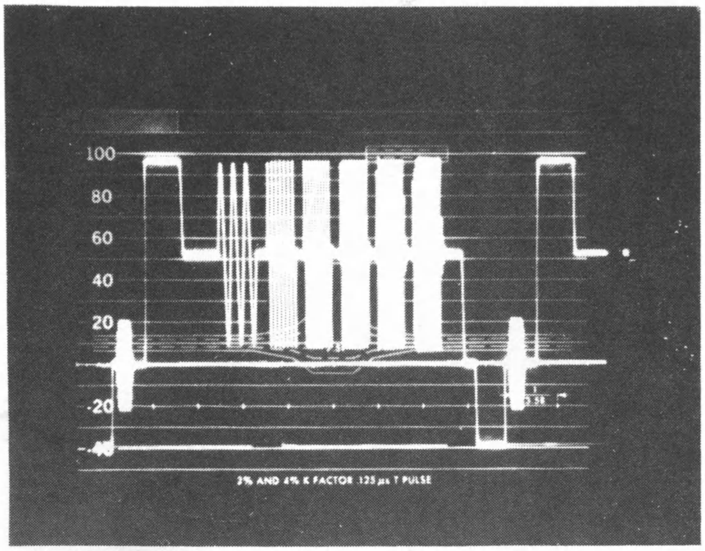


Figure 3-55. Equalization Flat Response

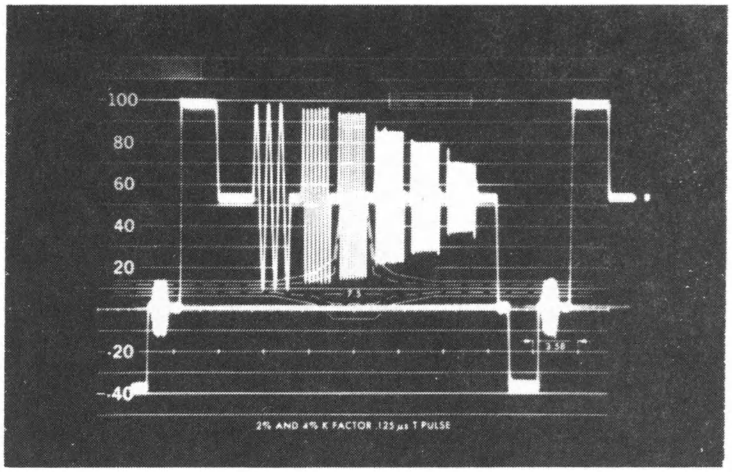


Figure 3-56. EQUALIZATION Control Maximum Counterclockwise

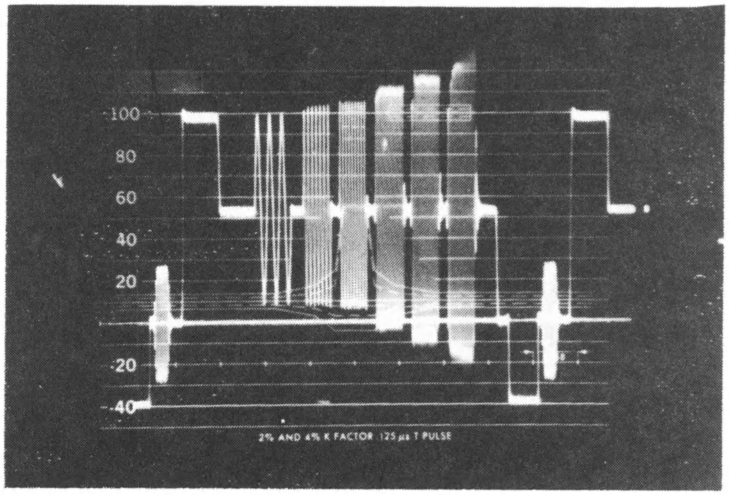


Figure 3-57. EQUALIZATION Control Maximum Clockwise

Inadequate equalizer range is indicated when, on a tape interchange basis, or with use of the Format C High-band Carrier Video Reference tape, flat frequency response cannot be attained. Excessive equalizer range is indicated when picture breakup occurs (black streaks from whites) with the manual EQUALIZATION control rotated fully clockwise. Excessive equalizer range is also indicated when, with EQUALIZATION control rotated full counterclockwise, burst amplitude is sufficiently reduced at the demodulator output so that the TBC switches to monochrome, deleting burst at the output.

Align and center the equalizer as follows:

STEP 1 Thread a work tape on the transport, and make a short recording of multiburst signal for equalizer alignment and modulated ramp or stairstep for differential gain alignment. Reference tapes contain both of these signals and can be used in this procedure. Refer to Section 4, Part I, Table 4-5. Rewind tape.

STEP 2 With VPR-80 power off, place Mod/Demod PWA on an extender.

STEP 3 Connect a waveform monitor to the VIDEO 2 OUT connector on the I/O connector panel. Also, connect the VIDEO 2 OUT to a vectorscope as loop-through from the waveform monitor, and terminate in 75Ω.

STEP 4 Establish the following operating conditions on the control panel:

a. Off-tape operation: EE indicator not lighted.

b. EQUALIZATION control enabled: CHROMA EQUAL indicator lighted.

c. EQUALIZATION control in detent position.

STEP 5 On the Mod/Demod PWA, set differential gain control 1R133 (DG CONT) to center detent.

STEP 6 Place scope probe on test point 1TP37, and adjust 1R134 for 0 Vdc ±50 mV.

STEP 7 Press PLAY switch.

STEP 8 Adjust 1R147 (EQUALIZATION RANGE) and 1R188 (DIFFERENTIAL GAIN CENTER) for flat frequency response (multiburst) on the waveform monitor, and minimum differential gain (modulated ramp/stairstep) on the vectorscope in DG mode.

Note

These controls interact. Do not sacrifice one value for the other.

With the equalizer set for flat frequency response, differential gain should be ±2% or better. Refer to Figure 3-55, and see Figure 3-58.

STEP 9 Play back the multiburst recording, and ensure that CHROMA EQUAL indicator is lighted. Vary EQUALIZATION control from full counter-clockwise to full clockwise. At subcarrier burst in the multiburst signal, the equalizer should have a range of:

System	Maximum	Minimum
NTSC	±20 IRE	±10 IRE
PAL	±14 mV	±7 mV

Refer to Figures 3-56 and 3-57.

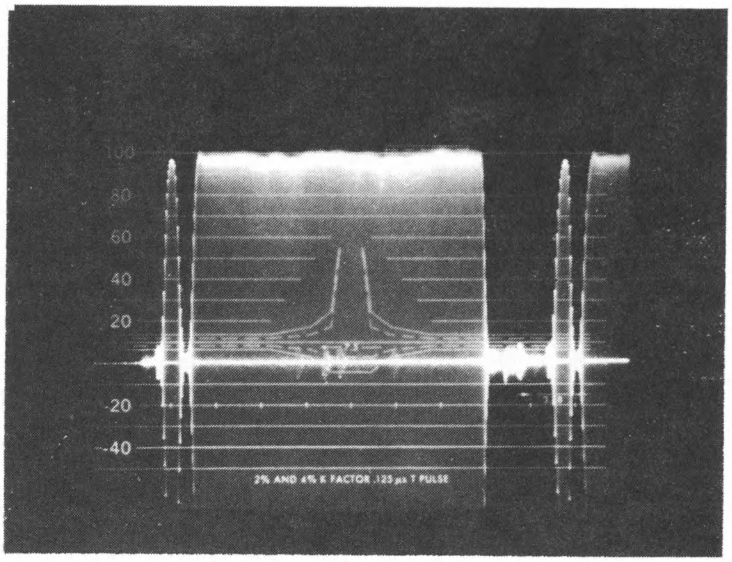


Figure 3-58. Vectorscope Display—Differential Gain Mode

STEP 10 Connect scope probe to test point 1TP25 (GATED BURST), and trigger scope on test point 4TP6 on AST Servo PWA. (See Figure 5-66.) Adjust 1L22 for maximum burst signal at 1TP25.

STEP 11 Rotate EQUALIZER control to detent position, and press CHROMA EQUAL/MANUAL switch.

STEP 12 With CHROMA EQUAL indicator not lighted (automatic equalization), play back the multiburst recording, and adjust 1R292 (AUTOCHROMA UNITY CALIB) for flat frequency response. This calibrates autochroma mode of operation for NTSC, PAL, and PAL-M systems.

Note

Control 1R342 (SECAM CHROMA LEVEL) is used to compensate for burst amplitude in PAL, and to compensate for line chroma amplitude in SECAM. 1R342 should need alignment only if the auto equalizer calibration changes when switching from PAL to SECAM in PAL/SECAM systems.

STEP 13 Press SHUTTLE and rotate tape speed control to shuttle STOP position (tape speed control pointer dot centered at top of knob).

STEP 14 Ensure that EE indicator is not lighted, and adjust tape speed control as necessary to freeze waveform monitor display on multiburst signal.

STEP 15 Adjust 1R150 (SHUTTLE EQUALIZER) for flat frequency response.

STEP 16 To check the range of 1R133 (DG CONT), the PWA edge differential gain control, play back the modulated ramp/stairstep recording and observe output on the vectorscope in differential gain mode of operation. Adjust 1R133 from full counterclockwise to full clockwise, then return to the center detent position. The range of differential gain should be approximately ±8%. This is not a specification, but merely a verification of the differential gain control operating range. See Figures 3-59 and 3-60.

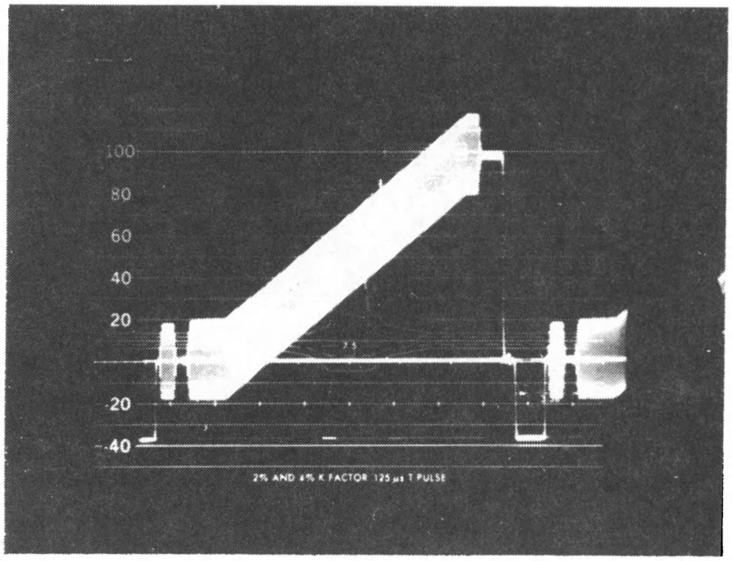


Figure 3-59. Waveform Monitor Display of Modulated Ramp Playback

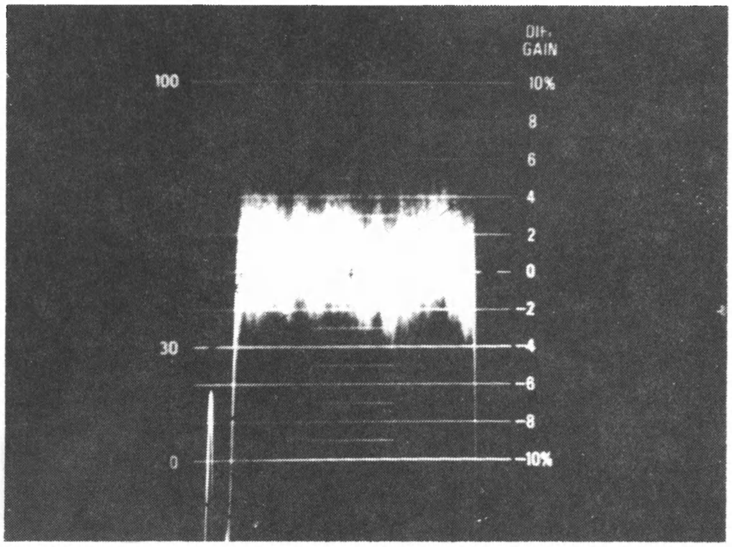


Figure 3-60. Vectorscope (Differential Gain Mode) Display of Modulated Ramp Playback

STEP 17 To set PWA edge differential phase control, 1R248 (DP CONT), connect input of the vectorscope to the VIDEO OUT connector of the time-base corrector, and play back the modulated ramp/stairstep signal. Adjust 1R248 for minimum differential phase. See Figures 3-61 and 3-62.

STEP 18 Recheck differential gain, and, if necessary, readjust 1R188 (DG CENTER).

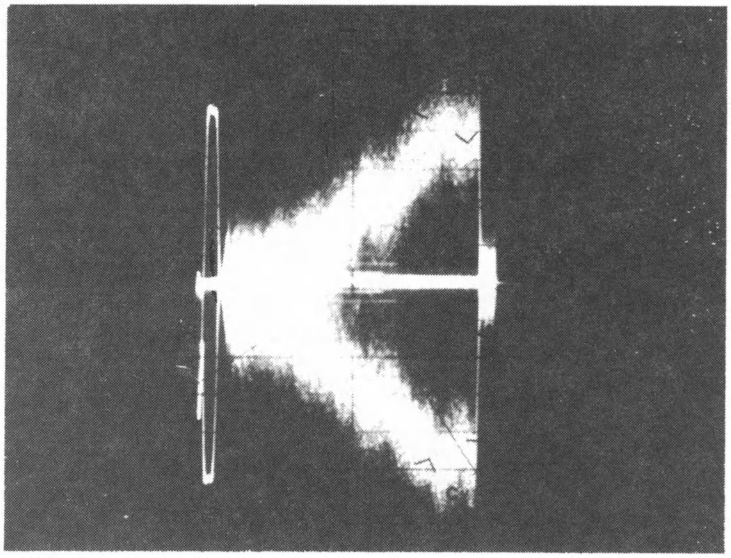


Figure 3-61. Vectorscope (Differential Phase Mode) Control 1R248 Misadjusted

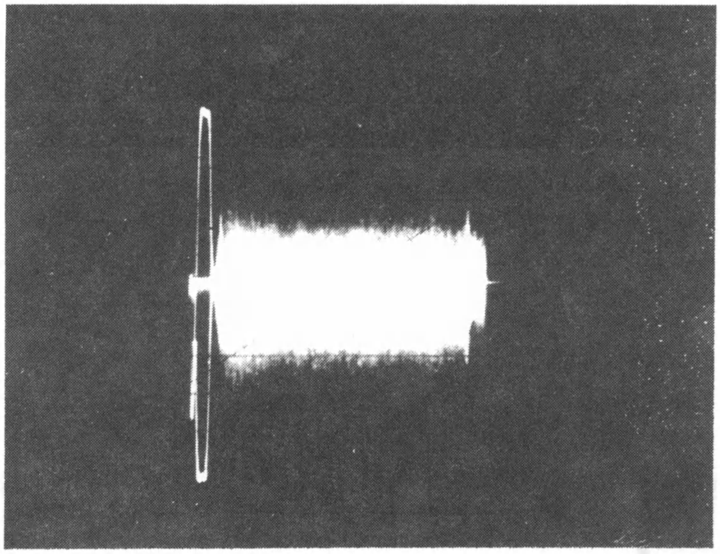


Figure 3-62. Vectorscope (Differential Phase Mode) Control 1R248 Correctly Adjusted (Vectorscope Misadjusted for Photo)

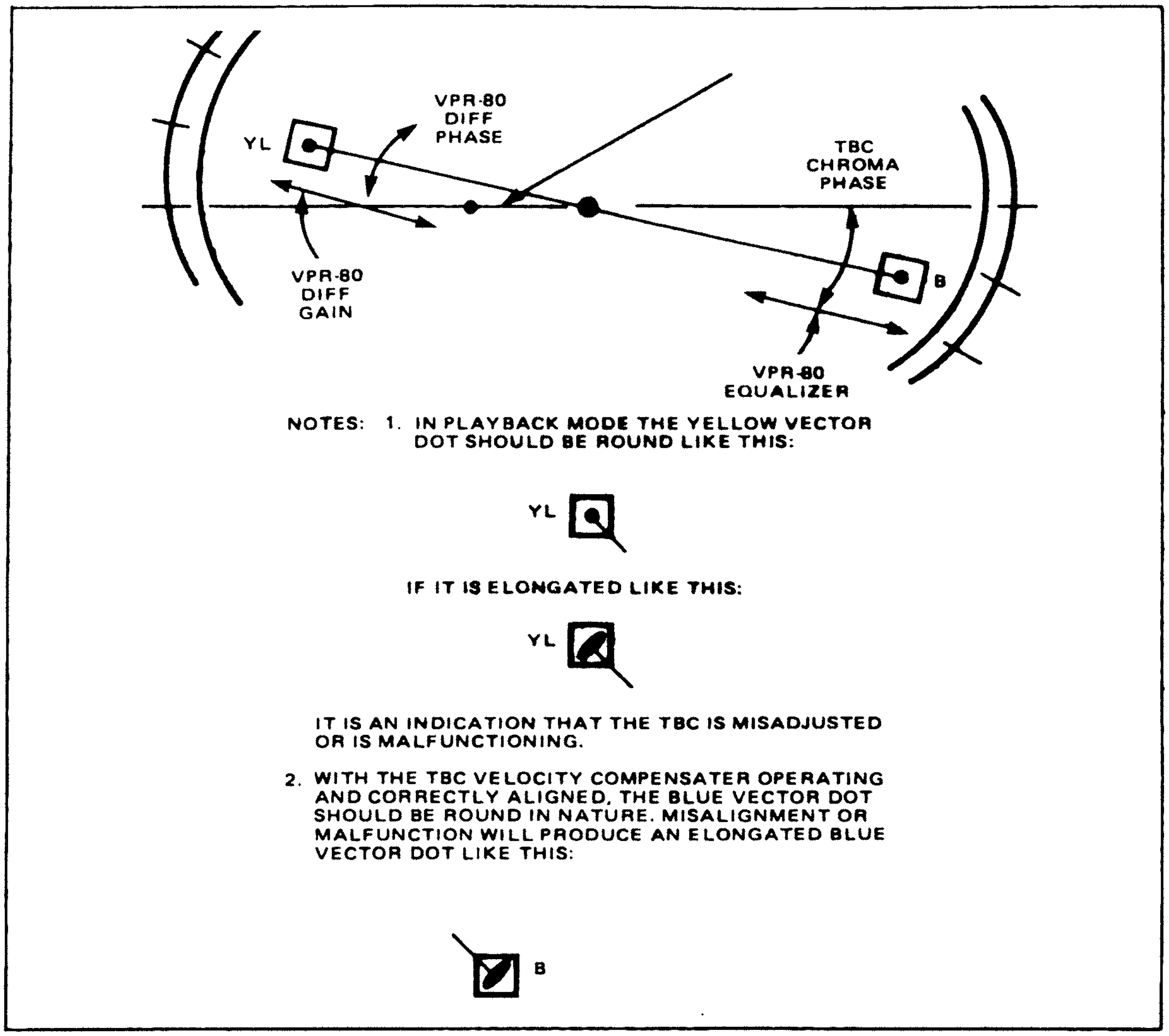
Figure 3-63 shows how to evaluate a color bar playback for signal system misadjustments or faults.

a. Observe first that in EE the color bars are correctly located in their respective boxes. Then play back reference tape. With signal system controls all in unity (detent) position, incorrect chroma level of the blue vector indicates misadjustment of the equalizer centering controls.

b. Incorrect level of the yellow vector indicates the presence of differential gain.

c. Incorrect phase of the blue vector indicates TBC chroma phase variable/unity misalignment.

d. Incorrect phase of the yellow vector indicates VPR-80 or TBC differential phase misalignment. Alignment of the TBC velocity



NOTES: 1. IN PLAYBACK MODE THE YELLOW VECTOR DOT SHOULD BE ROUND LIKE THIS:

IF IT IS ELONGATED LIKE THIS:

IT IS AN INDICATION THAT THE TBC IS MISADJUSTED OR IS MALFUNCTIONING.

2. WITH THE TBC VELOCITY COMPENSATER OPERATING AND CORRECTLY ALIGNED, THE BLUE VECTOR DOT SHOULD BE ROUND IN NATURE. MISALIGNMENT OR MALFUNCTION WILL PRODUCE AN ELONGATED BLUE VECTOR DOT LIKE THIS:

Figure 3-63. Effect of Adjustment on Yellow and Blue Vectors

compensator should be verified before alignment of VPR-80 differential phase controls. Refer to step 17.

3-97 Video Erase Drive

Evidence of what appears to be moiré when recording color bars over color bars may be an indication of incorrect or missing video erase drive. Normal record mode checks longitudinal video erase assembly, and insert edit mode checks scanner video erase assembly.

3-98 Bulk Erase

The video bulk erase drive circuitry is located on the Audio PWA. Set the level of the video bulk erase drive as follows:

STEP 1 Connect a video input of any convenient test signal to the VIDEO IN connector on the I/O connector panel.

STEP 2 With VPR-80 power off, thread a blank work tape on transport.

STEP 3 Open VPR-80 rear door assembly.

STEP 4 Disengage four captive screws securing shield over Audio PWA, and detach shield.

STEP 5 Connect scope probe to Audio PWA test point TP5 (VIDEO ERASE). See Table 4-9.

STEP 6 Turn VPR-80 power on, and press PLAY and RECORD switches at the same time.

STEP 7 Observe scope and adjust R190 on Audio PWA for 1.2 Vp-p. See Table 4-10.

3-99 Edit Erase

Malfunction of video edit erase is most probably due to head failure. There is less chance of malfunction in the edit erase drive.

The video edit erase drive circuitry is located on the Record Amplifier and Edit Erase PWA. Set the frequency of the video edit erase drive as follows:

STEP 1 Thread a blank work tape on the transport.

STEP 2 Connect a sine-squared pulse and bar signal to the VIDEO IN connector on the I/O connector panel.

STEP 3 Turn on VPR-80 power, and zero the tape timer. Ensure that MASTER RECORD LOCKOUT indicator is not lighted.

STEP 4 Make a one-minute recording at studio operating level. Rewind tape.

STEP 5 Press INSERT and then PLAY. Observe tape time display.

STEP 6 After 10 seconds of play mode, press PLAY and RECORD at the same time.

STEP 7 After 20 seconds of record mode, press STOP and rewind tape.

STEP 8 Press PLAY and observe picture monitor. Look for evidence of what appears to be moiré between 10 and 30 seconds of tape time. If such evidence exists, continue with steps 9 through 14.

STEP 9 Unthread tape, turn VPR-80 power off, and remove transport trim as described in Part I, paragraph 4-12.

STEP 10 With VPR-80 power off, remove three no. 4 screws and washers securing shield over Record Amplifier and Edit Erase PWA, and detach shield. Refer to Figure 3-13.

STEP 11 Rethread work tape on transport. Slowly shuttle tape to beginning of recording made in step 4, and press STOP.

STEP 12 Connect scope probe to test point TP1 on Record Amplifier and Edit Erase PWA. Trigger scope on reference point. (See Figure 3-66.)

STEP 13 Ensure that INSERT indicator is lighted, and that MASTER RECORD LOCKOUT indicator is not lighted.

STEP 14 Enter record mode and observe scope. Edit erase drive waveform should be as shown in Figure 3-64. If necessary, adjust L1 for maximum amplitude (typically 40 Vp-p).

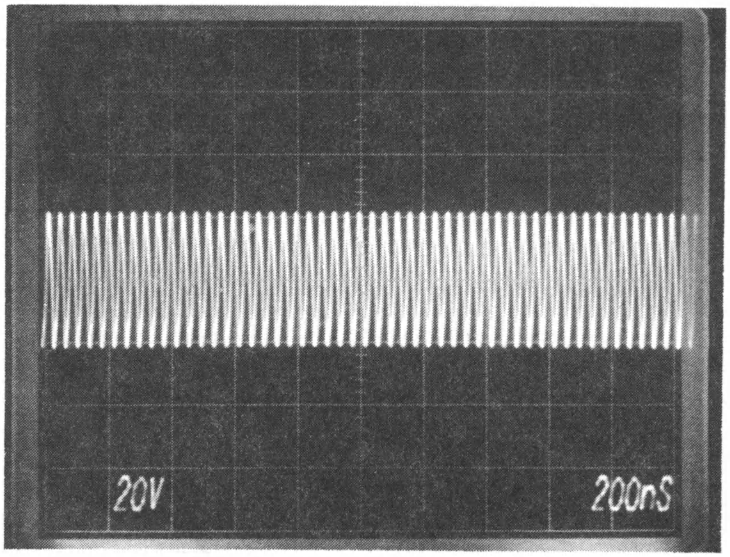


Figure 3-64. Video Edit Erase Drive—L1 Correctly Adjusted

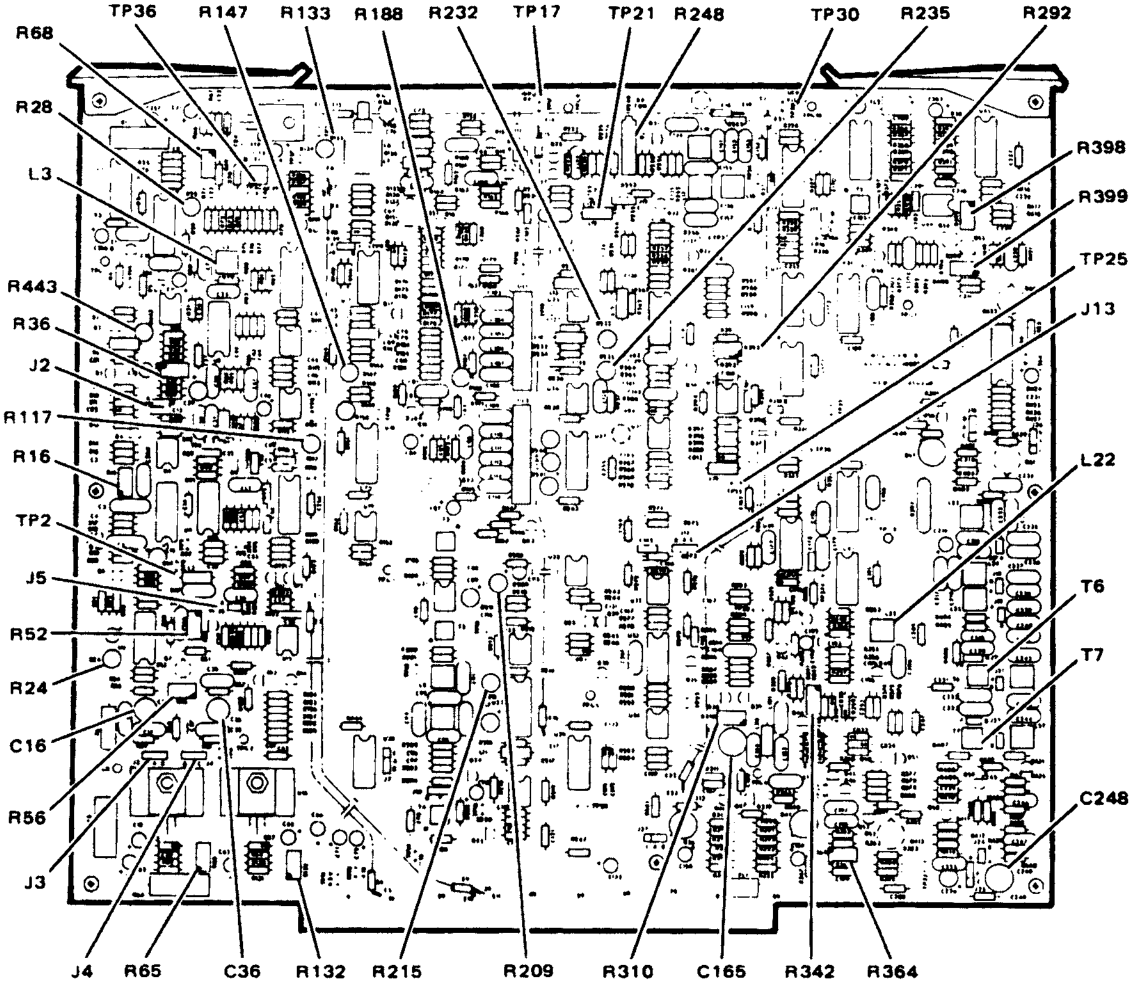


Figure 3-65. Modulator/Demodulator PWA, NTSC, PAL-M Modulator/Demodulator PWA, PAL/SECAM Jumpers, Test Points, and Adjustment Controls

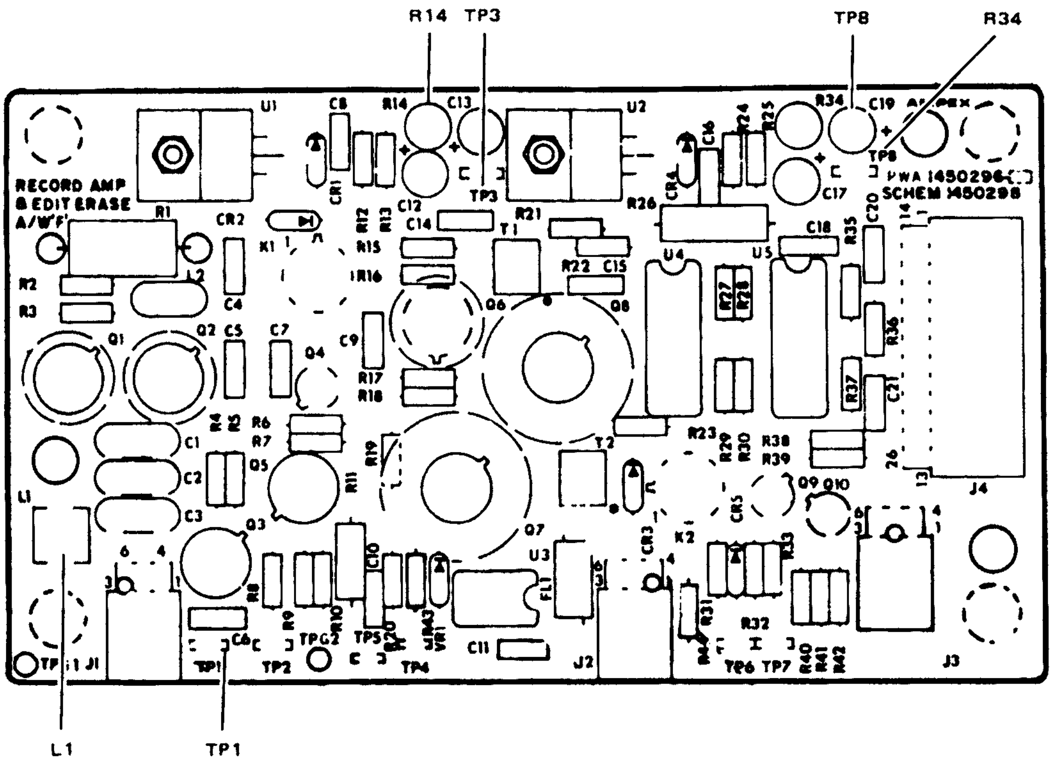


Figure 3-66. Record Amplifier and Edit Erase PWA
Test Points and Adjustment Controls

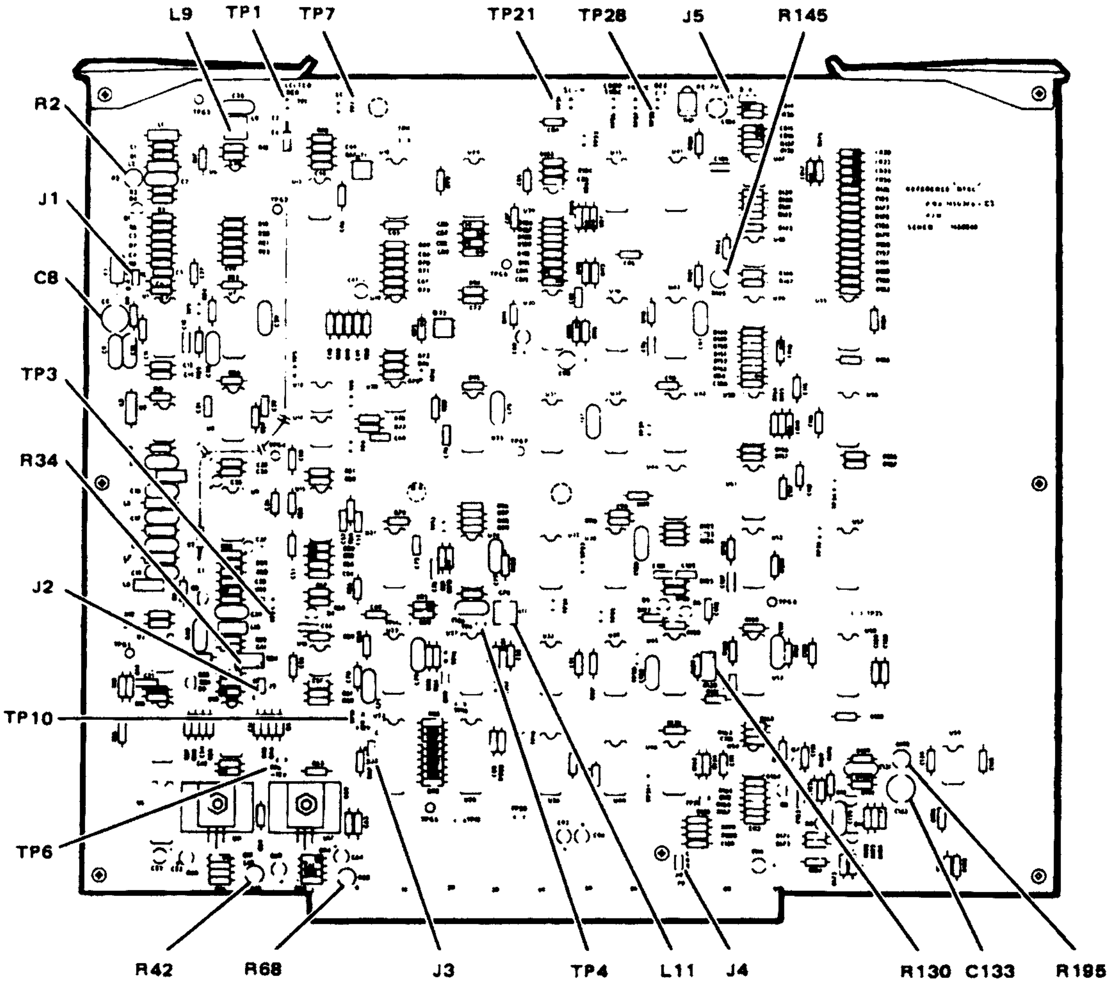


Figure 3-67. Reference PWA, NTSC
Jumpers, Test Points, and Adjustment Controls

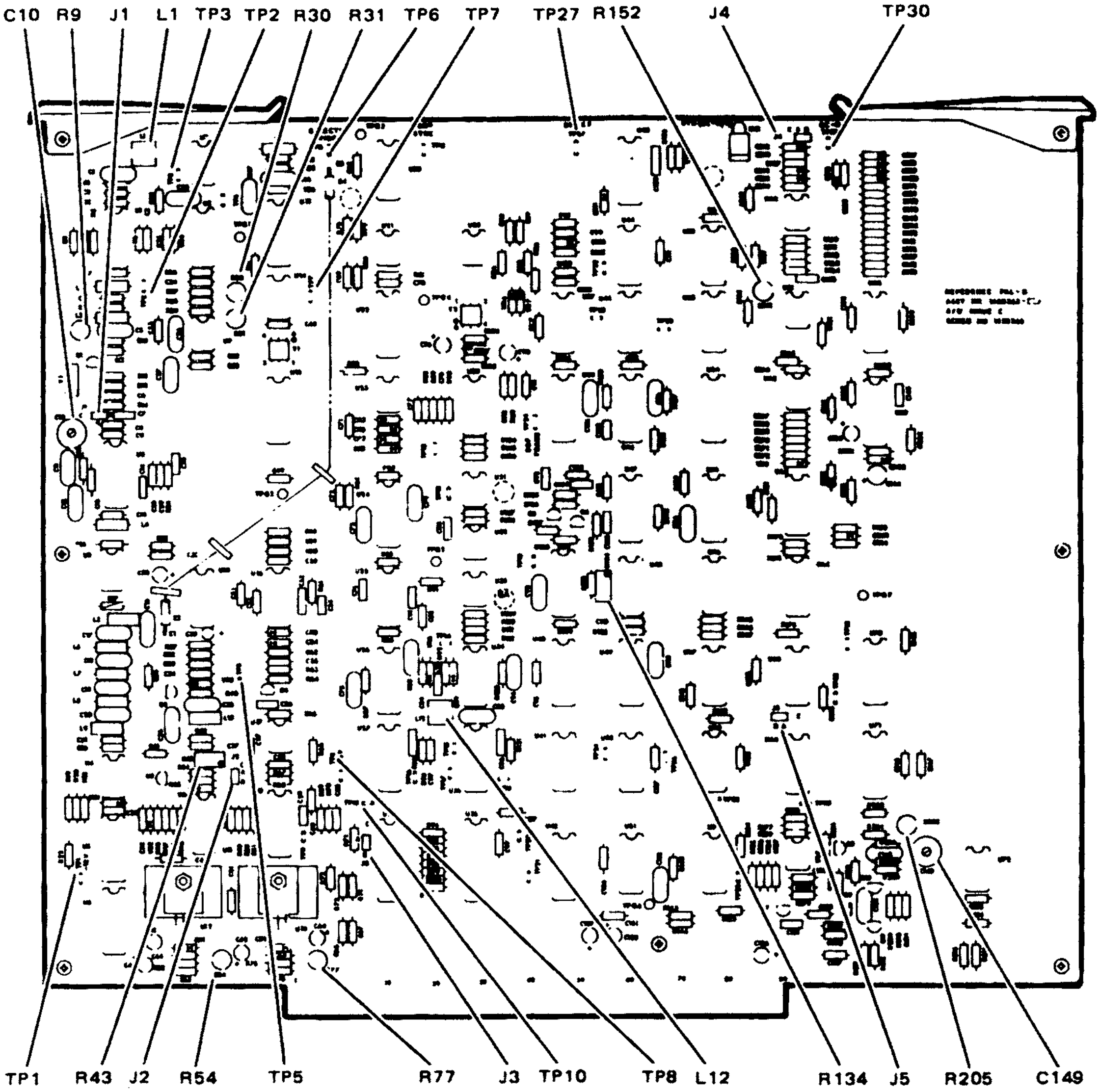


Figure 3-68. Reference PWA, PAL-M Jumpers, Test Points, and Adjustment Controls

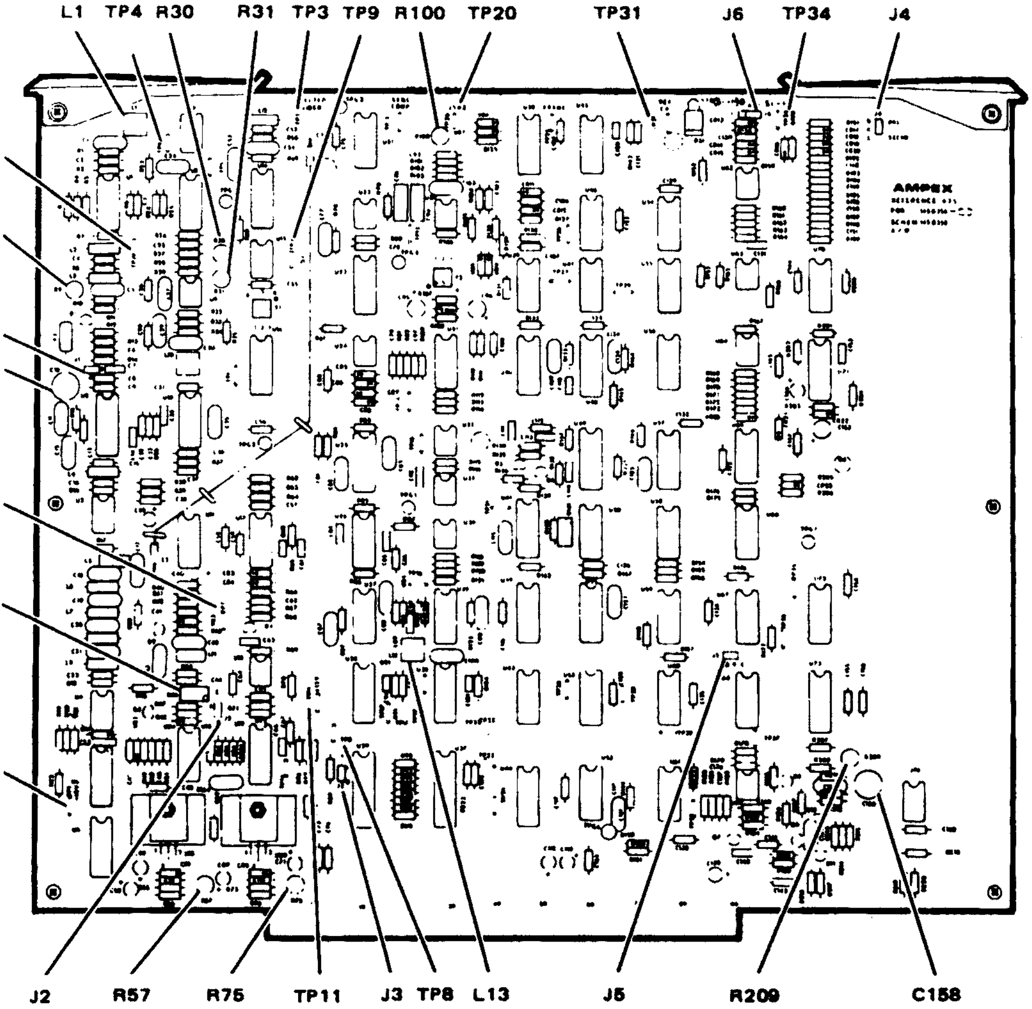


Figure 3-69. Reference PWA, PAL/SECAM Jumpers, Test Points, and Adjustment Controls

PART II
SECTION 4
AUDIO SYSTEM

4-1 GENERAL

This section provides theory of operation information for the audio system. Instructions are given for removal and reinstallation of the Audio PWA and audio and control track longitudinal head stacks. Jumper placement is explained and adjustment controls are tabulated. All procedures necessary for audio system performance verification and alignment are spelled out in detail.

The following drawings, which are included in the *VPR-80 Parts Lists and Schematics* manual, are referenced in this section.

Drawing	**Drawing No.**
Audio PWA	1450422
Audio PWA Schematic	1450424
System Interconnect Wiring Diagram	1465497

In addition, the following tables are included at the end of this section.

Table 4-9. Audio PWA Jumpers and Test Points
Table 4-10. Audio PWA Adjustments

4-2 THEORY OF OPERATION

Audio system and control track electronics are located on the Audio PWA. This PWA provides the following:

- Three channels of record/play electronics in conformance with either SMPTE or EBU standard.
- Erase current for audio, video, and control track longitudinal erase heads.
- Amplification for a microphone (low-level) input source. Amplified input can be connected separately or in combination to any of the three audio channels by jumper placement.
- Monitoring of the three audio channels separately or in any combination.
- Recording and playback of the control track signal.

Microphone input and three audio line input and output connections are made at the input/output connector panel located at the rear of the cabinet. These signals are connected to the Audio PWA via two-wire shielded cables. All audio inputs and outputs are balanced line. Record and play level controls, located on the primary control panel, provide dc levels to control amplifier gains on the Audio PWA. Mode and timing information is supplied to the Audio PWA via the bidirectional VPR-80 system bus.

Theory of operation of major functions of the Audio PWA is given in paragraphs that follow. Since operation of all three channels is similar, only channel 1 is described in detail. Referenced circuits are shown in the audio system block diagram, Figure 4-1 (sheets 1 and 2). Also refer to the Audio PWA Schematic Diagram No. 1450388.

4-3 Control Interface Logic

The Audio PWA receives instructions from the control system microprocessor via the 8-bit system data bus. Data lines are connected in parallel to octal data latches U65, U72, and U90. The 6-bit system address bus word is decoded by U56 which enables one of the three data latches to receive the instruction word and assert the various commands used on the Audio PWA. Commands to the various components on the Audio PWA (data latch outputs) are shown on sheet 1 of Figure 4-1, and are discussed in audio circuit descriptions. When the system is initially powered, a high system reset command enters the PWA at J11-25, and after inversion by Q46 clears the three data latches so that all latch outputs are in the reset (low) state.

4-4 Record Mode

The +8 dB (nominal) audio line input signal to be recorded is routed from connector J1 on the audio I/O connector panel to J2 pins 20 and 7 of the Audio PWA. This signal is applied to high-input impedance 0.5 gain differential amplifier U38-1 which converts the balanced line input signal to single-ended. The amplified signal is fed through jumper J4 in the line (A-B) position to selectable gain amplifier U38-7.

When a low-impedance (200Ω) microphone input is used, the microphone signal is fed through matching transformer T1 to amplifier U7-6. The amplified signal can then be assigned to any of the three audio channels in any combination by means of jumpers J4 (channel 1), J5 (channel 2), or J6 (channel 3). Also, if channel 1 is selected for a microphone input, amplifier U38-7 gain is increased from unity to +16 dB by placing jumper J7 in the B-C position.

The amplified signal from U38-7 is fed to dc-controlled transconductance amplifier U80-8. The gain of U80-8 is controlled by setting the audio 1 record level potentiometer R1 located on the primary control panel. This control provides a dc level that is routed through voltage follower U79-1 to amplifier U80-8. Record unity gain calibration potentiometer R146 is used to set record unity gain when front panel potentiometer R1 is set to the center (detent) position.

The gain-controlled signal from amplifier U80-8 is routed to record drive analog switch U83-10 and to EE monitoring analog switch U83-2. These switches are controlled by the system bus. In record mode both analog switches are closed.

The signal from switch U83-10 is fed to a record driver/equalizer circuit consisting of amplifier U74-7 and associated components. Potentiometer R481 is used to set record equalization to boost high frequencies when operating in the SMPTE or EBU standard.

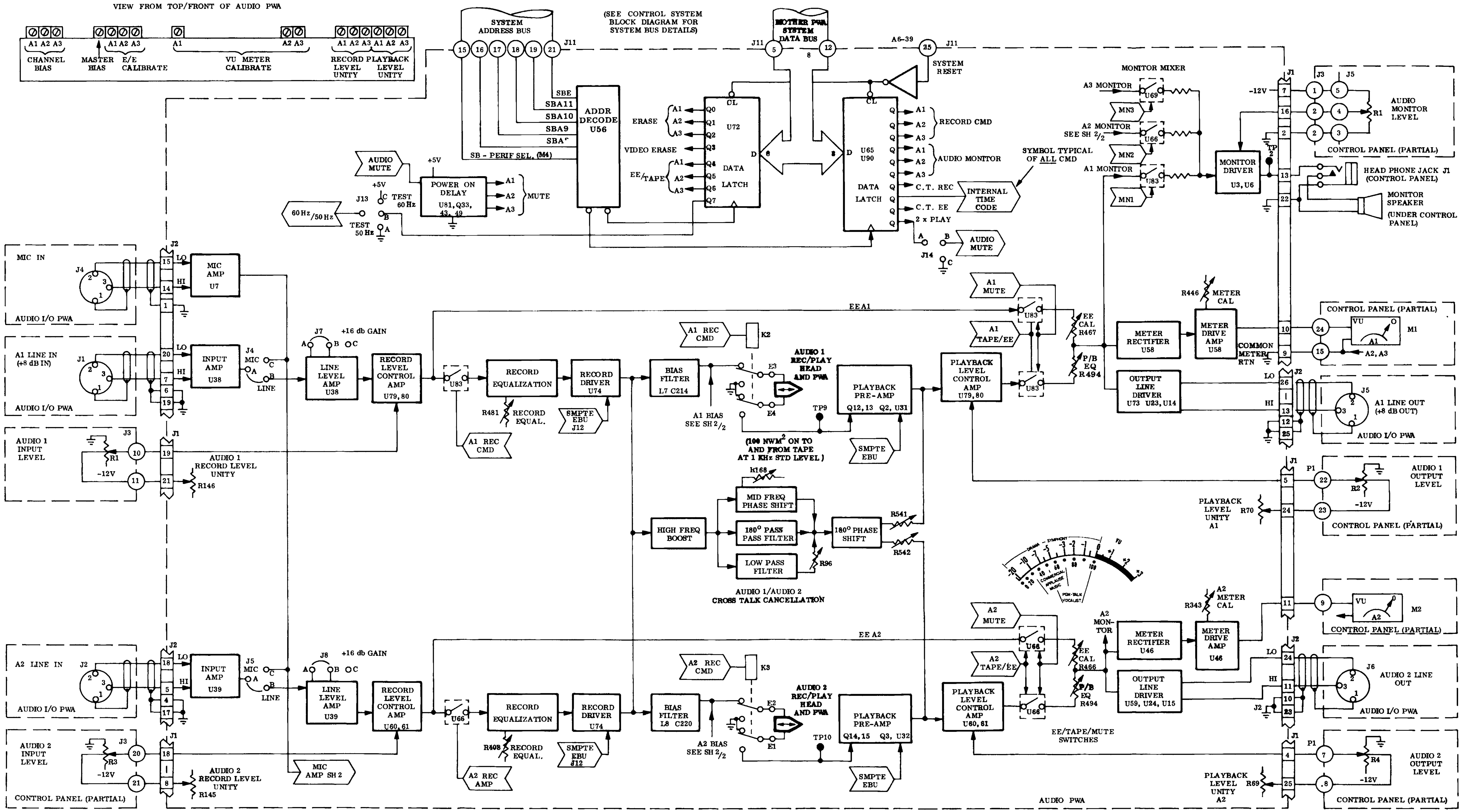


Figure 4-1.
Audio System Simplified Block Diagram
(Sheet 1 of 2)

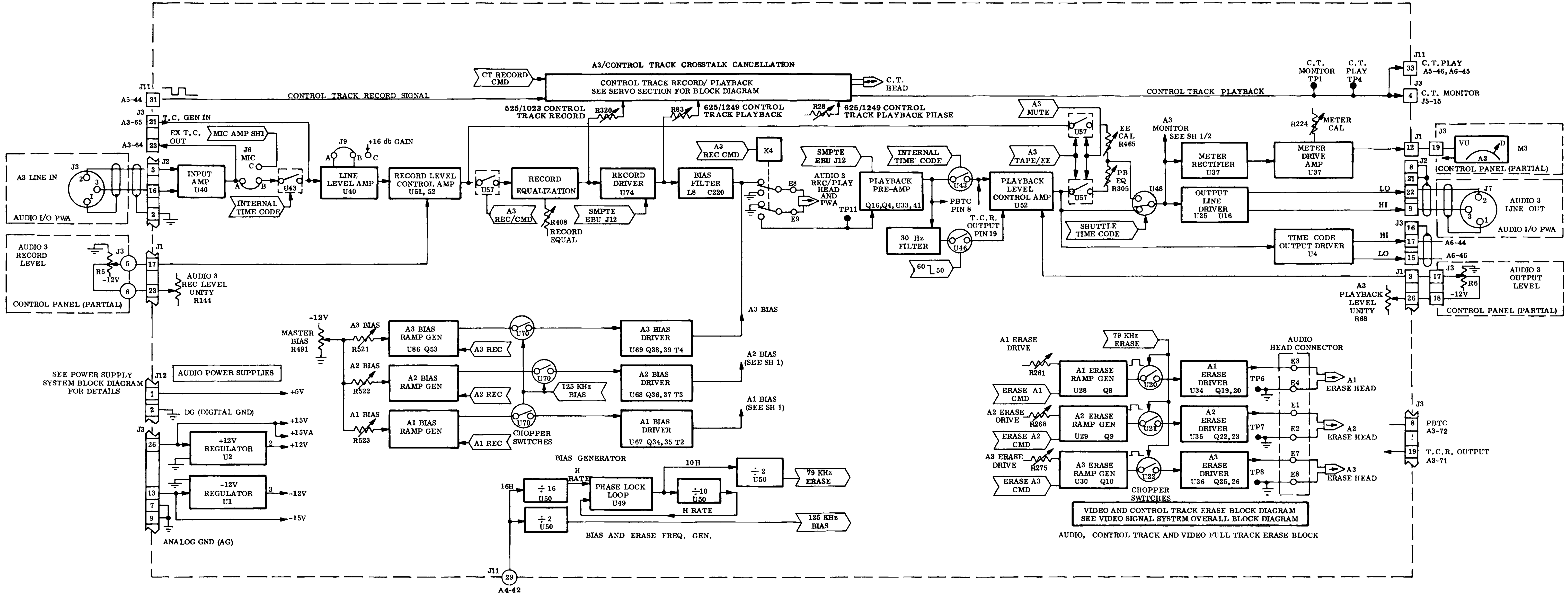


Figure 4-1.
Audio System Simplified Block Diagram
(Sheet 2 of 2)

Additionally, for SMPTE standard only frequencies below 50 Hz are boosted at the rate of 6 dB per octave. When operating in SMPTE standard, FET switch Q50 is open and capacitor C251 (located in the feedback path of amplifier U-74) is active. FET switch Q50 is controlled by placement of standards selector jumper J10.

The equalized signal from U74-7 is dc-coupled through C239 and applied through bias trap L7/C215, and constant current resistor R365 to the record/play head assembly. Record/play relay K2 is energized in record mode to remove a ground node and permit a 125-kHz bias signal to be mixed with the program signal at terminal E4 of the head connector. Current through the head is routed through a second set of contacts on relay K2 and goes to ground through bias-sensing resistor R368.

Relay K2 is controlled by D latch U87-5. When entering record mode, the relay is closed before the bias ramp starts up, and when coming out of record the relay is opened after the bias ramp has decayed.

For monitoring purposes, the signal from voltage-controlled amplifier U80-8 is fed through analog switch U83-2, EE calibration potentiometer R467, and summing amplifier U73-6 to three places: to A1 VU meter drive circuitry, to the monitor/mixer circuitry to feed the monitor speaker, and to the A1 line-out balanced bridge amplifiers U23-6/U14-6. These amplifiers operate out of phase, thus performing like a 2:1 step-up transformer, enabling the output signal to reach +24 dBm output peaks.

4-5 Play Mode

To play back a prerecorded tape, relay K2 is deenergized and voltage induced across the head is connected between ground and bases of dual transistor Q12, which is the input stage of integrating playback preamplifier Q12/U31-7. This amplifier gain decreases with increasing frequencies, thus compensating for the play head opposite characteristic of 6 dB per octave rise and resulting in a flat play mode response.

When in record mode, Q12 is biased with a high input current by FET switch Q13, which is on, connecting 100Ω resistor R297 from base to ground. To prevent a pop or click when switching from record to play mode, FET Q13 opens slowly as C148 discharges and causes Q12 transistor bias to gradually change to a lower bias current.

The gain of the preamplifier is determined by the value of feedback components C107/R174, which sets the lower integrating frequency cutoff at 12.5 Hz.

The signal is ac-coupled from amplifier U31-7 to inverting amplifier U31-1 through capacitor C88 in SMPTE standard, or through C88 and C87 connected in parallel in EBU standard. The single capacitor used for SMPTE standard provides a 6-dB-per-octave rolloff starting at 50 Hz (3180 µs) to compensate for the 6-dB-per-octave boost provided in record mode. The net effect is to reduce hum and provide a flat response. (No record or playback boost is used for EBU standard.) The switching in or out of capacitor C88 is controlled by placement of SMPTE/EBU jumper J10, which controls FET switch Q2.

The amplified signal from U31-1 is ac-coupled to dc-controlled transconductance amplifier U80-9 in a circuit identical to that described for record mode. The gain of U80-9 is controlled by the setting of audio 1 play level potentiometer R2 located on the primary control panel. This potentiometer provides a dc level that is routed through voltage follower U79-7 to amplifier U80-9. Playback unity gain calibrate potentiometer R70 is used to set playback gain to unity when front panel potentiometer R2 is set to center (detent) position. The gain-controlled signal from amplifier U80-9 is routed through normally closed contacts of switch U83-15 to amplifier U73-6. From here the signal path is the same as that previously described for record mode.

Potentiometer R494, in conjunction with components L13/L2/C235/C237/R495, forms a playback equalizer to provide a 15-µs time constant (rise in response starting at 10.6 kHz) to compensate for playback head gap loss.

Audio channel 3 is similar to the operation of channel 1 but with two major differences. Because of the close proximity of the control track head winding to the audio channel 3 head winding and the high level (1000 nWb/m) SMPTE control track signal level, tape fringing occurs into the audio 3 channel. Therefore, a 30-Hz peaking filter is used in SMPTE mode that adds the 30-Hz signal on channel 3 back into the audio channel 3 playback signal 180° out of phase.

The playback audio channel 3 signal at the output of channel 3 preamplifier U33-1 is tapped and applied to 30-Hz peaking filter R165/R90/C81/C82/R164/U41-1. The filter amplifies and inverts the 30-Hz component and feeds the signal through switch U43-6 to a summing point at the junction of R231/R292. Switch U43-6 is closed by the high 60/50 command from latch U72-19.

When playing back time code on channel 3 in shuttle mode, playback equalizer R305/C167/C11/C169/R30 is bypassed by action of switches U48-14 and U48-2. These switches are controlled by shuttle time-code command, which in shuttle causes switch U48-14 to open and U48-2 to close. The playback signal path goes from front-panel-controlled transconductance amplifier U52-9, through switch U57-5, amplifier U53-1, switch U48-2 to the channel 3 balanced bridge line out amplifiers U25-6/U16-8. The unequalized playback signal at the output of amplifier U53-1 is also supplied to amplifiers U4-7/U4-1 and routed to time-code output connector J3 pins 17/15. This output is then routed to the control PWA.

4-6 Audio Channel 1 and 2 Crosstalk Cancellation

Because of transformer action within the audio head assembly, bidirectional crosstalk between audio channel 1 and 2 occurs. To remedy the problem when one channel is recording while the other is playing back, audio from the channel in record is inserted 180° out of phase into the channel playing back. The record audio signal is applied to crosstalk cancellation circuitry where three bandpass filters separate the signal into its high, midrange, and low-frequency components, thus enabling high- and low-frequency components to be individually controlled so that head characteristics can be matched to the circuitry. The three frequency components are then summed, amplitude-adjusted, and applied to the playback amplifier path. Cancellation circuitry is active except when both channels are simultaneously in play mode.

The record audio signal from channel 1 amplifier U74-7 (TP14) or from channel 2 amplifier U74-1 (TP 13) is applied to the junction of C171 and pin 5 of amplifier U42-7. High-frequency components are bandpass-filtered by U26-7 and associated components, and applied through summing resistor R94 to the input pin 2 of summing amplifier U26-1. Potentiometer R168 is used to adjust high-frequency gain.

Midrange frequency components are bandpass-filtered by C105/R170/C106/R171 and fed through summing resistor R97 to the summing point pin 2 of amplifier U26-1. Low-frequency components are bandpass-filtered by U42-1 and associated components and applied through summing resistor R96 to summing point pin 2 of amplifier U26-1. Potentiometer R166 is used to adjust low-frequency gain. Summed signals are then routed through crosstalk level controls R542 (channel 2) and R541 (channel 1) to the playback channel path.

In SMPTE record mode frequencies below 50 Hz are pre-emphasized at the rate of 6.0 dB per octave. Therefore, switch U43-11 is open in SMPTE mode to add capacitor C123 into the low-frequency signal path to de-emphasize the boosted signal.

When both channels are simultaneously in playback, record input signals to crosstalk cancellation circuitry are shorted to ground by switches U43-14 and U48-11 being closed. This improves playback signal-to-noise by removing cancellation circuitry from the signal path.

4-7 Audio/Mixer

The three audio channels can be applied separately or in any combination to the internal monitor speaker (or a headset) for monitoring purposes. Signals routed to monitor circuitry correspond to the recorder mode of operation (record, play, or EE).

The audio signal at the output of amplifiers U73-6 (channel 1), U59-6 (channel 2) and either U47-6 or U53-1 (channel 3) are fed to mixer selector switches U53-7 (channel 1), U66-7 (channel 2), and U57-7 (channel 3), respectively. The channel or channels to be monitored are selected by pressing the appropriate pushbutton switch on the secondary control panel. When a pushbutton switch is pressed, a monitor command (MN1, MN2, MN3) from octal latch U65 goes high and causes the appropriate mixer selector switch to close. Selected audio signals are combined in summing amplifier R556/U6-13 and applied to voltage-controlled amplifier U3-8. The gain of amplifier U3-8 is controlled by the setting of the speaker/phones volume control potentiometer R1 located on the secondary control panel. This potentiometer provides a dc level that is routed through buffer U3-9 to amplifier U3-8. The signal is further amplified by U6-2 and routed to the headphone jack and monitor speaker.

4-8 Audio Bias and Erase

Audio bias and erase circuitry provides ramped-on and ramped-off 125-kHz bias and 79-kHz erase signals. Ramped on and off portions of the signal are provided to help prevent recording of pulses (pops and clicks), magnetizing of heads, and to provide smooth edit transitions.

A 16H reference frequency, generated on the AST Servo PWA, is counted down to provide the bias (125-kHz) and erase (79-kHz) frequencies (nominal).

4-9 Audio Bias Drive

Audio bias is mixed with the program signal at the head assembly. Master bias control R491 is used to select a dc-voltage value between +3.0 Vdc and +10 Vdc. This selected value is buffered by U78-6 and applied to each of the three channels' bias-drive potentiometers. For channel 1, the voltage value selected by bias-drive potentiometer R523 is fed through voltage-follower U84-7, and applied to dc ramp generator Q51/U84-1. This ramp generator is turned on when the A1 $\overline{\text{REC}}$ logic level signal from on-board control interface latch U65 goes high. The ramp generator provides a ramp whose peak amplitude is from ground to between +3.0 Vdc and +10 Vdc, as determined by the setting of bias drive potentiometer R523. This ramp is always of a fixed time duration.

Ramped dc level is applied to switch U70-2, which is turned on and off by a 125-kHz signal provided by count-down circuit U50-11/Q45. This switch action produces a 125-kHz chopped square wave that is switched between ground and the positive dc voltage level at the output of U84-1. The resulting square wave is filtered and applied to bias drive power amplifier U67-1/Q34/Q35/T2. The bias drive amplifier operates in a class AB configuration to minimize crossover distortion. Amplified output from complementry drivers Q34/Q35 is applied to series-resonant tank circuit consisting of C192 and primary of T2, which further filters the square wave to a sine wave. The 125-kHz sine wave signal at the secondary of T2 is ac-coupled through C191 to the record/play head where it is mixed with the record signal.

4-10 Audio Erase Drive

Audio erase drive circuitry provides a ramped-on and ramped-off 79-kHz signal to the audio erase head assembly. To enable a smooth transition from old audio material to new audio material, the erase current and record signal are overlapped at the 6.0-dB erasure point during ramp time. Because erase current erasure is at the 6.0-db point halfway through the allotted 16-ms start-up time, it is necessary to cause the erase current ramp to reach maximum in three steps, each step at a faster rise time.

Initially the ramp generator is turned on when the A1 erase logic level from octal latch U72-2 goes high. The ramp generator provides a ramp whose peak amplitude is established by the dc voltage selected by erase drive potentiometer R261. This value is buffered by voltage follower U34-1 and applied through resistor R200 to integrator R201/C67/U28-7. Output of the integrator is connected to comparators U28-1 and U28-10. As integrator output voltage builds up, comparator U28-1 first changes state and closes switch U20-11, causing the integrator time constant to be shortened. This is followed by comparator U28-10 changing state and closing switch U20-8, thus further reducing the integrator time constant by adding resistor R130 in parallel with R129. Ramp output of integrator U28-7 is fed through voltage-follower U28-16 to input of switch U20-1, which is turned on and off by the 79-kHz signal provided by the 16H countdown circuitry. This switch action produces a 79-kHz chopped square wave. The square wave is filtered and applied to erase-drive power amplifier U34/Q19/Q20. Transistors Q19/Q20 are complementary pair drivers, and R264 provides feedback to pin 6 of amplifier U34-7. Output of the drivers is applied to FET switch Q21, which is turned on by the A1 erase command filtered by R329-R331 and associated capacitors. This action provides a ramped turn-on of FET Q21 to prevent pops and clicks from being introduced into adjacent channels. The audio erase signal is ac-coupled to the head assembly in a series-resonant circuit consisting of C176 and the head assembly winding to provide maximum current through the head assembly.

4-11 Bias and Erase Frequency Generator

A 16H reference frequency, generated on the AST Servo PWA, enters the Audio PWA at J11 pin 29 and is applied to the bias and erase frequency generator. This circuitry counts down the 16H frequency to provide 125-kHz (8H) audio bias frequency and 79-kHz (5H) erase frequency.

The 16H frequency is divided by two by counter U50-11 to provide 8H (125 kHz). This signal is filtered and dc-restored by R516/C258/Q48 and routed to the bias drive circuitry previously described.

The reference 16H is also divided by 16 by counter U50-14 to provide a 1H sync signal to phase-lock loop (PLL) U49-4. The PLL provides a 10H signal to counter U50-3 which divides the 10H signal by two to provide 79 kHz (5H). This signal is filtered and dc-restored by C180/R340/Q31 and routed to the erase drive circuitry previously described. The PLL operating frequency is determined by components C175/R384.

4-12 Video and Control Track Erase Drive

Video and control track erase drive circuitry provides a ramped-on and ramped-off 79-kHz signal to the video erase head and to the control track erase head.

When the video erase command from octal latch U72-9 goes high, FET switch Q41 turns on and activates integrator U54-10. Integrator U54-10 provides a 16.0-ms dc ramp whose fixed peak amplitude is from ground to +5.0 Vdc. Ramped dc level is applied to the input of switch U13-11, which is turned on and off by the 79-kHz signal provided by the 16H countdown circuitry previously described. Switch action produces a 79-kHz chopped square wave. The signal is converted to a sine wave by filter network C16/C42/R58/R60 and amplified by U19-1. The amplified signal is routed to video and control track erase level set potentiometers.

The video erase level selected by potentiometer R190 is amplified by feedback driver amplifier U45-6/Q17/Q18. The erase signal is ac-coupled to the head assembly in a series-resonant circuit consisting of C136 and the video erase head winding to provide maximum current through the head assembly.

The control track erase level selected by potentiometer R193 is amplified by feedback driver amplifier U27-6/Q5/Q6. The amplified signal is applied to FET switch Q7, which is slowly turned on by the video erase command filtered by R439/C134. This action prevents any pops and clicks from being recorded. The erase signal is ac-coupled to the head assembly in a series-resonant circuit consisting of C163 and the control track erase head winding to provide maximum current through the head assembly.

4-13 Audio/Control Track Crosstalk Cancellation

Because of the close proximity of the audio channel 3 head winding to the control track head winding, and the low-level (100 nWb/m) EBU control track signal level recorded on tape, it is necessary in insert edit mode (channel 3 audio in record mode) to activate crosstalk cancellation circuitry.

Channel 3 audio is added 180° out of phase to the playback control track signal to provide crosstalk cancellation. Audio from channel 3 record amplifier U53-7 is coupled through C194 to inverting amplifier U10-1. The signal is then fed through cancellation gain control potentiometer R46 to phase-shift filter amplifier U10-7. Filter network potentiometer R113 affects low-frequency component cancellation, and potentiometer R44 affects high-frequency component cancellation.

The phase-shifted and gain-controlled audio channel 3 record signal is summed with the control track play signal at the junction of R42/R40 and applied to pin 2 of switch U9-2. When the CT $\overline{\text{EE}}$ command is high, combined signals are routed to summing amplifier U17-1.

Gain of amplifier U17-1 is increased when operating in the EBU standard. Gain is increased when a low is supplied by octal latch U72 (through jumper J13 in the normal position) to switch U8-3 located in the feedback path of amplifier U17-1. This low causes switch U8-3 to open and thus remove parallel connected potentiometer R98 from the amplifier feedback path. For test purposes, jumper J13 can be placed in the EBU position to provide a constant low.

The signal from U17-1 is then routed to two places: one path is through amplifier U5-7 to monitor out connector J3 pin 6 for routing to rear panel MONITOR connector J5; the other path is through amplifiers U18-1/U12-7 to the control track play connector J11 pin 33 for routing to the Servo PWA and Control PWA.

4-14 Control Track Play Mode

In play mode, relay K1 is deenergized and voltage induced across the head is connected between ground and the base of transistor Q1, which is the input stage of integrating playback preamplifier Q1/U17-7. This preamplifier provides equalization such that amplifier gain decreases with increasing frequencies, thus compensating for the play head opposite characteristic of 6 dB per octave rise, and resulting in a flat play mode response.

In all modes except shuttle and cue, switch U9-11 in the input stage of Q1 and switch U8-11 in the output stage of U17-9 are closed to insert shunt filter components to help eliminate 125-kHz audio channel 3 bias crosstalk frequencies that enter the control track play channel in insert edit mode. In shuttle and cue modes, a high from latch U65-9 opens the switches to increase bandwidth and high-frequency response.

Switch U8-14 opens in shuttle and cue modes to decrease capacitive coupling to help eliminate low-frequency noise.

4-15 Control Track Record Mode

Type C format standard defines the format used for control track recording.

The SMPTE control track is recorded using 79-kHz bias, and consists of saturated square waves that alternate in polarity at a field rate with an extra pair of transitions added on alternate frames to identify the color frame. The alternate frame identification pulse also identifies field I. See Figure 4-2.

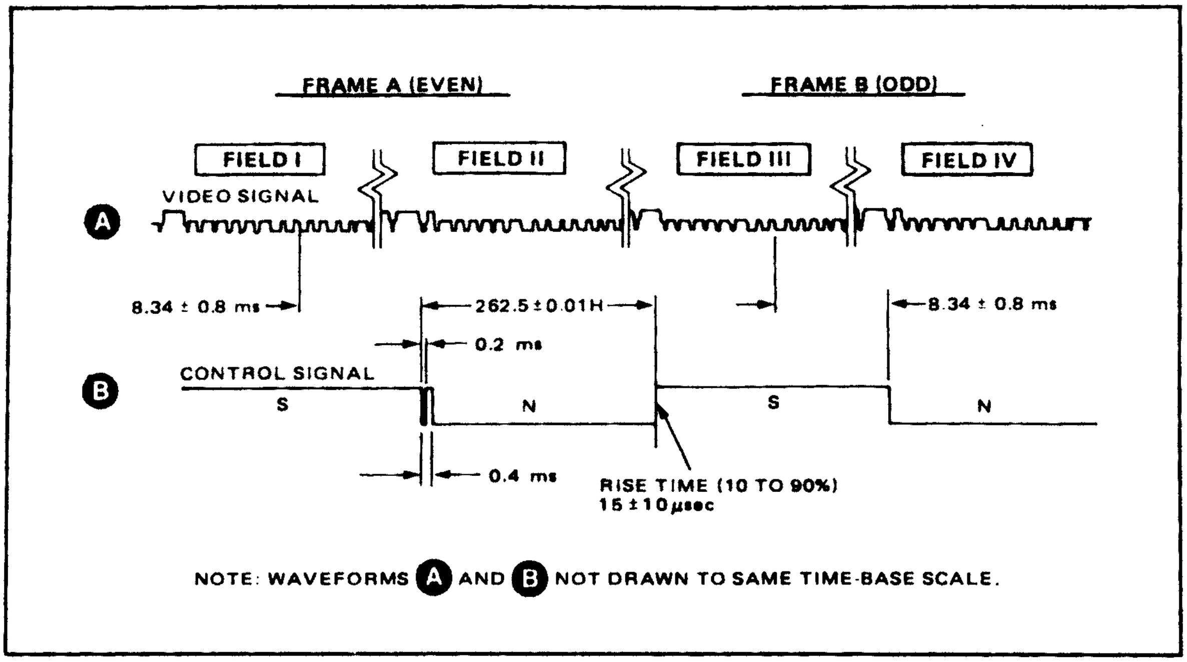


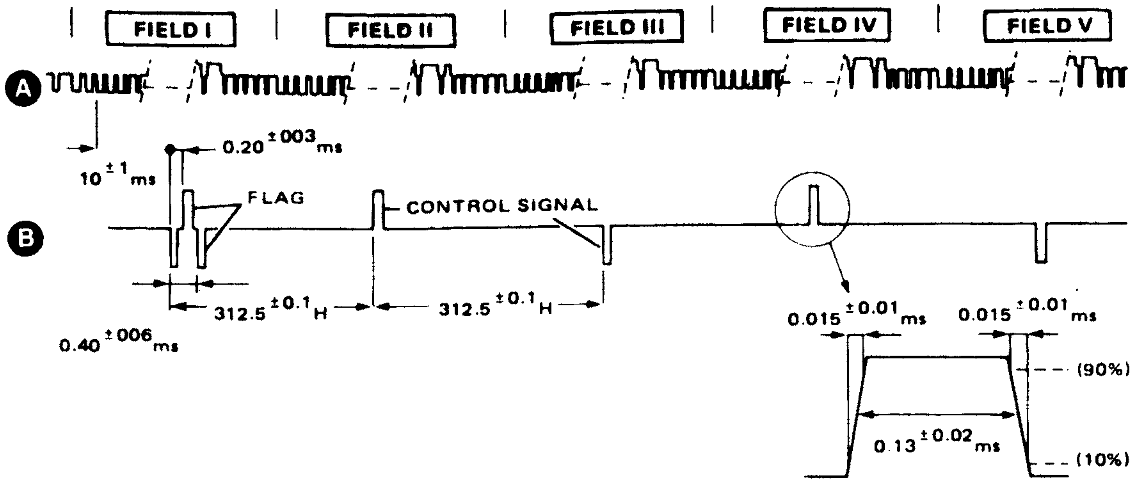
Figure 4-2. SMPTE Control Track Format

The EBU control track is recorded using 79-kHz bias, and consists of a series of alternating polarity pulses with an extra pulse added to identify the PAL eight-field and color frame sequence. See Figure 4-3.

The control track signal, either 30-Hz (SMPTE) or 25-Hz (EBU) from the Servo PWA, enters the Audio PWA at J11, pin 31 as a NRZ (non-return-to-zero) signal. The signal is buffered by U64-3 and is fed through AND gate U55-11 which is enabled in record mode by the high control-track record command signal from latch U65-12.

4-16 SMPTE Mode Operation

In SMPTE mode, the 60/50 command from latch U72-19 is high and causes one-shot U71 to be disabled by the high applied to its external (pin 9) reset input and switch U63-10 to be closed. A ramped dc voltage from ramp generator voltage follower U54-7 (described later) is applied through closed switch U63-10 and voltage follower U62-1 to the input of switches U63-9 and U63-3, which are driven by an alternate phase signal. The NRZ signal from AND gate U55-11 is inverted by exclusive OR gate U64-4 and fed through enabled AND gate U55-3 to the switch



NOTES: 1. THE FIGURE SHOWS THE TRACKING CONTROL WAVEFORM AND TIMING. AN EDIT PULSE IS INCLUDED WHICH IDENTIFIES THE PAL EIGHT-FIELD SEQUENCE. THE PAL/SECAM FOUR-FIELD SEQUENCE CAN BE DERIVED FROM THIS INFORMATION.

2. WAVEFORMS Ⓐ AND Ⓑ NOT DRAWN TO SAME TIME-BASE SCALE.

Figure 4-3. EBU Control Track Format

gate input of switch U63-9. The NRZ signal is also fed from gate U55-11 through enabled gate U55-10 to the switch gate of switch U63-3. Switches U63-9 and U63-3 operate out of phase to provide a push/pull signal to amplifier U62-7. The control track signal is then routed through switch U9 pins 15/3,14 (in EE mode) to two paths. One path is to amplifier U17-1 previously described. The other path is through high-pass filter C40/R53 to a summing point where the signal is combined with a ramped 79-kHz bias signal.

The combined signal is amplified by push/pull drivers U11-6/U18-7 and applied to the contacts of control track record/play relay K1. Amplifier U11-6 is a constant current amplifier as established by feedback resistor R118 feeding back through R50 to the noninverting input of U11-6. This provides for constant current through the head.

Relay K1 is energized after video and control track erase circuitry has been activated but before the bias and signal ramps have risen. Initially, the video erase command from latch U72-9 goes high. This high is applied to the D input of latch U88-9. Latch U88-9 is clocked high by the frame reference pulse entering the PWA at pin 27. The high from U88-9 turns on Q47 which activates record relay Q47. The control track command from latch U65-12 then goes high and after inversion by gate U76-8 holds latch U88-9 high for the balance of record mode.

When record mode is terminated, the video erase command from latch U72-9 goes low followed by the control track record command from latch U65-12 going low. This enables latch U88-9 to be clocked low by the next frame pulse. Thus, record relay is deenergized after signal and bias ramps have decayed.

4-17 EBU Mode Operation

The EBU control track generator circuitry operates similar to SMPTE control track generator circuitry, with the major exception that EBU control track pulses and flag pulses are formed by 130-μs one-shot U71.

One-shot U71 is enabled by the low 60/50 command applied to its external reset (pin 9) input. The control track signal from gate U55-11 is applied to pulse former R444/C230/U64-11 which provides trigger pulses for one-shot U71 that correspond to each edge of the control track signal. The 130-μs pulses from U71-1 are fed through U64-10 (no inversion) to AND gates U55-3 and U55-10. The control track signal from gate U55-11 is inverted by U64-4 and applied to pin 2 of AND gate U55-3. The signal from U55-11 is also applied (no inversion) to pin 9 of AND gate U55-10. These AND gates are enabled by the 130 μs pulse from one-shot U71-10 to provide opposite polarity signals to close switches U63-9 and U63-3.

Ramped dc voltage from ramp generator voltage follower U54-7 is applied through control track amplitude adjust potentiometer R441 to input of switches U63-9 and U63-3, which are driven by the opposite phase control track signal. Switches U63-9 and U63-3 operate to provide EBU control track pulses. When switches are open, as occurs between pulses, push/pull amplifier U62-7 is referenced to ground to provide dc restoration. The control track signal is then routed as described for SMPTE mode.

4-18 Control Track Ramp Generator

The control track ramp generator Q40/U54 and associated components provide a dc ramp for bias and control track signal circuitry. The generator is turned on when the control track record command, from latch U65-12, goes high. Approximately +2.5 Vdc from divider R378/R811 is applied to integrator U54-1 which provides a 16.0-ms dc ramp. Ramped voltage is applied through voltage follower U54-7 to switch U13-9, which is turned on and off by the 79-kHz bias frequency signal (origin described earlier). This switch action produces a 79-kHz square wave whose amplitude is a function of the ramped voltage. The square wave is converted to a sine wave by filter network C66/C65/R122 and integrating amplifier U19-7. The signal is applied through filter C63/R54 to a summing point, where it is combined with the ramped control track record signal from U62-7. Ramped dc voltage is also supplied to the control track signal voltage follower U62-1 to provide a ramped on and off control track signal as previously described.

4-19 Mute and Power Up/Down

Audio channel 1, 2, and 3 outputs are automatically muted during power-on and power-off sequences. In addition, audio 1 and 2 outputs can be muted in shuttle and cue modes by placing jumper J14 in the A-B position. When shuttle or cue mode is selected, latch U65 provides a high through jumper A14 in the A-B position to Q54.

This high turns on Q54 which provides a low to comparator U81-7 which provides a high to the base of mute channel 1 transistor Q49 and mute channel 2 transistor Q43, turning them on. The resulting low on the mute channel 1 and mute channel 2 lines disables audio channel 1 switch U83 and audio channel 2 switch U66, respectively. When shuttle or cue mode is terminated, mute lines continue to stay low until capacitor C241 charges to +5.0 Vdc through R484.

When power is first applied, the +12-Vdc supply is active before the +5.0-Vdc supply and this enables all three channels to be temporarily muted. During this time divider R506/R551/R550/R552 connected between the +12-Vdc supply and ground provides positive bias to the base of mute transistors Q33/Q43/Q49, turning them on. After both supplies are active, diode CR37 conducts and provides a low to the base of channel 3 mute transistor Q33. This prevents channel 3 from being muted in shuttle and cue modes.

4-20 REMOVAL/INSTALLATION

The following paragraphs describe removal and reinstallation of audio and control track longitudinal head stacks and the Audio PWA.

4-21 Longitudinal Head Stacks

STEP 1 Remove plastic head cover and transport trim as outlined in Part I, paragraph 4-12.

STEP 2 Open hinged shield below longitudinal heads. See Figure 4-4.

STEP 3 Remove three screws and washers securing audio and control track head shield, and detach shield.

STEP 4 Disconnect head cables from audio/control track head stack and audio/control track erase head stack. See Figure 4-5.

STEP 5 Remove screw which secures each head stack to longitudinal head assembly plate, and detach head stacks.

Replace head stack as follows:

STEP 6 Clean head stack and head mounting surface with head cleaner. Secure head stack with screw. Ensure that head stack is aligned with locating pin on longitudinal head assembly plate and is flush to plate.

STEP 7 Reconnect cables at audio/control track and audio/control track erase head stacks.

STEP 8 Reinstall shield removed in step 3. Be sure that shield is aligned with and is flush against locating pins on longitudinal head assembly plate.

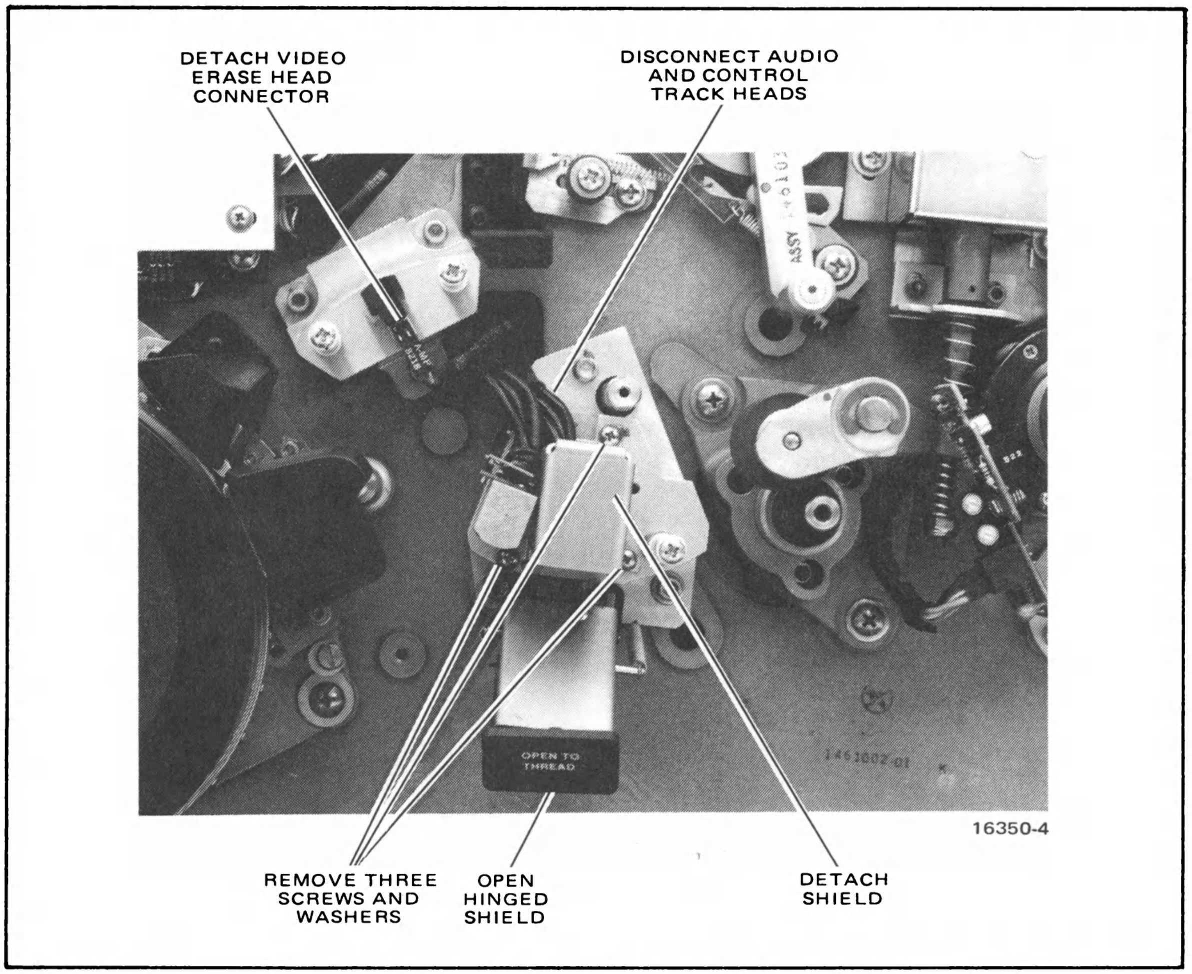

DETACH VIDEO ERASE HEAD CONNECTOR
DISCONNECT AUDIO AND CONTROL TRACK HEADS
OPEN TO THREAD
16350-4
REMOVE THREE SCREWS AND WASHERS
OPEN HINGED SHIELD
DETACH SHIELD

Figure 4-4. Disconnecting Longitudinal Heads

4-22 Audio PWA

To remove the Audio PWA from the VPR-80, and reinstall it, proceed as follows:

STEP 1 Remove plastic head cover and transport trim as outlined in Part I, paragraph 4-12.

STEP 2 Open hinged shield below longitudinal heads. See Figure 4-4.

STEP 3 Remove three screws and washers securing audio and control track head shield, and detach shield.

STEP 4 Disconnect head cables from audio/control track head stack and audio/control track erase head stack. Also detach connector at longitudinal video erase head.

STEP 5 Loosen two captive screws at rear of cabinet and lower rear door assembly as shown in Part I, Figure 4-3.

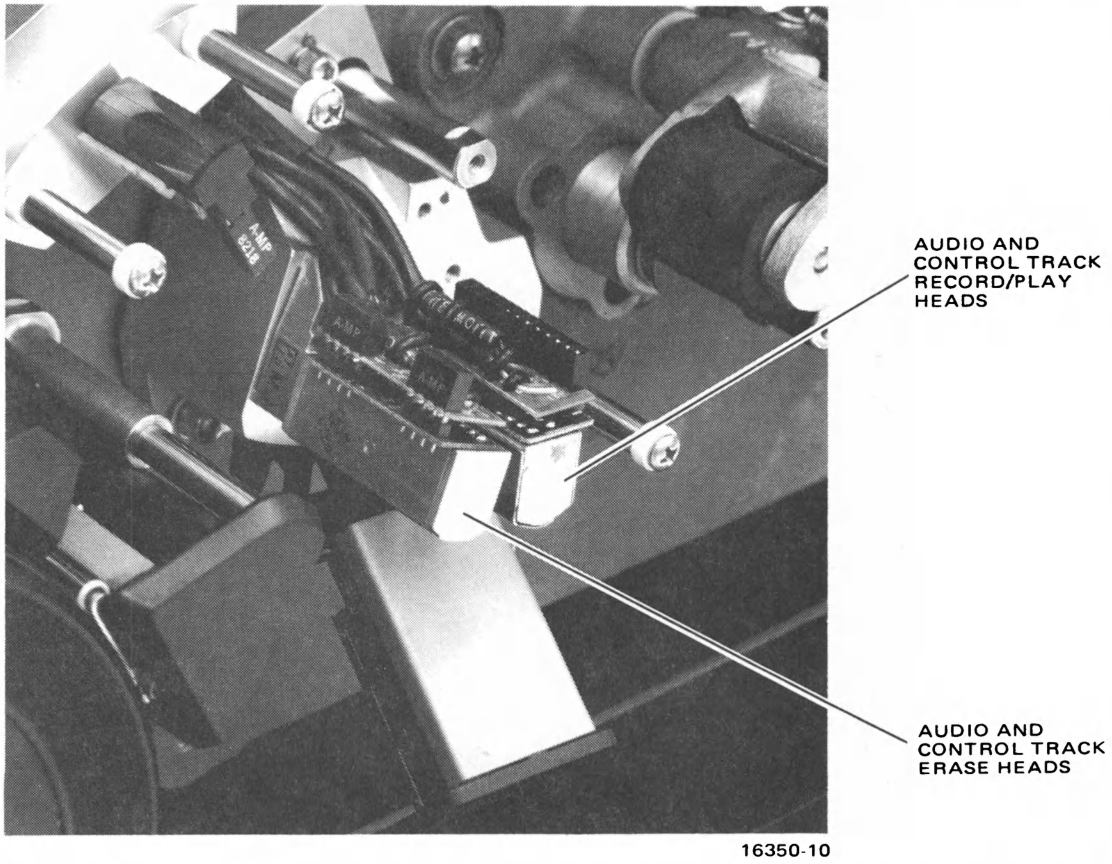

AUDIO AND CONTROL TRACK RECORD/PLAY HEADS
AUDIO AND CONTROL TRACK ERASE HEADS
16350-10

Figure 4-5. Replacing Audio/Control Track Head Stack

STEP 6 Detach four harness connectors J1, J2, J3, and J12 and ribbon cable connector J11 from the Audio PWA.

STEP 7 Disengage four captive screws securing Audio PWA mounting plate. Remove Audio PWA and its mounting plate and head cable harness from VPR-80. See Figure 4-6.

STEP 8 For access to Audio PWA components and adjustments on the PWA, disengage four captive screws securing Audio PWA shield, and detach shield.

Install Audio PWA in the VPR-80 as follows:

STEP 1 Pass Audio PWA harness connectors for the audio and control track record/play and erase heads and the video erase head through hole in transport casting above audio/control track head stacks.

STEP 2 Reinstall Audio PWA and reconnect cables disconnected in step 6 of removal procedure.

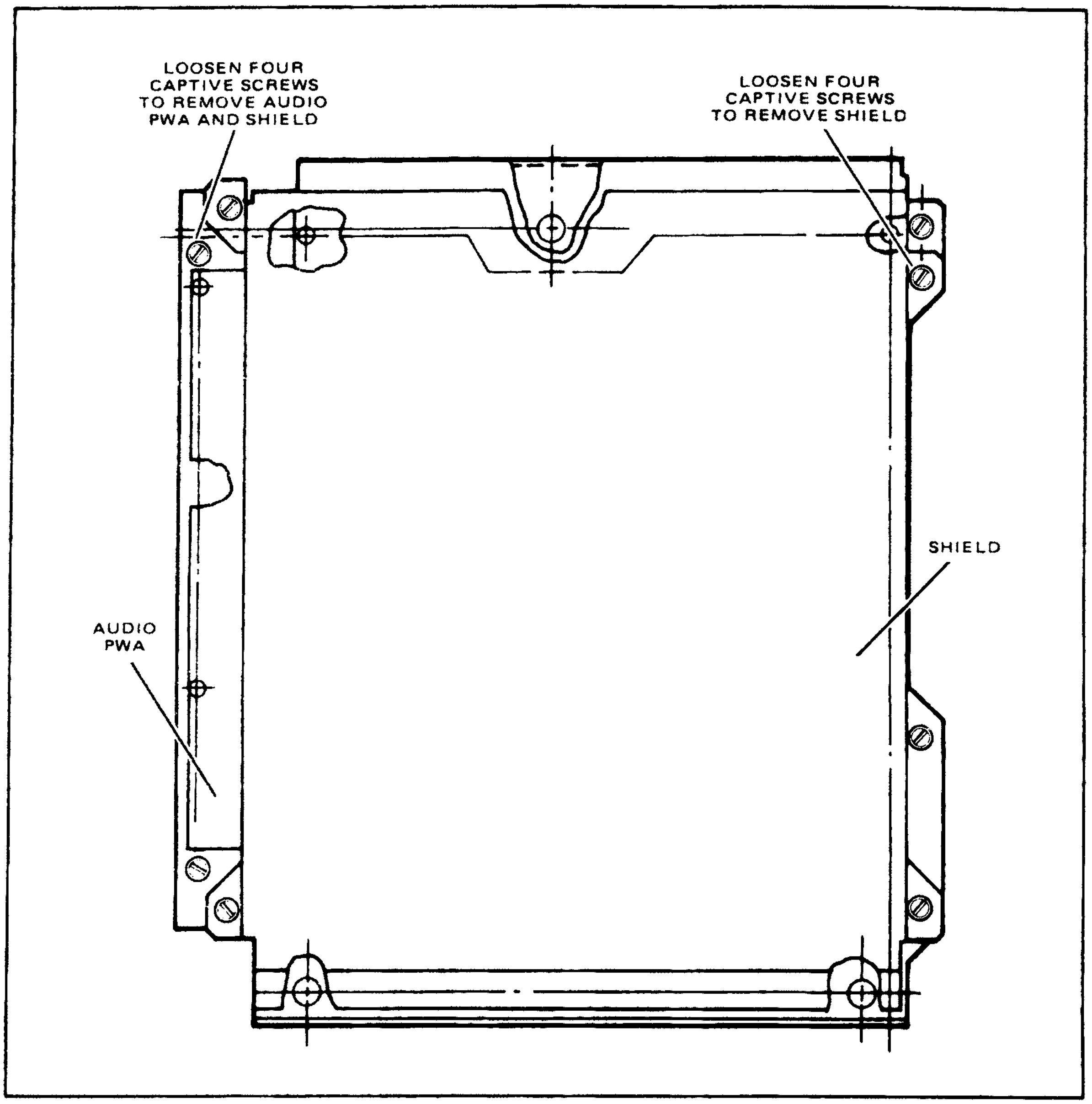

LOOSEN FOUR CAPTIVE SCREWS TO REMOVE AUDIO PWA AND SHIELD
LOOSEN FOUR CAPTIVE SCREWS TO REMOVE SHIELD
SHIELD
AUDIO PWA

Figure 4-6. Removing Audio PWA

STEP 3 Reinstall shield over Audio PWA, and close rear door assembly.

STEP 4 Reconnect Audio PWA harness connectors to head stacks from which they were disconnected in step 4 of removal procedure.

STEP 5 Reinstall audio head shield. Be sure that shield is aligned with and is flush against locating pins on longitudinal head assembly plate.

STEP 6 Reinstall transport trim and head cover removed in steps 1 and 3 of removal procedure.

4-23 AUDIO SYSTEM ALIGNMENT

The following paragraphs explain various configurations of the Audio PWA obtained by jumper changes; test frequencies on audio alignment tapes are tabulated. Checkout procedures for demonstrating compliance with VPR-80 audio system specifications are spelled out in detail. Adjustment procedures are then given for all variables so that proper audio system alignment can be made following repair or part replacement.

4-24 Audio PWA Configurations

Audio and control track configuration of the Audio PWA can be converted from SMPTE/PAL-M to EBU standards, or vice versa, by simply changing jumper placement. Conformance to differing studio record gain levels, conversion of an audio channel to microphone input, and audio muting/nonmuting during shuttle and cue modes are also accomplished by jumper changes. Audio PWA jumpers are shown in Table 4-9.

4-25 Microphone Input

The three audio line inputs are routed to line-level amplifiers through jumpers J4, J5, and J6 (A1, A2, and A3), which are placed in the A-B position at the factory. MICROPHONE input is left unconnected. If an audio channel will be used for microphone input, the corresponding jumper must be placed in the B-C position.

Jumper	Position	Function
J4 (A1) J5 (A2) J6 (A3)	A-B	Line input
	B-C	Microphone input

4-26 Record Gain

Record gain levels of the audio channels are each adjusted at the factory so that +8 dBm in equals 100 nWb/m (flux density on tape). Jumpers J7, J8, and J9 (A1, A2, A3) are placed in the A-B position. If the audio operating level of the studio is zero dBm or less, jumpers should be changed from position A-B to position B-C. The VPR-80 can then be set up for other input levels, typically -10 dB.

Jumper	Position	Function
J7 (A1) J8 (A2) J9 (A3)	A-B	Use with normal studio operating levels (i.e., +4 dB or +8 dB)
	B-C	Use with semiprofessional operating levels (i.e., -10 dB)

4-27 Format Standard

Placement of jumper J10 governs configuration conformance to audio standards. Jumper J10 is placed in A-B position at the factory.

Jumper	Position	Function
J10	A-B	SMPTE/PAL-M
	B-C	EBU

4-28 Control Track Bias

Jumper J13 is placed in the B (NORM) position at the factory. When in position B, jumper J13 enables control track to conform to SMPTE or EBU format standards, using microprocessor information obtained from pin 19 of the Reference PWA. The jumper can be moved to the A or C positions if you want to force control track circuitry to conform to either EBU or SMPTE standards, regardless of logic level on pin 19 of the Reference PWA.

Jumper	Position	Function
J13	A	EBU (records control track using bias)
	B	NORM
	C	SMPTE (records control track using saturation recording)

4-29 Audio Muting

Jumper J14 is placed in the A-B position at the factory. When in position A-B, jumper J14 mutes audio channels 1 and 2 when the VPR-80 is in shuttle or cue mode. When placed in position B-C, all audio channels are audible when in shuttle or cue mode.

Jumper	Position	Function
J14	A-B	Audio channels 1 and 2 muted
	B-C	Audio not muted

4-30 Audio Alignment Tapes

Ampex audio alignment tapes which are required in audio system test and adjustment procedures are listed in Table 4-1. Refer back to Section 4, Part I, for precautions which apply to the use of these tapes.

The audio alignment tape listed in Table 4-1 is used to check and set VPR-80 playback level and frequency response. The format of the audio alignment tapes is shown in Figure 4-7. This figure also shows corresponding locations of audio and control tracks used in 1-in., Type C, helical scan, videotape recording. Audio alignment tape is recorded full width with the exception of a path of blank (erased) tape which brackets the control track location.

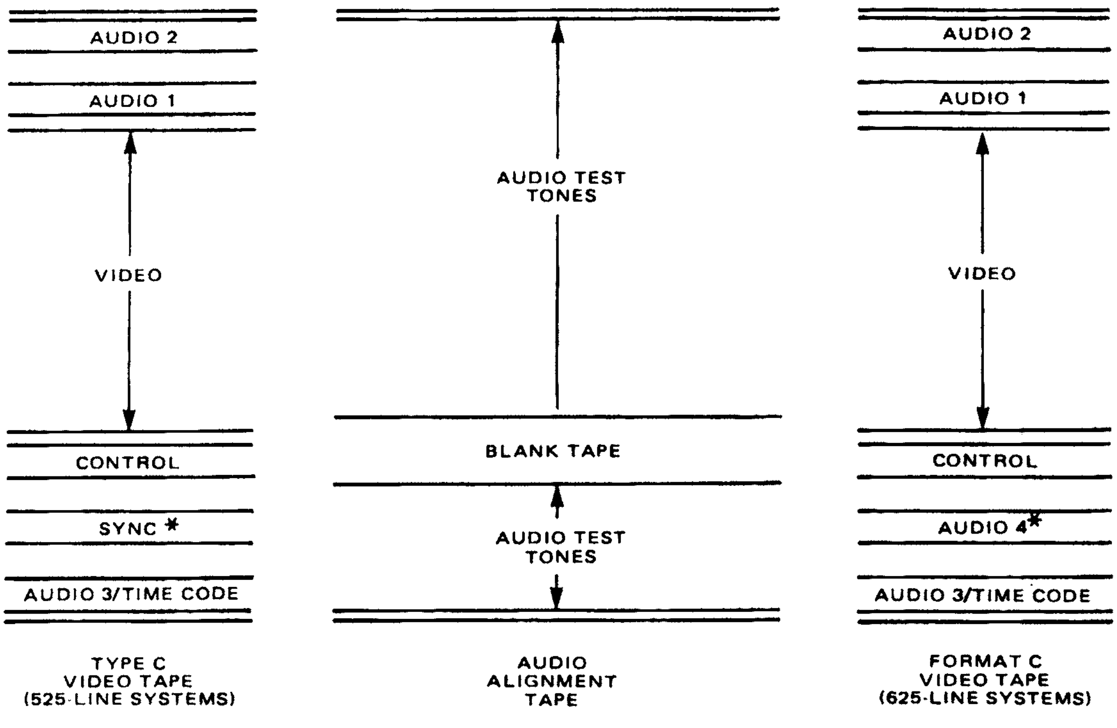
Table 4-1. Audio Alignment and Reference Tapes

Ampex Catalog Number	Description	Length (Minutes)
1498600	Audio Alignment, 525/NTSC*	15
1498601	Audio Alignment, 625/PAL**	15
1498614	Biased Control Track Reference Level (1 kHz at 9.4409 in, 100 nWb/m, 625/PAL**	5

* Included in Maintenance Tool Kit 1450014
** Included in Maintenance Tool Kit 1450015

4-31 Audio PWA Controls

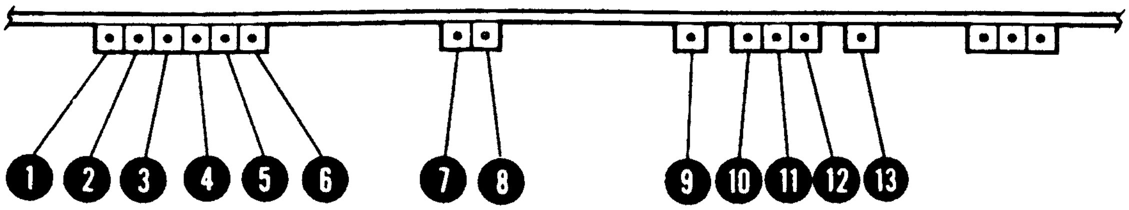
PWA edge-mounted controls on the Audio PWA which are referenced in the audio adjustment procedures are listed in Table 4-2. Other adjustment controls located on the PWA itself are shown in Table 4-10.



* NEITHER OF THESE OPTIONS IS AVAILABLE ON THE VPR-80.

Figure 4-7. Audio Alignment Tape Format

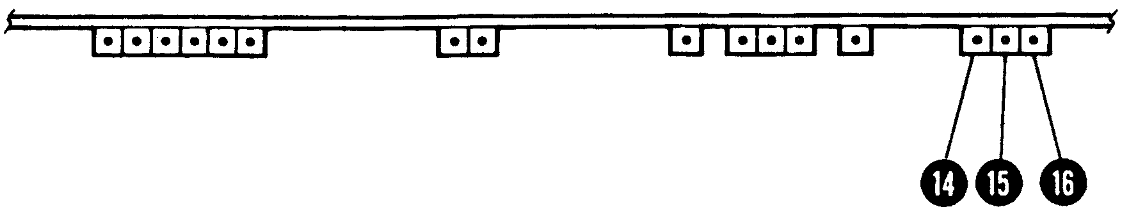
Table 4-2. Audio PWA Edge-Mounted Controls



Index No.	Description	Function
1	Audio 3 unity playback, R68	Unity playback level adjustments. See paragraph 4-49.
2	Audio 2 unity playback, R69	
3	Audio 1 unity playback, R70	
4	Audio 3 unity record, R144	Unity record level adjustments. See paragraph 4-53.
5	Audio 2 unity record, R145	
6	Audio 1 unity record, R146	
7	Audio 3 VU meter adjust, R224	VU meter calibration adjustments. See paragraph 4-55.
8	Audio 2 VU meter adjust, R343	
9	Audio 1 VU meter adjust, R446	
10	Audio 3 EE calibration, R465	EE level calibration adjustments. See paragraph 4-54.
11	Audio 2 EE calibration, R466	
12	Audio 1 EE calibration, R467	
13	Master bias adjust, R491	Master bias drive and optimization adjustment. See paragraph 4-51.

(Continued next page)

Table 4-2. Audio PWA Edge-Mounted Controls (Continued)



Index No.	Description	Function
14	Audio 3 bias drive adjust, R521	Bias drive and optimization adjustments. See paragraph 4-52.
15	Audio 2 bias drive adjust, R522	
16	Audio 1 bias drive adjust, R523	

4-32 Performance Verification

Ampex Type 196 videotape, or equivalent, is used in the following tests. Specifications apply to all audio channels unless specified otherwise. Also, unless specified otherwise, all VPR-80 record and play level controls are placed in center detent (unity) position.

Note

The VPR-80 has transformerless audio outputs. It is aligned at the factory with balanced measuring devices. If instruments such as Hewlett-Packard Model 8903A Audio Analyzer or Sound Technology Model 1710A Distortion Measuring System, or equivalent, are not available, it is not advisable to use power cord ground isolation plugs on devices with unbalanced inputs (i.e., Hewlett-Packard Models 400 or 3400A ac voltmeters); output lines become unbalanced and all output indications will be 6 dB lower than balanced output.

4-33 Playback Frequency Response

Frequency response is checked by playing the appropriate audio alignment tape (control panel AUDIO PLAY controls in detent—unity—position) while observing an audio (ac) voltmeter placed across the corresponding AUDIO OUT connector. Voice announcements on the alignment tape identify the series of test frequencies on the tape. The audio alignment tape, having been recorded effectively full width, plays back lower frequencies at a higher level than the +8 dBm desired. This additional signal, called fringing, is seen and accounted for in Table 4-3.

Table 4-3. Frequency Response Check

Frequency	Audio 1		Audio 2		Audio 3		Notes	Time
	+8 dBm = 0 VU	__ = 0 VU	+8 dBm = 0 VU	__ = 0 VU	+8 dBm = 0 VU	__ = 0 VU		
1 kHz	+9.3		+9.3		+9.3		Gain check	1 minute
10 kHz	+8.4		+8.4		+8.4		Gain check	1 minute
1 kHz	+9.3		+9.3		+9.3		Response check	30 seconds
10 kHz	+8.4		+8.4		+8.4		Response check	30 seconds
63 Hz	Not used							10 seconds
125 Hz								10 seconds
250 Hz							Reference Frequency	10 seconds
500 Hz								10 seconds
1 kHz	+9.3		+9.3		+9.3			10 seconds
2 kHz	Not used							10 seconds
4 kHz								10 seconds
8 kHz								10 seconds
10 kHz	+8.4		+8.4		+8.4			10 seconds
12.5 kHz	Not used							10 seconds
16 kHz	+8.0		+8.0		+8.0			10 seconds
1 kHz	+9.3		+9.3		+9.3		Gain Check	1 minute

When reproducing a recorded track which is the same width as the reproduce head, the playback does not exhibit fringing. Therefore, recordings made with the same head used for playback will not exhibit fringing. If the VPR-80 plays back the alignment tape in accordance with values shown in Table 4-3, playback of its own recording should be nominal across the spectrum, ± system tolerance.

Check playback frequency response as follows:

STEP 1 Thoroughly clean and demagnetize entire tape path. Refer to paragraph 4-14, Part I for cleaning instructions. Demagnetization instructions are given in Section 3 of the *VPR-80 Installation and Operation* manual.

STEP 2 Check tape tensions in accordance with paragraph 4-23, Part I. Adjust tape tensions as necessary.

STEP 3 Thread audio alignment tape on transport (Ampex Part No. 1498600 for 525/NTSC systems, or Part No. 1498601 for 625/PAL systems).

STEP 4 Holding down RECORD, press MASTER RECORD LOCKOUT, and ensure that red indicator is lighted.

STEP 5 Turn all three AUDIO PLAY controls (on primary control panel) to center detent position.

STEP 6 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

STEP 7 Press SPEAKER/PHONES AUDIO 1 (on secondary control panel above the VU meters). Ensure that green AUDIO 1 indicator is lighted. Turn VOLUME control to midrange.

STEP 8 Press PLAY and compare audio voltmeter indications with values listed in Table 4-3. Alignment tape should play back at listed values when VPR-80 is set up so that +8 dBm equals line output level. This is the specified value. Columns have been left blank in the table for the user to enter values for levels other than +8 dB.

STEP 9 Disconnect voltmeter from AUDIO 1 OUT connector, and connect it to AUDIO 2 OUT connector.

STEP 10 Press SPEAKER/PHONES AUDIO 1, and ensure that corresponding green indicator is not lighted. Press AUDIO 2, and ensure that corresponding green indicator is lighted.

STEP 11 Rewind audio alignment tape, and repeat step 8.

STEP 12 Disconnect voltmeter from AUDIO 2 OUT connector, and connect it to AUDIO 3 OUT connector.

STEP 13 Press SPEAKER/PHONES AUDIO 2, and ensure that corresponding green indicator is not lighted. Press AUDIO 3, and ensure that corresponding green indicator is lighted.

STEP 14 Rewind audio alignment tape, and repeat step 8.

4-34 Overall Frequency Response

Check overall frequency response as follows:

STEP 1 Turn on VPR-80 power.

STEP 2 Thoroughly clean and demagnetize entire tape path. Refer to Part I, paragraph 4-14 for cleaning instructions. Demagnetization instructions are given in Section 3 of *VPR-80 Installation and Operation* manual.

STEP 3 Check tape tensions in accordance with Part I, paragraph 4-23 of this manual. Adjust tape tensions as necessary.

STEP 4 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output to 400 Hz at +8 dB (studio operating level).

STEP 5 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-32 regarding balanced and unbalanced measurement devices.

STEP 6 Thread Ampex Type 196 videotape (or equivalent) on transport.

STEP 7 Turn all three AUDIO PLAY controls and all three AUDIO RECORD controls on primary control panel to detent (unity) position.

STEP 8 Zero the tape timer.

STEP 9 Enter record mode. Continue recording the 400-Hz audio oscillator input for 10 seconds (the reference frequency).

STEP 10 Reset audio oscillator output to 50 Hz.

STEP 11 While recording continues, slowly sweep audio oscillator output through all frequencies to 16 kHz. Pause sweep at each of the following frequencies:

50 Hz
100 Hz
500 Hz
1 kHz
5 kHz
10 kHz
12.5 kHz
16 kHz

STEP 12 Press CUE switch to rewind tape to zero tape time.

STEP 13 Press PLAY, and compare audio voltmeter indications with specifications. Tolerances are ±1 dB over the range of 500 Hz to 12 kHz, and ±2 dB over the range of 50 Hz to 16 kHz with respect to the 400-Hz reference tone level.

STEP 14 Disconnect audio oscillator from AUDIO 1 IN connector and connect it to AUDIO 2 IN connector. Set oscillator output to 400 Hz at +8 dB (studio operating level).

STEP 15 Disconnect voltmeter from AUDIO 1 OUT connector, and connect it to AUDIO 2 OUT connector. Rewind tape.

STEP 16 Repeat steps 8 through 13, testing overall frequency response of audio channel 2.

STEP 17 Disconnect audio oscillator from AUDIO 2 IN connector and connect it to AUDIO 3 IN connector. Set oscillator output to 400 Hz at +8 dB (studio operating level).

STEP 18 Disconnect voltmeter from AUDIO 2 OUT connector, and connect it to AUDIO 3 OUT connector. Rewind tape.

STEP 19 Repeat steps 8 through 13, testing overall frequency response of audio channel 3.

If response is not within tolerances stated in step 13, see paragraph 4-56 for record equalization adjustment procedure.

4-35 Depth of Erasure

Characteristic	**Specification**
Depth of erasure (reference recording at 200 nWb/m at 1 kHz)	-70 dB

Verify compliance with depth-of-erasure specification as follows:

STEP 1 Thread a reel of Ampex Type 196 videotape (or equivalent) onto transport.

STEP 2 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output frequency to 1 kHz.

STEP 3 Connect a spectrum analyzer (Hewlett-Packard Model 3580A, or equivalent) to AUDIO 1 OUT connector to identify 1-kHz component.

STEP 4 Make a 1-minute recording at +6 dB over studio operating level. Rewind tape.

STEP 5 Remove audio input signal, and short the three audio input pins (in the AUDIO 1 IN type XLR connector) together.

STEP 6 Play tape for 30 seconds and observe spectrum analyzer indication.

STEP 7 After 30 seconds of playback, enter record mode, thus recording over last 30 seconds of 1-minute recording made in step 4, and thus erasing audio channel 1.

STEP 8 Rewind tape and play back 1-minute recording. Observe change in spectrum analyzer indication midway through recording. Amount of residual 1 kHz in the second half of recording should be 70 dB or more below recorded level. That is, +14 dBm recording minus 70 dB erase = residual 1 kHz, or -56 dBm (or less).

STEP 9 Repeat steps 1 through 8 for audio channel 2.

STEP 10 Repeat steps 1 through 8 for audio channel 3.

4-36 Signal-to-Noise

Characteristic	Specification
Signal-to-noise (with respect to +8 dB above reference level)	Audio 1 and 2: -56 dB Audio 3: -54 dB

Verify compliance with signal-to-noise specification as follows:

STEP 1 Thread Ampex Type 196 videotape, or equivalent, onto transport.

STEP 2 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output frequency to 1 kHz.

STEP 3 Connect an audio (ac) voltmeter to the AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-32 regarding balanced and unbalanced measurement devices.

STEP 4 Make a 1-minute recording at +8 dB over studio operating level and rewind tape (8 dB over +8 dBm = peak). See Table 4-4.

Table 4-4. Signal-to-Noise Verification Indications (dBm)

Studio Operating Level	Channel Record Level (Peak)	Channel Playback Level			
		Balanced Output		Unbalanced Output	
		A1/A2	A3	A1/A2	A3
+8	+16	-40	-38	-46	-44

STEP 5 Ensure that all shields are in place and aligned as follows:

a. Takeup motor shield in place and secured.

b. Relay shield cover on the Audio PWA in place.

c. Audio PWA shield in place and secured.

d. Rear door assembly (card cage) in closed position and secured.

Note

Audio head stack base casting has two pressed-in locating pins located near the front of the casting (tape side). These pins locate audio head stack shield.

e. Head stack shield is touching locating pins on both sides. See Figure 4-8.

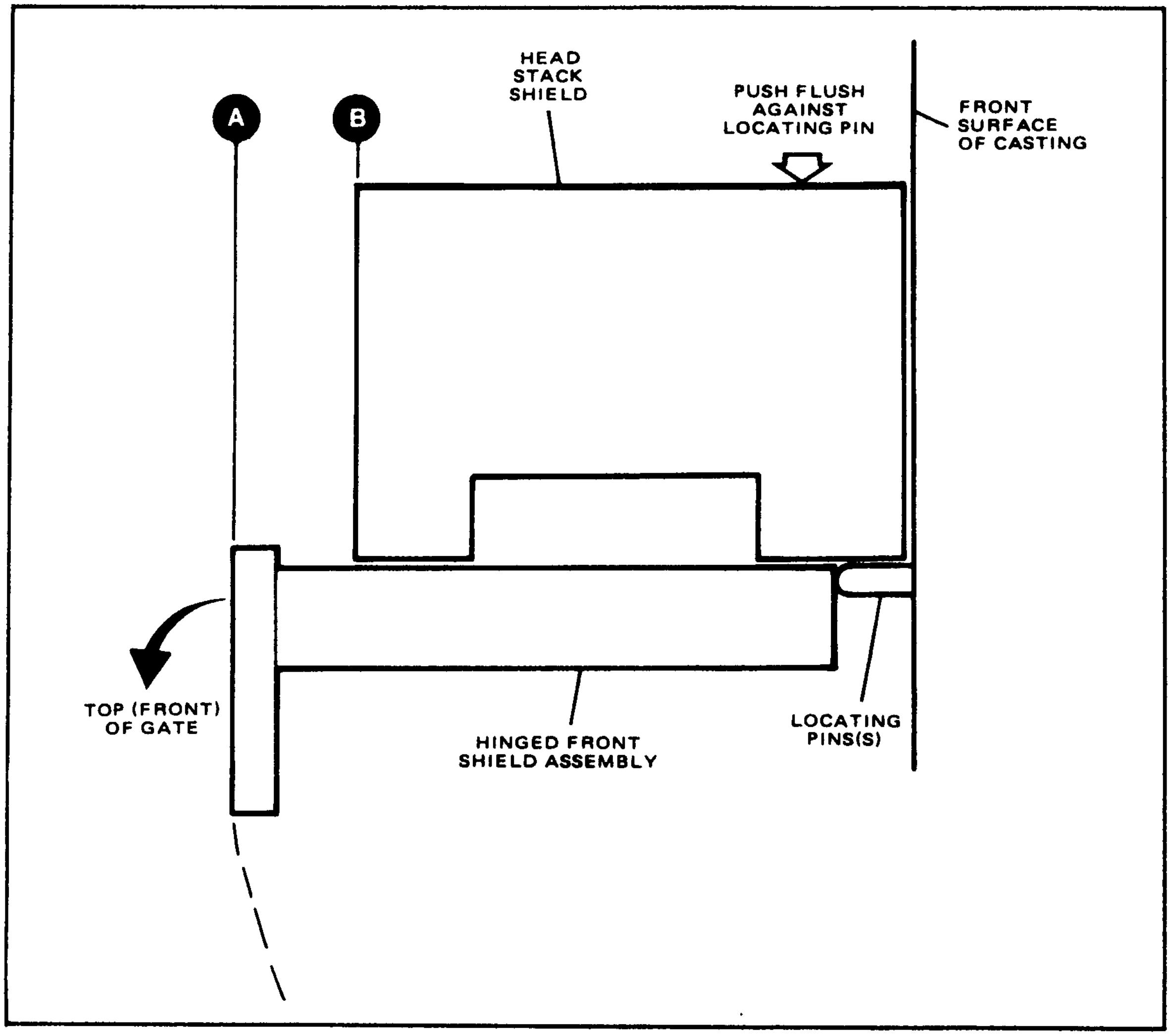


Figure 4-8. Hinged Front Shield Assembly Closure

STEP 6 Adjust hinged front shield assembly so that top (front) of gate (Figure 4-8 A) is parallel with top (front) of head stack shield (Figure 4-8 B) when closed. Check for contact between hinged front shield assembly and head stack shield at a minimum of three places.

STEP 7 Remove audio input signal, and short the three audio input pins (in the AUDIO 1 IN type XLR connector) together.

STEP 8 Play tape for 30 seconds and observe audio voltmeter indication.

STEP 9 After 30 seconds of playback, enter record mode, thus recording over last 30 seconds of 1-minute recording made in step 4, and thus erasing audio channel 1.

STEP 10 Rewind tape and play back 1-minute recording. Observe change in audio voltmeter indication midway through recording. In the second half of the recording the audio (ac) voltmeter should indicate 56 dB below peak record level as shown in Table 4-4.

STEP 11 Repeat steps 1 through 10 for audio channel 2. Audio (ac) voltmeter should indicate 56 dB below peak record level as shown in Table 4-4.

STEP 12 Repeat steps 1 through 10 for audio channel 3. Audio (ac) voltmeter should indicate -54 dB below peak record level as shown in Table 4-4.

Noise floor should be 56 dB below recording made in step 4 for channels 1 and 2 (54 dB for channel 3). For example, recording is +8 dB above +8-dBm operating level, or +16 dBm. Noise floor is 56 dB below +16 dBm for channels 1 and 2 (54 dB below for channel 3), or -40 dBm for channels 1 and 2 (-38 dBm for channel 3).

Note

Channel 3 has wideband capability for time code.

4-37 Playback Crosstalk

Playback crosstalk between channels 1 and 2 is measured by shorting the input of one channel and recording the 1-kHz reference frequency at +8 dBm level on the other. The recording is then played back while monitoring the shorted channel with a level meter.

4-38 Channel 1 to Channel 2. Crosstalk level specification is as follows:

Characteristic	**Specification**
Playback crosstalk (1 kHz at +8 dBm, or 100 nWb/m)	-50 dB maximum

Verify channel 1 to channel 2 crosstalk level specification as follows:

STEP 1 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output frequency to 1 kHz.

STEP 2 Short the three audio input pins in the AUDIO 2 IN (type XLR) connector together.

STEP 3 Make a 1-minute recording at +8 dBm. Rewind tape.

STEP 4 Remove short circuit from AUDIO 2 IN connector.

STEP 5 Connect an audio (ac) voltmeter to the AUDIO 2 OUT connector.

Note

Refer to note in paragraph 4-32 regarding balanced and unbalanced measurement devices.

STEP 6 Ensure that all shields are in place and aligned as follows:

a. Takeup motor shield in place and secured.

b. Relay shield cover on Audio PWA in place.

c. Audio PWA shield

d. Rear door assembly (card cage) in closed position and secured.

Note

The audio head stack base casting has two pressed-in locating pins near the front of the casting (tape side). These pins locate audio head stack shield.

e. The audio head stack shield is touching locating pins on both sides.

STEP 7 Play back the 1-minute recording. The audio (ac) voltmeter should indicate 50 dB (or more) below the +8 dBm recording level (-42 dBm maximum).

4-39 Channel 2 to Channel 1. Crosstalk level specification is as follows:

Characteristic	Specification
Playback crosstalk (1 kHz at +8 dBm, or 100 nWb/m)	-50 dB maximum

Verify channel 2 to channel 1 crosstalk level specification as follows:

STEP 1 Connect an audio oscillator to AUDIO 2 IN connector. Set oscillator output frequency to 1 kHz.

STEP 2 Short the three audio input pins in the AUDIO 1 IN (type XLR) connector together.

STEP 3 Make a 1-minute recording at +8 dBm. Rewind tape.

STEP 4 Remove short circuit from AUDIO 1 IN connector.

STEP 5 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-32 regarding balanced and unbalanced measurement devices.

STEP 6 Ensure that all shields are in place and aligned as follows:

a. Takeup motor shield in place and secured.

b. Relay shield cover on Audio PWA in place.

c. Audio PWA shield in place and secured.

d. Rear door assembly (card cage) in closed position and secured.

Note

Audio head stack base casting has two pressed-in locating pins near the front of the casting (tape side). These pins locate audio head stack shield.

e. Audio head stack shield is touching locating pins on both sides.

STEP 7 Play back 1-minute recording. Audio (ac) voltmeter should indicate 50 dB (or more) below the +8 dBm recording level (-42 dBm maximum).

4-40 Distortion

Third harmonic distortion is the ratio between the level of the third order harmonic and the fundamental frequency expressed in percent when recording at reference level.

4-41 Distortion at 100-nWb/m Record Level. Third harmonic distortion specification for VPR-80 recordings made at studio operating level (+8 dBm) is as follows:

Characteristic	Specification
Distortion at 100 nWb/m (+8 dBm)	1% maximum

Verify third harmonic distortion specification as follows:

STEP 1 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output frequency to 1 kHz.

STEP 2 Connect a spectrum analyzer to the AUDIO 1 OUT connector to identify the 3-kHz component.

STEP 3 Make a 1-minute recording at +8 dBm (studio operating level).

STEP 4 Play back the 1-minute recording. Examine the 3-kHz component of the output. This level will be -32 dBm, or less.

STEP 5 Repeat steps 1 through 4 for audio channel 2.

STEP 6 Repeat steps 1 through 4 for audio channel 3.

Since +8 dBm equals 2.0V into 600Ω, 1% equals 20 mV, or -32 dBm. Thus, third harmonic distortion (at 3 kHz) is 40 dB below the +8-dBm operating level.

4-42 **Distortion at 251-nWb/m Record Level.** Third harmonic distortion specification for VPR-80 recordings made +8 dBm above studio operating level (+16 dBm) is as follows:

Characteristic	Specification
Distortion at 251 nWb/m (+16 dBm)	3% maximum

Verify third harmonic distortion specification as follows:

STEP 1 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output frequency to 1 kHz.

STEP 2 Connect a spectrum analyzer to AUDIO 1 OUT connector to identify the 3-kHz component.

STEP 3 Make a 1-minute recording at +8 dBm above studio operating level (+16 dBm).

STEP 4 Play back the 1-minute recording. Examine the 3-kHz component of the output. This level will be -14.5 dBm, or less.

STEP 5 Repeat steps 1 through 4 for audio channel 2.

STEP 6 Repeat steps 1 through 4 for audio channel 3.

Since +16 dBm equals 5.0V into 600Ω, 3% equals 150 mV, or -14.5 dBm. Thus, third harmonic distortion (at 3 kHz) is 30.5 dB below the +16 dBm operating level.

4-43 Wow and Flutter

Long- and short-period fluctuations in tape speed (wow and flutter) are evidenced by frequency modulation of the precisely recorded 3-kHz tone on a flutter test tape. Traditionally, wow and flutter specifications are listed under audio characteristics, but because wow and flutter are actually tape transport faults, not faults of the audio system, the performance verification procedure is included in transport alignment procedures (Section 7, Part II).

4-44 Microphone Gains

Verify microphone gain as follows:

STEP 1 With VPR-80 power off, loosen two captive screws at cabinet rear and lower rear door assembly as shown in Part I, Figure 4-3.

STEP 2 For access to the Audio PWA, disengage four captive screws securing the Audio PWA shield, and detach shield. Refer to Figure 4-6.

STEP 3 Place Audio PWA jumper J4 in B-C position (channel 1 enabled for microphone input). See Table 4-9.

STEP 4 Connect a 1-kHz, -45.5-dBm signal to the MICROPHONE input connector on I/O connector panel.

STEP 5 Connect an audio (ac) voltmeter to the AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-32 regarding balanced and unbalanced measurement devices.

STEP 6 Place VPR-80 in stop mode/standby condition.

STEP 7 Press EE switch: EE indicator should be lighted. The audio (ac) voltmeter should indicate +8 dBm ±2 dBm.

STEP 8 Turn VPR-80 power off.

STEP 9 Replace Audio PWA jumper J4 in the A-B position (channel 1 enabled for line input). Place jumper J5 in the B-C position (channel 2 enabled for microphone input).

STEP 10 Disconnect voltmeter from AUDIO 1 OUT connector, and connect it to AUDIO 2 OUT connector. Rewind tape.

STEP 11 Turn VPR-80 power on.

STEP 12 Press EE: EE indicator should be lighted. The audio (ac) voltmeter should indicate +8 dBm ±2 dBm.

STEP 13 Turn VPR-80 power off.

STEP 14 Replace Audio PWA jumper J5 in the A-B position (channel 2 enabled for line input). Place jumper J6 in the B-C position (channel 3 enabled for microphone input).

STEP 15 Disconnect voltmeter from AUDIO 2 OUT connector, and connect it to AUDIO 3 OUT connector. Rewind tape.

STEP 16 Turn VPR-80 power on.

STEP 17 Press EE: EE indicator should be lighted. The audio (ac) voltmeter should indicate +8 dBm ±2 dBm.

STEP 18 Turn VPR-80 power off and return jumper J6 to A-B position.

4-45 Monitoring

The three audio channels can be monitored, singly or in any combination, via speaker or headphones.

Verify audio monitoring capability as follows:

STEP 1 Connect an audio oscillator output of 1 kHz at +8 dBm level to each of the three AUDIO IN connectors.

STEP 2 Press SPEAKER/PHONES AUDIO 1: corresponding green audio monitor indicator should light. Note audibility of 1-kHz tone on channel 1. Set VOLUME control to a comfortable audio level.

STEP 3 Press AUDIO 2. Corresponding green audio monitor indicator should light, and audio level from the speaker should increase slightly.

STEP 4 Press AUDIO 3. Corresponding green audio monitor indicator should light, and audio level from speaker should increase slightly.

4-46 Adjustment Controls

Sixteen adjustment controls are mounted on the top edge of the Audio PWA. Refer to Table 4-2.

Other adjustment controls are mounted on the Audio PWA itself. To gain accesss to these controls, remove shield covering the PWA. Controls are listed in Table 4-10.

Remove shield covering Audio PWA as follows:

STEP 1 Loosen two captive screws at rear of cabinet and lower rear door assembly as shown in Part I, Figure 4-3.

STEP 2 For access to Audio PWA components and adjustments in the field of the PWA, disengage four captive screws securing Audio PWA shield, and detach shield. Refer to Figure 4-6.

4-47 Successive Approximation

Result of adjustments made while the VPR-80 is in record mode cannot be observed until tape is rewound and played back. To compensate for this, use a process of successive approximation. In general, the process is as follows:

STEP 1 Press ZERO.

STEP 2 Place adjustment control in the center of its range.

STEP 3 Press PLAY and RECORD switches at the same time. Record for 5 to 10 seconds.

STEP 4 Press CUE to rewind tape.

STEP 5 Press PLAY, and monitor the result of the adjustment.

STEP 6 Press CUE to rewind tape.

STEP 7 Press PLAY and RECORD at the same time. Record for 5 to 10 seconds. While recording, readjust control as necessary based on observed result of previous adjustment.

Repeat steps 4 through 7 until desired results of adjustment can be monitored during playback.

4-48 Adjustments

The following paragraphs provide adjustment instructions for all adjustable audio parameters in the VPR-80.

Note

The VPR-80 has transformerless audio outputs, and it is aligned at the factory with balanced measuring devices. If instruments such as Hewlett-Packard Model 8903A Audio Analyzer or Sound Technology Model 1710A Distortion Measuring System, or equivalent, are not available, it is not advisable to use power cord ground isolation plugs on devices with unbalanced inputs (i.e., Hewlett-Packard Models 400 or 3400A ac voltmeters); output lines become unbalanced and all output indications will be 6 dB lower than balanced output.

4-49 Playback Unity Gain

Playback gain and equalization must be properly adjusted before record level and response can be set. Playback unity gain adjustment controls are mounted on the top edge of the Audio PWA as shown in Table 4-2.

Playback Unity Gain

Audio 1: R70
Audio 2: R69
Audio 3: R68

Adjust playback unity gain as follows:

STEP 1 Thoroughly clean and demagnetize entire tape path. Refer to paragraph 4-14, Part I for cleaning instructions. Demagnetization instructions are given in Section 3 of the *VPR-80 Installation and Operation* manual.

Note

If studio operating level is 0 dBm or less (i.e., -10dBm), change jumpers J7, J8, and J9 from A-B position to B-C position. Refer to paragraph 4-26.

STEP 2 Check tape tension in accordance with Part I, paragraph 4-23 of this manual. Adjust tape tension as necessary.

STEP 3 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 4 Thread audio alignment tape (Ampex Part No. 1498600 or 1498601) on transport.

STEP 5 Turn on VPR-80 power.

STEP 6 Turn all three AUDIO PLAY controls (on primary control panel) to detent (center) position.

STEP 7 Press MASTER RECORD LOCKOUT switch. Red indicator should be lighted.

STEP 8 Press SPEAKER/PHONES AUDIO 1 switch (on secondary control panel above VU meters). Ensure that green AUDIO 1 indicator is lighted. Turn VOLUME control to midrange.

STEP 9 Advance alignment tape to the 1-minute recording of 1 kHz. Stop tape, and zero tape timer.

STEP 10 Enter play mode and adjust R70 (as outlined in paragraph 4-47) for an indication of desired studio operating level on audio (ac) voltmeter.

Because of fringing introduced by full-width alignment tape, for a +8-dBm output level, meter should indicate +9.4 dBm. See Table 4-5 (all values expressed in dBm).

Table 4-5. Indicated Playback Unity Gain (dBm)

Studio Operating Level	Output Level Balanced Line	Output Level Unbalanced Line
+8.0	+9.4	+3.4
+4.0	+5.4	-0.6
0.0	+1.4	-4.6

STEP 11 Disconnect voltmeter from AUDIO 1 OUT connector, and connect it to AUDIO 2 OUT connector.

STEP 12 Enter play mode and adjust R69 for an indication of desired studio operating level on audio (ac) voltmeter.

STEP 13 Disconnect voltmeter from AUDIO 2 OUT connector, and connect it to AUDIO 3 OUT connector.

STEP 14 Enter play mode and adjust R68 for an indication of desired studio operating level on audio (ac) voltmeter.

4-50 Playback Equalization

Playback gain and equalization must be properly adjusted before record level and response can be set. Playback equalization adjustment controls are mounted on the Audio PWA. For access to these controls, remove shield covering the PWA. Refer to paragraph 4-46 and Figure 4-6.

Playback Equalization

Audio 1: R494
Audio 2: R393
Audio 3: R305

The following procedure assumes that playback unity gains have been adjusted in accordance with paragraph 4-49.

Adjust playback equalization as follows:

STEP 1 Thread audio alignment tape (Ampex Part No. 1498600 or 1498601) on transport.

STEP 2 Turn on VPR-80 power.

STEP 3 Press MASTER RECORD LOCKOUT switch. Red indicator should be lighted.

STEP 4 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 5 Advance alignment tape to 10-second recording of 16 kHz. Stop tape, and zero tape timer.

STEP 6 Turn all three AUDIO PLAY controls (on primary control panel) to detent (center) position.

STEP 7 Press SPEAKER/PHONES AUDIO 1 switch (on secondary control panel above VU meters). Ensure that green AUDIO 1 indicator is lighted. Turn VOLUME control to midrange.

STEP 8 Enter play mode and adjust R494 (as outlined in paragraph 4-47) for an indication of desired studio operating level on audio (ac) voltmeter. See Table 4-6 (all values expressed in dBm).

Table 4-6. Indicated Playback Equalization (dBm) at 16 kHz

Studio Operating Level	Output Level Balanced Line	Output Level Unbalanced Line
+8.0	+8.0	+2.0
+4.0	+4.0	−2.0
0.0	0.0	−6.0

STEP 9 Disconnect voltmeter from AUDIO 1 OUT connector, and connect it to AUDIO 2 OUT connector.

STEP 10 Enter play mode and adjust R393 (as outlined in paragraph 4-47) for an indication of desired studio operating level on audio (ac) voltmeter.

STEP 11 Disconnect voltmeter from AUDIO 2 OUT connector, and connect it to AUDIO 3 OUT connector.

STEP 12 Enter play mode and adjust R305 (as outlined in paragraph 4-47) for an indication of desired studio operating level on audio (ac) voltmeter.

4-51 Master Bias

Master bias control is mounted on the top edge of the Audio PWA as shown in Table 4-2.

Master Bias

Audio 1—3: R491

The master bias control provides simultaneous, linear bias adjustment of all audio channels, as well as quick bias adjustment when a tape will be used which requires a different audio bias level.

Proper adjustment of master bias allows sufficient range of adjustment for both individual channel bias and master channel bias.

Adjust master bias control as follows:

STEP 1 Turn VPR-80 power on.

STEP 2 With VPR-80 in stop mode, use a dc voltmeter to measure voltage at U78-6 on Audio PWA. Chip U78 is adjacent to R491 at the top of the PWA. See Table 4-10.

STEP 3 Adjust R491, as necessary, for +8.0 Vdc at U78-6.

After master bias has been adjusted as outlined above, and individual channel bias levels have been adjusted in accordance with instructions in paragraph 4-52, the master bias control, R491, can be used to rebias all three audio channels simultaneously. Only one channel need be monitored.

4-52 Individual Channel Bias

Bias adjustment controls for the three audio channels are mounted on the top edge of the Audio PWA as shown in Table 4-2.

Channel Bias

Audio 1: R523
Audio 2: R522
Audio 3: R521

Adjust individual channel bias levels as follows:

STEP 1 With VPR-80 power off, loosen two captive screws at rear of cabinet and lower rear door assembly as shown in Part I, Figure 4-3.

STEP 2 For access to Audio PWA, disengage four captive screws securing Audio PWA shield, and detach shield. Refer to Figure 4-6.

STEP 3 Place Audio PWA jumper J6 in B-C position (channel 3 enabled for microphone input). Ensure that jumpers J4 and J5 are in the A-B position (channels 1 and 2 enabled for line input).

STEP 4 Thread Ampex Type 196 videotape (or equivalent) on the transport.

STEP 5 Connect an audio (ac) voltmeter to the AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 6 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output to 10 kHz at 10 dBm below studio operating level.

STEP 7 Connect a microphone to MICROPHONE input connector.

STEP 8 Turn on VPR-80 power.

STEP 9 Turn all three AUDIO PLAY controls and all three AUDIO RECORD controls (on primary control panel) to detent (center) position.

STEP 10 Press SPEAKER/PHONES AUDIO 1 and AUDIO 3 switches (on secondary control panel above VU meters). Ensure that green AUDIO 1 and AUDIO 3 indicators are lighted. Turn VOLUME control to midrange.

STEP 11 Connect scope probe to test point TP10. (See Table 4-9.) Adjust scope as necessary to measure audio signals in the range of 150 to 250 mVp-p.

STEP 12 Zero tape timer (press ZERO), and enter record mode (press RECORD and PLAY at same time).

STEP 13 Observing scope, adjust bias control for channel 1 (R523, shown in Table 4-10) for indication of 150 mVp-p.

STEP 14 Key microphone, and announce "150 millivolts."

STEP 15 While recording continues, advance bias control R523 through the following scope indications:

a. 150 mVp-p

b. 175 mVp-p

c. 200 mVp-p

d. 225 mVp-p

e. 250 mVp-p

Pause at each of the above indications and make a voice announcement of the indication on the microphone.

STEP 16 Rewind tape and play back recording. Observe audio voltmeter and oscilloscope. Note announcements of voltage observed on scope required to obtain peak indication on the audio (ac) voltmeter and then drop 2 dB.

STEP 17 Enter record mode and adjust R523 for this voltage.

Note

If channel bias cannot be adjusted as outlined above because adjustment limit has been reached, master bias control, R491, should be adjusted. (See paragraph 4-51.) Then restart this procedure at step 11.

STEP 18 Move audio oscillator input from AUDIO 1 IN connector to AUDIO 2 IN connector.

STEP 19 Move audio (ac) voltmeter from AUDIO 1 OUT connector to AUDIO 2 OUT connector.

STEP 20 Move scope probe to test point TP11 (shown in Table 4-9).

STEP 21 Press SPEAKER/PHONES AUDIO 1, and ensure that corresponding green indicator is not lighted. Press AUDIO 2, and ensure that corresponding green indicator is lighted.

STEP 22 Repeat steps 12 through 17, adjusting R522 (shown in Table 4-10) for bias level of audio channel 2.

STEP 23 Replace Audio PWA jumper J6 in the A-B position (channel 3 enabled for line input). Place jumper J5 in the B-C position (channel 2 enabled for microphone input).

STEP 24 Move audio oscillator input from AUDIO 2 IN connector to AUDIO 3 IN connector.

STEP 25 Move audio (ac) voltmeter from AUDIO 2 OUT connector to AUDIO 3 OUT connector.

STEP 26 Move scope probe to test point TP12 (shown in Table 4-9).

STEP 27 Press SPEAKER/PHONES AUDIO 2, and ensure that corresponding green indicator is not lighted. Press AUDIO 3, and ensure that corresponding green indicator is lighted.

STEP 28 Repeat steps 12 through 17, adjusting R521 (shown in Table 4-10) for bias level of audio channel 3.

STEP 29 Return jumper J5 to A-B position (channel 2 enabled for line input).

STEP 30 Reinstall shield over Audio PWA, and close rear door assembly.

4-53 Record Level Unity

Record level controls for the three audio channels are mounted on the top edge of the Audio PWA as shown in Table 4-2.

Record Level

Audio 1: R146
Audio 2: R145
Audio 3: R144

Note

Playback unity gain, equalization, and bias controls must be aligned in accordance with paragraphs 4-49, 4-50, and 4-51 before beginning this procedure. In addition, AUDIO PLAY controls must be in center detent (unity) position when adjusting record level controls.

Adjust record levels as follows:

STEP 1 Thread Ampex Type 196 videotape (or equivalent) on the transport.

STEP 2 Place all three AUDIO RECORD level controls on primary control panel in detent (unity) position.

STEP 3 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output to 1 kHz at studio operating level.

STEP 4 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 5 Make a short (2-minute) recording, rewind tape, and play back recording. Note correction required between observed playback level and desired studio operating level. Press STOP switch.

STEP 6 With VPR-80 in stop mode, press EE. Ensure that EE indicator is lighted.

STEP 7 Note EE level at AUDIO 1 OUT connector. Adjust R146 by correction difference noted in step 5. Repeat steps 5 and 6 until playback level is equal to desired studio operating level. See Table 4-7 (all values expressed in dBm).

Table 4-7. Indicated Record Level (dBm)

Studio Operating Level	Output Level Balanced Line	Output Level Unbalanced Line
+8.0	+8.0	+2.0
+4.0	+4.0	−2.0
0.0	0.0	−6.0

STEP 8 Move audio oscillator input from AUDIO 1 IN connector to AUDIO 2 IN connector.

STEP 9 Move voltmeter from AUDIO 1 OUT connector to AUDIO 2 OUT connector.

STEP 10 Repeat steps 5, 6, and 7, adjusting R145 for audio channel 2.

STEP 11 Move audio oscillator input from AUDIO 2 IN connector to AUDIO 3 IN connector.

STEP 12 Move voltmeter from AUDIO 2 OUT connector to AUDIO 3 OUT connector.

STEP 13 Repeat steps 5, 6, and 7, adjusting R144 for audio channel 3.

4-54 EE Calibration

EE output calibration controls for the three audio channels are mounted on the top edge of the Audio PWA as shown in Table 4-2.

EE Calibration

Audio 1: R467
Audio 2: R466
Audio 3: R465

Note

All three AUDIO PLAY and all three AUDIO RECORD controls on primary control panel must be in center detent (unity) position when calibrating EE outputs.

Calibrate EE output levels as follows:

STEP 1 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output to 1 kHz at studio operating level.

STEP 2 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 3 With VPR-80 in stop mode, press EE switch. Ensure that EE indicator is lighted.

STEP 4 Observing voltmeter, adjust channel 1 EE output control (R467) so that EE output is equal to studio operating level.

STEP 5 Move audio oscillator input from AUDIO 1 IN connector to AUDIO 2 IN connector.

STEP 6 Move voltmeter from AUDIO 1 OUT connector to AUDIO 2 OUT connector.

STEP 7 Observing voltmeter, adjust channel 2 EE output control (R466) so that EE output is equal to studio operating level.

STEP 8 Move audio oscillator input from AUDIO 2 IN connector to AUDIO 3 IN connector.

STEP 9 Move voltmeter from AUDIO 2 OUT connector to AUDIO 3 OUT connector.

STEP 10 Observing voltmeter, adjust channel 3 EE output control (R465) so that EE output is equal to studio operating level.

4-55 Meter Calibration

Meter calibration controls for the three audio channels are mounted on the top edge of the Audio PWA as shown in Table 4-2.

Meter Calibration

Audio 1: R446
Audio 2: R343
Audio 3: R224

Note

The three AUDIO RECORD controls on the primary control panel must be in detent (unity) position when calibrating AUDIO 1—3 meters.

Calibrate AUDIO 1—3 meters as follows:

STEP 1 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output to 1 kHz at studio operating level.

STEP 2 With VPR-80 in stop mode, press EE. Ensure that EE indicator is lighted.

STEP 3 Observe AUDIO 1 meter on primary control panel and adjust channel 1 meter calibration control (R446) for zero VU.

STEP 4 Move audio oscillator input from AUDIO 1 IN connector to AUDIO 2 IN connector.

STEP 5 Observe AUDIO 2 meter on primary control panel and adjust channel 2 meter calibration control (R343) for zero VU.

STEP 6 Move audio oscillator input from AUDIO 2 IN connector to AUDIO 3 IN connector.

STEP 7 Observe AUDIO 3 meter on primary control panel and adjust channel 3 meter calibration control (R224) for zero VU.

4-56 Record Equalization

Record equalization controls are mounted on the Audio PWA. For access to these controls, remove shield covering the PWA. (Refer to paragraph 4-46 and Figure 4-6.)

Record Equalization

Audio 1: R481
Audio 2: R408
Audio 3: R360

Adjust record equalization as follows:

STEP 1 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output to 1 kHz at studio operating level.

STEP 2 Connect an audio (ac) voltmeter to the AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 3 Record 1 minute of 1-kHz input. Then change oscillator frequency to 15 kHz, and record that input for 1 minute. Rewind tape.

STEP 4 Play recording made in step 3, and, observing voltmeter, adjust channel 1 record equalization control (R481) *only* if playback level at 15 kHz differs by more than ±0.2 dB from level at 1 kHz. See Table 4-10.

STEP 5 Repeat steps 3 and 4 until no further adjustment is necessary.

STEP 6 Move audio oscillator input from AUDIO 1 IN connector to AUDIO 2 IN connector.

STEP 7 Move voltmeter from AUDIO 1 OUT connector to AUDIO 2 OUT connector.

STEP 8 Record 1 minute of 1-kHz input. Then change oscillator frequency to 15 kHz, and record that input for 1 minute. Rewind tape.

STEP 9 Play recording made in step 8; observing voltmeter, adjust channel 2 record equalization control (R408) *only* if playback level at 15 kHz differs by more than ±0.2 dB from the level at 1 kHz. See Table 4-10.

STEP 10 Repeat steps 8 and 9 until no further adjustment is necessary.

STEP 11 Move audio oscillator input from AUDIO 2 IN connector to AUDIO 3 IN connector.

STEP 12 Move voltmeter from AUDIO 2 OUT connector to AUDIO 3 OUT connector.

STEP 13 Record 1 minute of 1-kHz input. Then change oscillator frequency to 15 kHz, and record that input for 1 minute. Rewind tape.

STEP 14 Play recording made in step 13; observing voltmeter, adjust channel 3 record equalization control (R360) *only* if playback level at 15 kHz differs by more than ±0.2 dB from level at 1 kHz. See Table 4-10.

STEP 15 Repeat steps 13 and 14 until no further adjustment is necessary.

4-57 Audio Erase Drive

Erase drive adjustment controls are mounted on the Audio PWA. For access to these controls, remove shield covering the PWA. Refer to paragraph 4-46 and Figure 4-6.

Erase Drive

Audio 1: R261
Audio 2: R268
Audio 3: R275

Adjust erase drive (and depth of erasure) as follows:

STEP 1 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output to 1 kHz.

STEP 2 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 3 Move jumper J6 to position B-C to allow microphone input on channel 3. See Table 4-9.

STEP 4 Connect scope to Audio PWA test point TP7 (channel 1 erase drive). See Table 4-9.

STEP 5 Zero tape timer (press ZERO).

STEP 6 Adjust channel 1 AUDIO RECORD level control on primary control panel to produce a voltmeter indication of 8 dB *above* studio operating level (+14 dBm for a studio operating level of +8 dBm).

STEP 7 Make a 2-minute recording of this input. Then press CUE to rewind tape to beginning of recording.

STEP 8 Disconnect audio oscillator at AUDIO 1 IN connector and play 1 minute of 1-kHz recording.

STEP 9 Enter record mode and adjust channel 1 erase drive control (R261) for an indication of 1.0 Vp-p on scope. Key microphone, and announce "1 volt."

STEP 10 Slowly increase erase drive to 3.5 Vp-p. While increasing erase drive, pause at 0.5V increments and make voice announcements of voltage (p-p) indications on the microphone.

STEP 11 Press CUE to cue tape to beginning of recording.

STEP 12 Play tape and monitor voice announcements on channel 3. Note level at which the 1-kHz signal is reduced by 74 dB ±2 dB

STEP 13 Enter record mode and set channel 1 erase drive control (R261) for the indication noted in step 12. The first minute of the 2-minute recording can then be used to verify this adjustment.

Note

The least amount of erase drive which yields the specified depth of erasure is the best adjustment. This adjustment will provide optimum editor performance.

STEP 14 Ensure that jumper J5 is in the A-B position (channel 2 enabled for line input).

STEP 15 Repeat steps 1 through 13 with channel 2 input and output. Observe channel 2 erase drive at test point TP8 and adjust R268.

STEP 16 Return jumper J6 to A-B position (channel 3 enabled for line input). See Table 4-9.

STEP 17 Move jumper J4 to B-C position (channel 1 enabled for microphone input).

STEP 18 Repeat steps 1 through 13 with channel 3 input and output. Observe channel 3 erase drive at test point TP9 and adjust R275.

STEP 19 Return jumper J4 to A-B position.

4-58 Control Track Erase Drive

Control track erase drive adjustment R193 is mounted on the Audio PWA. For access to this adjustment, remove shield covering the PWA. Refer to paragraph 4-46 and Figure 4-6.

Adjust control track erase drive as follows:

STEP 1 Thread Ampex Type 196 videotape (or equivalent) on transport.

STEP 2 Ensure that MASTER RECORD LOCKOUT and INSERT indicators are not lighted.

STEP 3 Connect oscilloscope probe to Audio PWA test point TP6. See Figure 4-9.

STEP 4 Turn on VPR-80 power and enter record mode.

STEP 5 Adjust control track erase drive (R193) for scope indication of 1.8 Vp-p. See Table 4-10.

4-59 Video Erase Drive

Video erase drive circuitry resides on the Audio PWA. Instructions for adjustment of video erase drive are included in video system alignment procedures. Refer to Section 3, Part II.

4-60 Record-to-Play Crosstalk Cancellation

Note

Crosstalk cancellation adjustment procedures outlined in paragraphs 4-61 and 4-62 must be done in sequence given below.

4-61 Channel 1 to Channel 2. Crosstalk cancellation adjustment controls are mounted on the Audio PWA. For access to these controls, remove shield covering the PWA. Refer to paragraph 4-46 and Figure 4-6.

Crosstalk Cancellation (A1 to A2)

Audio 1 to Audio 2
Overall Level: R542
High Frequencies: R168 Low Frequencies: R166

Adjust crosstalk cancellation (channel 1 to channel 2) as follows:

STEP 1 Thread Ampex Type 196 videotape (or equivalent) on transport.

STEP 2 Connect an audio oscillator to AUDIO 1 IN connector. Set oscillator output to 300 Hz at studio operating level.

STEP 3 Connect an audio (ac) voltmeter to the AUDIO 2 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 4 Establish the following operating conditions on the control panel:

a. Off-tape operation: EE indicator not lighted.

b. Insert edit mode: INSERT indicator lighted.

c. Audio channel 1 enabled: AUDIO 1 RECORD LOCKOUT red indicator *not* lighted.

d. Audio channel 2 inhibited: AUDIO 2 RECORD LOCKOUT red indicator lighted.

STEP 5 Put VPR-80 in insert edit record mode.

STEP 6 Sweep oscillator frequency from 300 Hz to 8 kHz while maintaining +8-dBm input level.

STEP 7 Adjust R542, R168, and R166 until channel 2 output level is at least 30 dB below channel 1 output over range of 300 Hz to 8 kHz. See Table 4-8 (all values expressed in dBm). See Table 4-10.

Table 4-8. Channel-to-Channel Crosstalk Cancellation (dBm)

Studio Operating Level	Output Level Balanced Line	Output Level Unbalanced Line
+8	−22	−28
+4	−26	−32
0	−30	−36

4-62 Channel 2 to Channel 1. Crosstalk cancellation adjustment controls are mounted on the Audio PWA. For access to these controls, remove shield covering the PWA. Refer to paragraph 4-46 and Figure 4-6.

Crosstalk Cancellation (A2 to A1)

Audio 2 to Audio 1 Overall Level: R541

The following procedure assumes that the channel 1 to channel 2 crosstalk cancellation adjustment outlined in paragraph 4-61 has been performed.

Adjust crosstalk cancellation (channel 2 to channel 1) as follows:

STEP 1 Connect an audio oscillator to AUDIO 2 IN connector. Set oscillator output to 300 Hz at studio operating level.

STEP 2 Connect an audio (ac) voltmeter to AUDIO 1 OUT connector.

Note

Refer to note in paragraph 4-48 regarding balanced and unbalanced measurement devices.

STEP 3 Establish the following operating conditions on the control panel:

a. Off-tape operation: EE indicator not lighted.

b. Insert edit mode: INSERT indicator lighted.

c. Audio channel 1 inhibited: AUDIO 1 RECORD LOCKOUT red indicator lighted.

d. Audio channel 2 enabled: AUDIO 2 RECORD LOCKOUT red indicator *not* lighted.

STEP 4 Put VPR-80 in insert edit record mode.

STEP 5 Sweep oscillator frequency from 300 Hz to 8 kHz while maintaining +8-dBm input level.

STEP 6 Adjust R541 until channel 1 output level is at least 30 dB below channel 2 output over the range of 300 Hz to 8 kHz. See Table 4-8 (all values expressed in dBm). See Table 4-10.

4-63 Control Track Playback Level

Control track playback level controls are mounted on the Audio PWA. For access to these controls, remove shield covering the PWA. Refer to paragraph 4-46 and Figure 4-6.

Control Track Playback Level

SMPTE: R98
EBU: R99

4-64 SMPTE (525/60) Systems. Before beginning this adjustment, turn R99 (the EBU control) full clockwise. This is a precaution to avoid interaction with R98.

Adjust control track playback level as follows:

STEP 1 Thread Ampex Type 196 videotape (or equivalent) on transport.

STEP 2 Ensure that editor is off (neither INSERT nor ASSEM indicator is lighted). Make a 2-minute recording and rewind tape.

STEP 3 Connect scope probe to test point TP4. See Table 4-9.

STEP 4 Play recording made in step 2, and adjust R98 (SMPTE) for 6 Vp-p at TP4. See Table 4-10.

Note

Playback gain can also be verified using 525/NTSC highband carrier video reference tape (Ampex Part No. 1498604).

4-65 EBU (625/50) Systems. Adjust control track playback level as follows:

STEP 1 Thread 625/PAL biased control track reference level tape (Ampex Part No. 1498614) on transport.

STEP 2 Connect scope probe to test point TP4. See Table 4-9.

STEP 3 Play reference tape, and adjust R99 (EBU) for 6 Vp-p at TP4. See Table 4-10.

4-66 Control Track Record Level

4-67 SMPTE (525/60) Systems. Control track record drive is not adjustable in SMPTE (525/60) systems. Control R441 is the adjustment device in EBU (625/50) systems. It is not used in SMPTE (525/60) systems.

4-68 EBU (625/50) Systems. The control track record level control is mounted on the Audio PWA. For access to this control, remove shield covering the PWA. Refer to paragraph 4-46 and Figure 4-6.

Control Track Record Level

EBU: R441

Adjust control track record level as follows:

STEP 1 Thread Ampex Type 196 videotape (or equivalent) on transport.

STEP 2 Make a 2-minute recording and rewind tape.

STEP 3 Connect scope probe to test point TP4. See Table 4-9.

STEP 4 Play recording made in step 2. The newly recorded control track level should be 6 Vp-p.

STEP 5 If control track level is not 6 Vp-p, adjust R441 clockwise to increase or counterclockwise to decrease control track drive. See Table 4-10.

STEP 6 Repeat step 4 to confirm adjustment.

4-69 Channel 3 to Control Track Crosstalk Cancellation

Crosstalk cancellation adjustment controls are mounted on the Audio PWA. For access to these controls, remove shield covering the Audio PWA. Refer to paragraph 4-46 and Figure 4-6.

Crosstalk Cancellation (A3 to CT)

Low Frequencies:	R46
Midrange Frequencies:	R44
High Frequencies:	R113

4-70 SMPTE (525/60) Systems. Channel 3 to control track crosstalk cancellation is not adjustable in SMPTE (525/60) systems in which the control track is a saturated recording. Simply ensure that R46 is at its full counterclockwise position. See Table 4-10.

4-71 EBU (625/50) Systems. Adjust crosstalk cancellation (channel 3 to control-track) as follows:

STEP 1 Connect an audio oscillator to AUDIO 3 IN connector.

STEP 2 Establish the following operating conditions on control panel:

a. EE operation: EE indicator lighted.

b. Insert edit mode: INSERT indicator lighted.

c. Video and Audio channels 1 and 2 inhibited: VIDEO, AUDIO 1, and AUDIO 2 RECORD LOCKOUT red indicators lighted.

d. Audio channel 3 enabled: AUDIO 3 RECORD LOCKOUT red indicator *not* lighted.

STEP 3 Increase channel 3 AUDIO RECORD control on VPR-80 control panel to maximum gain.

STEP 4 Connect scope probe to test point TP4. See Table 4-9.

STEP 5 Put VPR-80 in insert edit record mode.

STEP 6 Set audio oscillator frequency to 100 Hz, and adjust R46 for minimum audio crosstalk (100 Hz) at TP4. See Table 4-10.

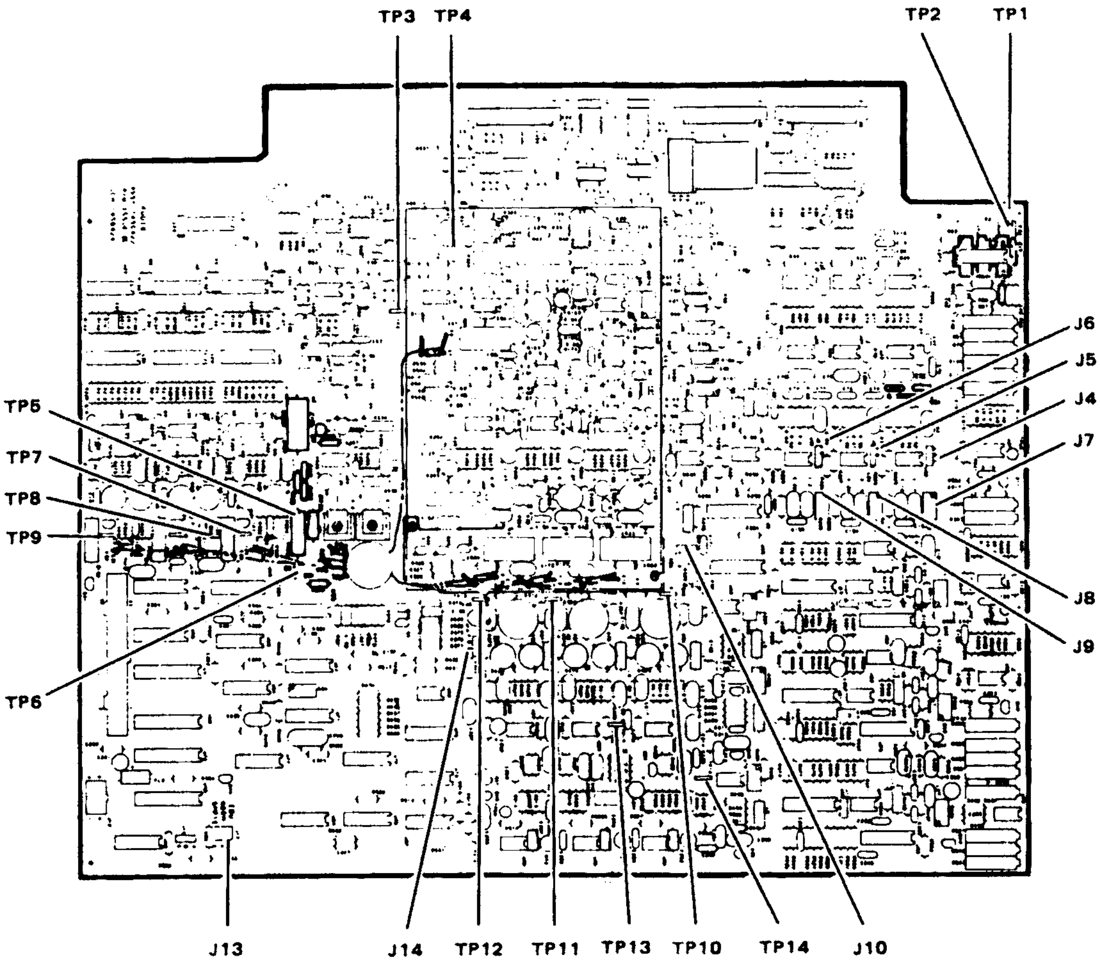
STEP 7 Sweep oscillator to frequencies from 1 kHz through 10 kHz. Adjust R113 and R44 for minimum crosstalk at TP4.

Note

R113 and R44 are interactive.

STEP 8 Sweep oscillator from 100 Hz through 10 kHz and verify that the audio crosstalk component on the control track waveform at TP4 is 1 Vp-p or less throughout the frequency range.

Table 4-9. Audio PWA Jumpers and Test Points



Jumper	Position	Function
J4	A-B	Audio 1 line input enabled.
	B-C	Audio 1 microphone input enabled.
J5	A-B	Audio 2 line input enabled.
	B-C	Audio 2 microphone input enabled.

(Continued next page)

Table 4-9. Audio PWA Jumpers and Test Points (Continued)

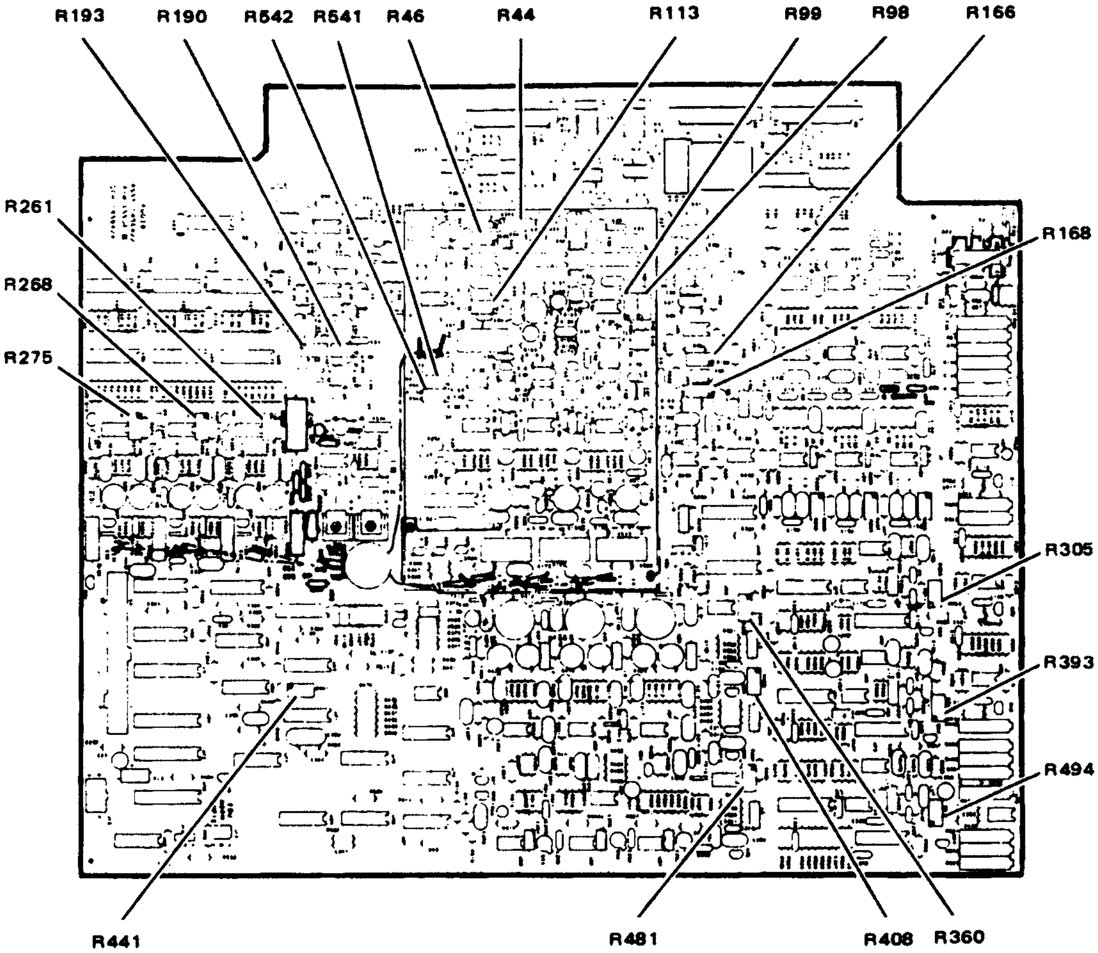
Jumper	Position	Function
J6	A-B	Audio 3 line input enabled.
	B-C	Audio 3 microphone input enabled.
J7	A-B	Audio 1 record gain: Setting for normal studio operating levels (i.e., +4 dB or +8 dB).
	B-C	Use with semiprofessional operating levels (i.e., −10 dB).
J8	A-B	Audio 2 record gain: Setting for normal studio operating levels (i.e., +4 dB or +8 dB).
	B-C	Use with semiprofessional operating levels (i.e., −10 dB).
J9	A-B	Audio 3 record gain: Setting for normal studio operating levels (i.e., +4 dB or +8 dB).
	B-C	Use with semiprofessional operating levels (i.e., −10 dB).
J10	A-B	SMPTE/PAL-M format standard.
	B-C	EBU format standard.
J13	A	EBU: control track bias forced to EBU standard.
	B	NORMAL: control track recorded in accordance with Reference PWA.
	C	SMPTE: control track bias forced to SMPTE standard.
J14	A-B	Audio muted in shuttle and cue modes.
	B-C	Audio not muted in either shuttle or cue mode.

(Continued next page)

Table 4-9. Audio PWA Jumpers and Test Points (Continued)

Test Point	Function
TP1	Control track monitor
TP2	Audio monitor output
TP3	Audio 3 record level
TP4	Control track playback signal-analog
TP5	Video erase
TP6	Control track head
TP7	Audio 1 erase head current
TP8	Audio 2 erase head current
TP9	Audio 3 erase head current
TP10	Audio 1 record/play head current (100Ω)
TP11	Audio 2 record/play head current (100Ω)
TP12	Audio 3 record/play head current (100Ω)
TP13	Audio 2 record level
TP14	Audio 1 record level

Table 4-10. Audio PWA Adjustments



Reference Designation	Function
R44	Audio 3 to control track crosstalk cancellation (midrange frequencies)
R46	Audio 3 to control track crosstalk cancellation (low frequencies)
R68*	Audio 3 playback unity gain
R69*	Audio 2 playback unity gain
R70*	Audio 1 playback unity gain
R98	Control track playback level (SMPTE)

(Continued next page)

Table 4-10. Audio PWA Adjustments (Continued)

Reference Designation	Function
R44	Audio 3 to control track crosstalk cancellation (midrange frequencies)
R46	Audio 3 to control track crosstalk cancellation (low frequencies)
R68*	Audio 3 playback unity gain
R69*	Audio 2 playback unity gain
R70*	Audio 1 playback unity gain
R98	Control track playback level (SMPTE)
R99	Control track playback level (EBU)
R113	Audio 3 to control track crosstalk cancellation (high frequencies)
R144*	Audio 3 record unity gain
R145*	Audio 2 record unity gain
R146*	Audio 1 record unity gain
R166	Audio 1 into Audio 2 crostalk cancellation (high frequencies)
R168	Audio 1 into audio 2 crosstalk cancellation (low frequencies)
R190	Video erase drive
R193	Control track erase drive
R224*	Audio 3 VU meter calibration
R261	Audio 1 erase drive
R268	Audio 2 erase drive
R275	Audio 3 erase drive
R305	Audio 3 playback equalization
R343*	Audio 2 VU meter calibration
R360	Audio 3 record equalization
R393	Audio 2 playback equalization
R408	Audio 2 record equalization
R441	Control track record level (EBU)
R446*	Audio 1 VU meter calibration
R465*	Audio 3 EE calibration
R466*	Audio 2 EE calibration
R467*	Audio 1 EE calibration
R481	Audio 1 record equalization
R491*	Master bias adjust
R494	Audio 1 playback equalization
R521*	Audo 3 bias drive
R522*	Audio 2 bias drive
R523*	Audio 1 bias drive
R541	Audio 2 into Audio 1 crosstalk cancellation (overall)
R542	Audio 1 into Audio 2 crosstalk cancellation (overall)

* Mounted on top edge of Audio PWA. Refer to Table 4-2.

PART II
SECTION 5
SERVO SYSTEM

5-1 GENERAL

This section provides theory of operation information for the servo system, as well as instructions for removing and reinstalling the AST Driver PWA, tension arm, scanner, and capstan assemblies. It also contains procedures for cleaning and replacing parts within these assemblies. Alignment of the AST servo, capstan tach, scanner tach, and tension arm assembly is explained. A/D converter gain and zero offset adjustments are also spelled out in detail.

The following drawings, which are included in the *VPR-80 Parts Lists and Schematics* manual, are referenced in this section.

Drawing	Drawing No.
AST Servo PWA	1450256
AST Servo PWA Schematic	1450258
AST Driver PWA	1450266
AST Driver PWA Schematic	1450268
Servo PWA	1465234
Servo PWA Schematic	1450308
Capstan Tach PWA	1463431
Capstan Tach PWA Schematic	1463433
Photo Potentiometer PWA	1461341
Photo Potentiometer PWA Schematic	1461350
Tension Arm (LED) PWA	1461040
Tension Arm (LED) PWA Schematic	1461164
Reel Tach PWA and Schematic	1468525
System Interconnect Wiring Diagram	1465497

In addition, the following illustrations are included at the end of this section.

Figure 5-66.	AST Servo PWA Test Points and Adjustments
Figure 5-67.	AST Driver PWA Test Points and Adjustments
Figure 5-68.	Servo PWA Test Points, Jumpers, and Adjustments
Figure 5-69.	Capstan Tach PWA Test Points and Adjustments
Figure 5-70.	Photo Potentiometer PWA Adjustments

5-2 THEORY OF OPERATION

5-3 General

Physical components of the servo system are: Servo PWA, AST Servo PWA, AST Driver PWA, and capstan, scanner, and tension arm assemblies. Functionally, the servo system includes capstan, scanner, reel motor, and AST servos. The Servo PWA also includes the servo system control interface and microprocessor (CPU) and the control track generator. The AST Servo also includes playback sync processing and reference pulse generator circuits.

The servo system is a low-level power system providing low-level output signals which are then amplified by the AST Driver PWA and four motor drive amplifiers (MDAs). The capstan/scanner and reel MDAs are considered part of the transport system and are discussed in Section 7, Part II.

In discussions that follow, circuit reference designations on the Servo and AST Servo PWAs are preceded by the PWA number (i.e., 5 or 4). Thus, for example, 5U33 indicates chip U33 on the Servo PWA, and 4U43 indicates chip U43 on the AST Servo PWA.

Major circuits of the servo system are summarized below.

5-4 Control Interface and CPU Kernel

The control interface connects the system data bus and system address/control bus to the servo system CPU and kernel. The Servo CPU interprets commands from the primary CPU on the Control PWA, controls the servo system accordingly, and returns servo status information back to the primary CPU.

The servo system kernel is composed of the CPU, EPROMs, RAM, address decoders, and I/O buffers. The CPU exercises control over the servo system via a data bus and address/control bus structure which is independent of the system bus structure. The servo CPU communicates with servo system analog circuits through A/D and D/A converters.

The control interface and servo system CPU kernel are discussed in detail in paragraphs 5-13 through 5-36.

5-5 Reference PWA Circuits

The Reference PWA in card cage slot 2, Ampex Part No. 1450346 (NTSC), 1450356 (PAL/SECAM), or 1450363 (PAL-M), includes two major circuits which are of particular relevance to the servo system: the reference selector and the color field 1 identifier.

The reference selector supplies the selected composite sync signal to reference pulse generator circuits on the AST Servo PWA for further processing. The reference pulse generator furnishes reference vertical, reference frame, 2H, 16H, and 256H to the control, servo, and audio systems. Reference selector circuits are discussed in detail in Section 3, Part II.

Color field 1 identifier circuits supply the color field 1 reference signal to the control track generator on the Servo PWA. Color field 1 identifier circuits are discussed in detail in Section 3, Part II.

5-6 Reference Pulse Generator

Reference selector circuits on the Reference PWA provide the selected composite sync signal to the reference pulse generator on the AST Servo PWA. Reference pulse generator outputs are frame rate, vertical rate, and multiples of horizontal rate. Reference pulse generator outputs are distributed to the control, video, and audio systems as well as to the servo system. All reference outputs are synchronized with the selected reference composite sync input. If that input is absent, reference pulse generator outputs are derived from a free running oscillator.

The reference pulse generator is discussed in detail in paragraph 5-38.

5-7 Playback Sync Processor

Playback sync processor circuits on the AST Servo PWA use the tape sync signal from the video system to provide playback vertical reference and vertical blanking pulses to the time-base corrector, and vertical blanking to the video system. The vertical blanking signal and a servo vertical reference are also furnished to the Reference PWA for insertion of vertical sync in the video output to the picture monitor. A scanner phase error signal (derived from processed scanner tach) is provided to the scanner servo, and playback frame information is furnished to the AST servo.

The playback sync processor is discussed in detail in paragraph 5-43.

5-8 Control Track Logic

The VPR-80 generates a control track signal when in nonedit record and assemble edit modes. Depending on the applicable video standard, the control track waveform conforms with either SMPTE Recommended Practice RP 85-1979 or EBU Technical Information Sheet No. 7. In play modes, the off-tape control track signal is compared with reference frame, 2X frame, and (EBU only) 4X frame to regulate capstan speed and maintain color framing.

Control track logic is discussed in detail in paragraph 5-47.

5-9 Scanner Servo

The scanner servo is composed of two loops: velocity and phase (position). At scanner motor turn-on, the velocity loop drives the scanner motor to lock (field rate) speed as quickly as possible. It maintains lock speed by use of a digital ramp-and-sample circuit which is triggered and sampled by delayed scanner tach pulses. The phase loop also uses a digital ramp generator which is triggered by reference vertical and sampled at delayed tach time, and the phase loop also measures scanner phase error during edit play mode. If the scanner phase on tape differs by more than 10 µs from the scanner phase of the VPR-80 upon which the tape is being edited, the servo signals the operator that edit optimization is required.

The scanner servo is discussed in detail in paragraph 5-54.

5-10 Capstan Servo

The capstan servo regulates the speed of tape travel in all modes except shuttle. The servo system CPU causes a programmable interval timer to generate a reference frequency for comparison with capstan tach frequency. Capstan motor speed is corrected until tach frequency matches reference frequency. Reference frequency can be varied at vertical rate by the CPU.

The capstan servo is discussed in detail in paragraph 5-62.

5-11 AST Servo

When in nonedit play modes, the Automatic Scan Tracking (AST)* servo controls transverse position of the video record/play head. The AST servo senses tracking errors by detecting variations in the off-tape rf envelope. A feedback arrangement alters the transverse position of the record/play head, causing it to follow the center of the helical video track. Head deflection compensates for tape-speed-induced tracking errors in slow motion and still-frame modes of operation. The head can be deflected ±1 helical video track.

The AST servo is discussed in detail in paragraph 5-69.

5-12 Reel Servos

Takeup and supply reel servos are essentially identical. They maintain proper tape tensions applicable to the commanded mode of operation and tape speed. Digitized tension arm position voltage, summed with the applicable reference voltage, is made available continuously to the servo system CPU. The CPU generates error correction words which are converted to analog form and supplied to reel MDAs as error voltages. Takeup and supply reel servos also continuously supply the CPU with reel speeds and calculated tape pack diameters. In addition, tape speed information is furnished to the AST servo. Tape speed is calculated from information supplied by the tape timer tach processor.

Reel servos are discussed in detail in paragraph 5-96.

5-13 Servo System Kernel

The servo system kernel is shown in Figure 5-1. It is located on the Servo PWA and is composed of an 8-bit microprocessor (CPU) and the chips which are connected to the CPU. Thus, the servo system kernel includes 16K bytes of erasable programmable read-only memory (EPROM), 1024 bytes of random access memory (RAM), address decoder, internal data buffer, AST data buffer, and AST address buffer.

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*TM Ampex Corporation

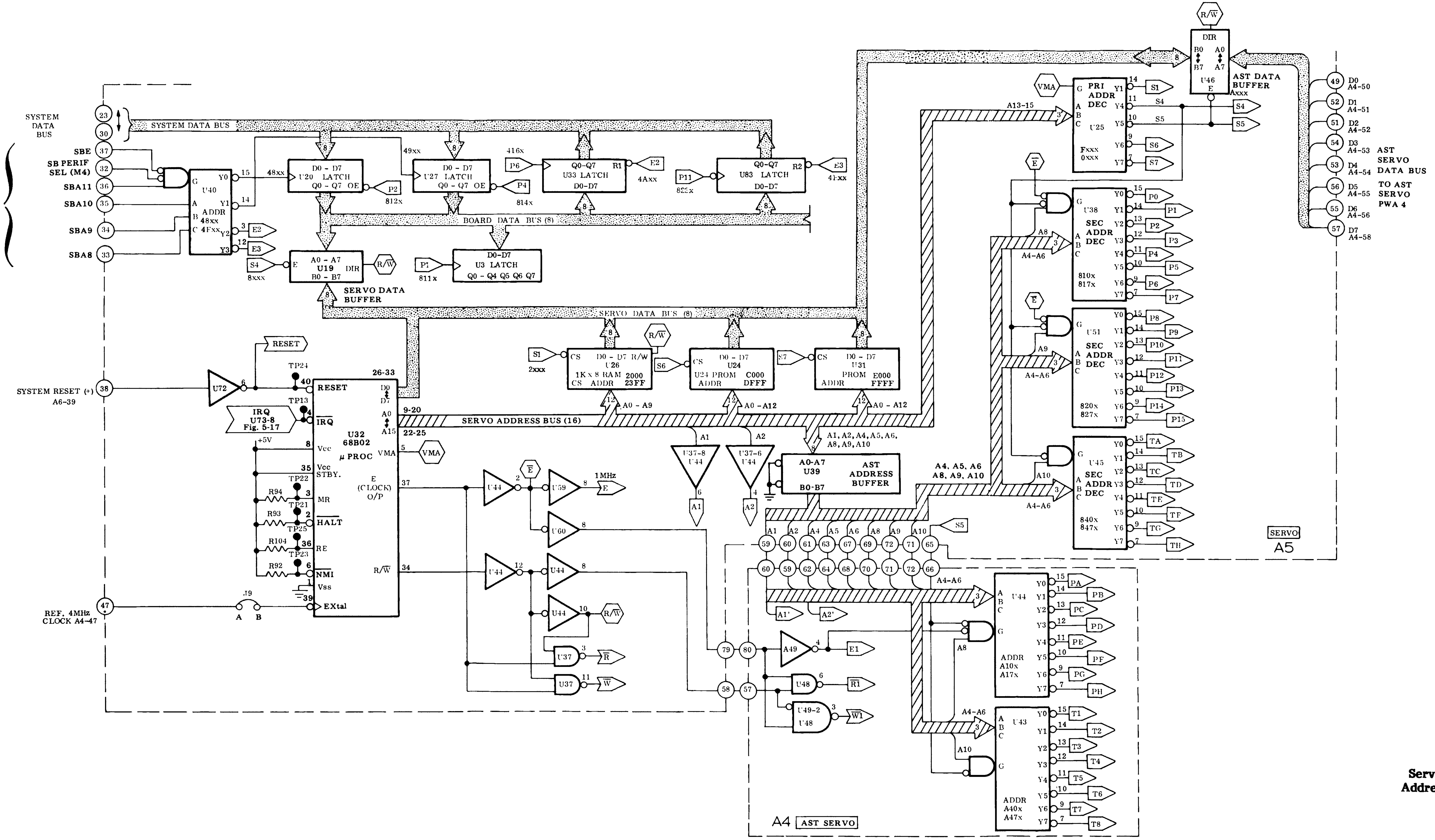


Figure 5-1.
Servo System Kernel and Address Decoding—PWA 5

5-14 Microprocessor

Microprocessor (CPU) chip 5U32 is an 8-bit, NMOS processor (Motorola Type MC68B02) with internal clock divider circuit and 128 bytes of internal RAM storage. Unlike the control system CPU, internal RAM storage is *not* protected by battery backup. The address bus output presents 16 address bits in parallel and is thus capable of accessing 64K of memory. Characteristics of each of the CPU I/O signals are described in detail on the CPU data sheet which is included in Appendix A of the *VPR-80 Parts Lists and Schematics* manual. The BA (bus available), xtal (crystal), halt, and NMI (nonmaskable interrupt) input connections are not used in this application.

5-15 Power, Clock, and Reset Inputs. Regulated and filtered +5V supply is applied at 5U32 Vcc input pin 8. It is also applied to MR (memory ready) input pin 3. The MR input must be held high to insure the nominal 1-MHz frequency of the E (enable) output at pin 37. Regulated +5V is also applied to Vcc standby input pin 35.

The reference generator on the AST Servo PWA supplies a nominal 4-MHz clock to 5U32 EXtal input pin 39. The EXtal clock input is derived from a phase-locked VCO which is locked to the incoming reference signal. The EXtal clock frequency is 256 X H. The CPU internal divide-by-four circuit provides the nominal 1-MHz clock for the CPU and the E (enable) output.

The servo system CPU is reset by the system reset signal from the control system CPU. System reset can be activated in four ways: power-up reset, watchdog timeout, manual reset, and decay of the +5V supply. Reset input pin 40 is held high during normal CPU operation. See paragraph 6-10, Part II for details on the generation of system reset.

5-16 E, VMA, and R/W Outputs. The E (enable) output at pin 37, which is a nominal 1-MHz, TTL-compatible clock signal, is derived from the 4-MHz (256 x H) external clock input to the CPU. E gates the read and write outputs of the CPU. E also clocks programmable interval timers (PITs) 5U77 and 5U49 in the scanner servo and 5U23 and 5U36 in the capstan servo. Inverted E gates outputs of address decoders 5U38 and 5U51. The period of the E output is 993 nanoseconds for 525-line standard or 1 µs for 625-line standard.

The VMA (valid memory address) output at CPU pin 5 is the validating strobe to address decoder 5U25. Decoder 5U25 examines address bits A13-A15, and provides enabling outputs to EPROMs 5U24 and 5U31, RAM 5U26, servo data buffer 5U19, and AST data buffer 5U46. When the CPU accesses other components of the Servo PWA, decoder 5U25 asserts peripheral select signal S4. The S4 output of decoder 5U25 is applied to decoders 5U38, 5U51, and 5U45 as the validating strobe. When the CPU accesses components on the AST Servo PWA, decoder 5U25 asserts peripheral select signal S5. The S5 output of decoder 5U25 is applied to decoders 4U44 and 4U43 as the validating strobe.

The R/W (read/write) output at CPU pin 34 is placed on the servo address/control bus in both normal (high = read/low = write) and inverted form (low = read/high = write). These outputs tell the memory chips whether the CPU is in a read or write state. R/W is also used to control bidirectional data buffers.

5-17 Data Bus

Pins 26 through 33 of the CPU are the 8-bit (D0--D7) data bus port. The data bus is bidirectional. It transfers data and commands from the CPU to the rest of the servo system on a write cycle. It transfers status information and instructions from the control system to the servo CPU on a read cycle. Data bus pins on the CPU are the inputs and outputs of bidirectional tristate buffers. Details of the data bus structure are given in paragraph 5-23.

5-18 Address Bus

Pins 9 through 20 and 22 through 25 of the CPU are the 16-bit (A0--A15) address bus port. Unidirectional address bus outputs are routed to address decoder 5U25, EPROMs 5U24 and 5U31, RAM 5U26, and AST address buffer 5U39. Details of the address bus structure are given in paragraph 5-28.

5-19 Memory

The servo system kernel contains two EPROM chips and one RAM chip. The EPROMs each have the capacity to contain 8K bytes of information, thus providing a total storage capacity of 16K x 8. The low active PRGM (program enable) inputs at pin 27 are pulled up to +5 volts, and are thereby disabled. The contents of EPROMs 5U24 and 5U31 are selectively accessed by the S6 and S7 outputs of address decoder 5U25, which are applied in parallel to the low active CE (chip enable) and OE (output enable) inputs at pins 20 and 22.

RAM 5U26 provides temporary storage for 1024 bytes of information, such as machine status, servo status, and servo commands. RAM 5U26 is accessed by the S1 output of address decoder 5U25 and the R/W (high = read/low = write) output of CPU 5U32. The contents of RAM 5U26 are *not* protected by battery backup.

5-20 Address Decoding

As shown in Figure 5-1, system address/control bus bits SBA8—11, SBE, and SB PERIF SEL are routed to address decoder 5U40. When the control system CPU accesses the servo system, SBA11 (high) and low active SB PERIF SEL (M4) enable decoder 5U40 which sorts out address bits SB8—10. Thus, 5U40 is a secondary decoder on the system address bus. Its four outputs are E0—E3. E0 and E1 clock input data latches 5U20 and 5U27; E2 and E3 clock output data latches 5U33 and 5U83. These data latches, which are controlled by the control system CPU, gate information between the control system CPU and the servo system CPU via the system data bus.

Address decoding within the servo system is also accomplished at two levels. High-order address bits are decoded to derive a chip select, output enable, or clock (load enable) output to the addressed chip. Low-order address bits define the specific address within that chip.

For example, when accessing a memory chip, high-order address bits enable the chip output, and low-order address bits access the specific address within the chip. If the addressed chip is an input buffer, where all bits present at the buffer inputs are to be gated as one word, low-order address bits are irrelevant.

5-21 Memory Map

The servo system memory map is shown in simplified form in Figure 5-2. Design of the memory map is straightforward. Generally, all addresses are expressed in hexadecimal (hex) notation. (Figure 5-2 shows both hex and decimal notation.) Where less than four hex digits are used, as in Figure 5-1, lower-order digits (on the right) are irrelevant, or in "don't care" states, designated by X.

As seen in Figure 5-2, addresses 0000—007F are dedicated to the CPU internal RAM, or scratchpad memory. Addresses for accessing contents of RAM 5U26 are contained in address block 2000—23FF. This block of addresses is enabled by S1 from primary decoder 5U25.

Addresses for accessing Servo PWA I/O ports and programmable interval timers (PITs) are contained in address block 8000—84FF. Addresses in this block are enabled by P0—P15 from secondary address decoders 5U38 and 5U51 and by TA—TH from secondary address decoder 5U45.

Addresses for accessing AST Servo PWA I/O ports and programmable interval timers (PITs) are contained in address block A000—A4FF. Addresses in this block are enabled by PA--PH from secondary address decoder 4U44 and by T0—T7 from secondary address decoder 4U43.

Addresses for accessing the contents of EPROM 5U24 are contained in address block C000—DFFF. This block of addresses is enabled by S6 from primary decoder 5U25.

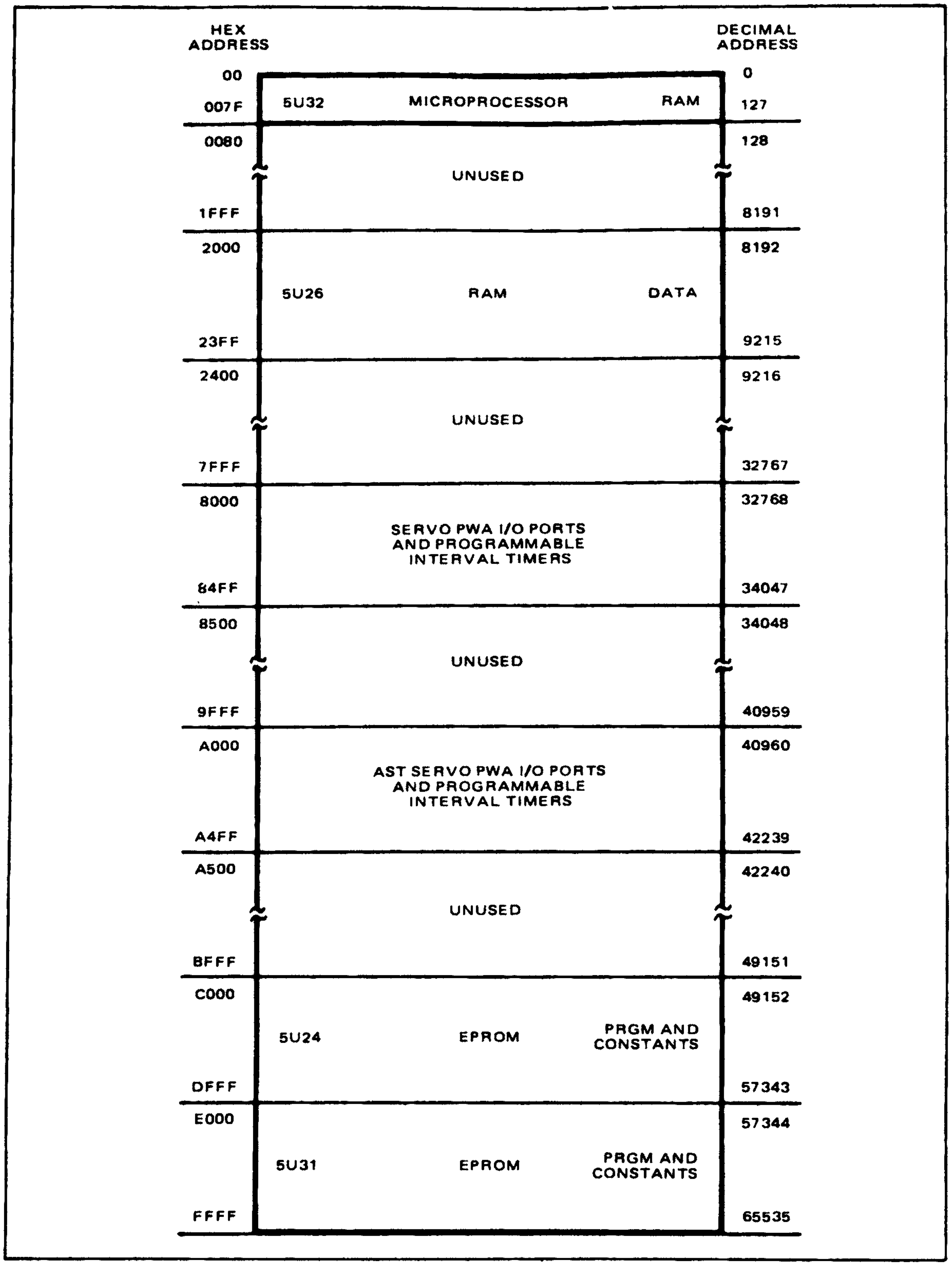
Addresses for accessing the contents of EPROM 5U31 are contained in address block E000—FFFF. This block of addresses is enabled by S7 from primary decoder 5U25.

5-22 Address Decoders

Primary decoder 5U25 takes the three highest-order address bits (A13—A15) and divides the entire address range into eight parts. Of the eight, only five parts (S1, S4, S5, S6, and S7) are used. Three of these outputs (S1, S6, and S7) are used directly with no further decoding to enable the two EPROMs and RAM 5U26.

The S4 output of primary decoder 5U25 enables servo data buffer 5U19. Thus, data transfer between the servo CPU data bus and the rest of the Servo PWA is enabled. Direction of data transfer is governed by the state of the R/W output of CPU 5U32. S4 and address bit A8 enable secondary decoder 5U38 to which address bits A4—A6 are applied. 5U38 decodes S4, A8, and A4—A6 to produce 1 of 8 port selection enabling outputs, P0—P7.

Similarly, S4 and address bit A9 enable secondary decoder 5U51 to which address bits A4—A6 are applied. 5U51 decodes S4, A9, and A4—A6 to produce 1 of 8 additional port selection enabling outputs, P8—P15.



HEX ADDRESS				DECIMAL ADDRESS
00 – 007F	5U32	MICROPROCESSOR	RAM	0 – 127
0080 – 1FFF		UNUSED		128 – 8191
2000 – 23FF	5U26	RAM	DATA	8192 – 9215
2400 – 7FFF		UNUSED		9216 – 32767
8000 – 84FF		SERVO PWA I/O PORTS AND PROGRAMMABLE INTERVAL TIMERS		32768 – 34047
8500 – 9FFF		UNUSED		34048 – 40959
A000 – A4FF		AST SERVO PWA I/O PORTS AND PROGRAMMABLE INTERVAL TIMERS		40960 – 42239
A500 – BFFF		UNUSED		42240 – 49151
C000 – DFFF	5U24	EPROM	PRGM AND CONSTANTS	49152 – 57343
E000 – FFFF	5U31	EPROM	PRGM AND CONSTANTS	57344 – 65535

Figure 5-2. Simplified Servo System Memory Map

S4 and address bit A10 enable secondary decoder 5U45 to which address bits A4--A6 are applied. 5U45 decodes S4, A10, and A4--A6 to produce 1 of 7 timer selection enabling outputs, TA--TG.

The S5 output of primary decoder 5U25 enables AST data buffer 5U46. Thus, data transfer between the Servo PWA data bus and the AST Servo PWA data bus is enabled. The direction of data transfer is governed by the state of the R/W output of CPU 5U32. S5 and address bit A8 enable secondary decoder 4U44 to which address bits A4—A6 are applied. 4U44 decodes S5, A8, and A4—A6 to produce 1 of 7 AST servo port selection enabling outputs, PA—PG.

Similarly, S5 and address bit A10 enable secondary decoder 4U43 to which address bits A4—A6 are applied. 4U43 decodes S5, A10, and A4—A6 to produce one of eight AST servo timer selection enabling outputs, T1—T8.

Destinations of Servo PWA secondary address decoder outputs P0—P15 and TA—TG and destinations of AST Servo PWA secondary address decoder outputs PA—PG and T1—T8 are listed in Table 5-1.

Table 5-1 lists I/O addresses in ascending order. The table shows address mnemonics used on schematic diagrams and lists point of origin for each decoded address. The Remarks column of Table 5-1 lists outputs of the accessed devices. Input = input to the CPU. Output = output from the CPU. In addition, the following abbreviations are used in the Remarks column to conserve space:

Table 5-1. Servo System Memory Map

Address	Mnemonic	Source	Remarks
0000–007F	----	CPU 5U32	Scratchpad memory addresses (internal to 5U32).
2000–23FF	S1	PAD 5U25-14	Chip and output enables to RAM 5U26.
810X	P0	SAD 5U38-15	Enables IDB 5U9 and commands ADC 5U8 to present digitized analog values to IDB 5U9.
811X	P1	SAD 5U38-14	Clocks ODL 5U3. 4-bit output of 5U3 enables MUX 5U2 and selects 1 of 8 analog inputs.
812X	P2	SAD 5U38-13	Enables IDB 5U20. Connects information from system data bus to Servo PWA data bus. Data clocked by E0.
813X	P3	SAD 5U38-12	Enables IDB 5U18. Indicator DS1 status gated to Servo PWA data bus.
814X	P4	SAD 5U38-11	Enables IDB 5U27. Connects information from system data bus to Servo PWA data bus. Data clocked by E1.

(Continued next page)

Table 5-1. Servo System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
815X	P5	SAD 5U38-10	Clocks ODL 5U78. Control information gated from Servo PWA data bus to capstan and scanner servos.
816X	P6	SAD 5U38-9	Clocks ODL 5U33. Data gated from Servo PWA data bus to system data bus. Chip enabled by E2
817X	P7	SAD 5U38-7	Enables IDB 5U69. Control track information and interrupt flags gated to Servo PWA data bus.
820X	P8	SAD 5U51-15	Enables SPIB 5U17. Scanner phase DIP switch information gated to Servo PWA data bus
821X	P9	SAD 5U51-14	Enables DAC 5U4. Scanner position (phase) error data gated from Servo PWA data bus and converted to analog voltage for scanner MDA.
822X	P10	SAD 5U51-13	Enables DAC 5U10. Scanner velocity error data gated from Servo PWA data bus and converted to analog voltage for scanner MDA.
823X	P11	SAD 5U51-12	Clocks ODL 5U83. Data gated from Servo PWA data bus to system data bus. Chip enabled by E3.
824X	P12	SAD 5U51-11	Enables DAC 5U11. Takeup reel error data gated from Servo PWA data bus and converted to analog voltage for takeup reel MDA.
825X	P13	SAD 5U51-10	Enables DAC 5U5. Supply reel error data gated from Servo PWA data bus and converted to analog voltage for supply reel MDA.
826X	P14	SAD 5U51-9	Enables IDB 5U76. Reel servo status (tape direction) gated to Servo PWA data bus.
827X	P15	SAD 5U51-7	Ensures clock input to takeup reel TSC 5U63 once per field.
8400–8407	TA	SAD 5U45-15	Enables PIT 5U36: control track flag sample gate, timing counter, and half-ramp delay.
8410–8417	TB	SAD 5U45-14	Enables PIT 5U23: capstan tracking one-shot, inner loop reference, and control track noise eliminator one-shot.

(Continued next page)

Table 5-1. Servo System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
8420–8427	TC	SAD 5U45-13	Enables PIT 5U77: scanner tach delay one-shot, velocity ramp generator, and AST IRQ.
8430–8437	TD	SAD 5U45-12	Enables PIT 5U49: scanner vertical phase one-shot, phase ramp generator, and phase error counter.
8440–8447	TE	SAD 5U45-11	Enables PIT 5U56: reel servo tape tach divider and tape speed counters.
8450–8457	TF	SAD 5U45-10	Enables PIT 5U36: takeup reel servo diameter counters and takeup reel speed counter.
8460–8467	TG	SAD 5U45-9	Enables PIT 5U70: supply reel servo diameter counters and supply reel speed counter.
A10X	PA	SAD 4U44-15	Clocks ODL 4U37: AST control data.
A11X	PB	SAD 4U44-14	Clocks ODL 4U38: TBC control data.
A12X	PC	SAD 4U44-13	Clocks IDL 4U55: AST ramp data.
A13X	PD	SAD 4U44-12	Enables IDB 4U36: AST status data.
A14X	PE	SAD 4U44-11	Enables IDB 4U10: AST track jump timing switch (4S1) data.
A15X	PF	SAD 4U44-10	Enables DAC 4U2: AST ac error.
A16X	PG	SAD 4U44-9	Loads ASTRG 4U52/4U57.
A400–A407	T1	SAD 4U43-15	Enables PIT 4U23: reference generator vertical one-shot, vertical counter, and reference present one-shot.
A410–A417	T2	SAD 4U43-14	Enables PIT 4U35: reference generator H/2 eliminator and divide-by-4 clock.
A420–A427	T3	SAD 4U43-13	Enables PIT 4U16: tape vertical processor noise eliminator one-shot, one-field delay one-shot, and pulse forming one-shot.
A430–A437	T4	SAD 4U43-12	Enables PIT 4U41: tape vertical generator vertical pulse one-shot, variable delay one-shot, and blanking pulse generator.
A440–A447	T5	SAD 4U43-11	Enables PIT 4U11: tape sync processor one-shots.
A450–A457	T6	SAD 4U43-10	Enables PIT 4U3: track jump timing one-shot, scanner tach delay one-shot, and tape H generator.

(Continued next page)

Table 5-1. Servo System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
A460–A467	T7	SAD 4U43-9	Enables PIT 4U47: null test frequency generator, dither frequency generator, and dither phase delay generator.
A470–A477	T8	SAD 4U43-7	Enables PIT 4U56: AST ramp reference generator, track jump one-shot, and speed control AST ramp reference generator.
C000–DFFF	S6	PAD 5U25-9	Chip and output enables to EPROM 5U24.
E000–FFFF	S7	PAD 5U25-87	Chip and output enables to EPROM 5U31.

ADC	Analog-to-Digital Converter
ASTAB	AST Address Buffer
ASTDB	AST Data Buffer
ASTRG	AST Ramp Generator
CPU	Central Processor Unit
DAC	Digital-to-Analog Converter
IDB	Input Data Buffer
IDL	Input Data Latch
MUX	Multiplexer
ODL	Output Data Latch
PAD	Primary Address Decoder
PIT	Programmable Interval Timer
SAB	Servo Address Buffer
SAD	Secondary Address Decoder
SDB	Servo Data Buffer
SPIB	Scanner Phase Input Buffer
TSC	Tape Speed Counter

5-23 Data Bus Structure

The servo system data bus structure is composed of three major segments plus the portion of the system data bus which is internal to the Servo PWA. The three major segments of the data bus are:

- Servo CPU data bus
- Servo PWA data bus
- AST Servo PWA data bus

5-24 System Data Bus

The system data bus (SBD0--SBD7) enters the Servo PWA at PWA-edge contacts 23 through 30 and is applied to I/O data buffers 5U83, 5U20, 5U27, and 5U33. Data buffers provide the path for bidirectional data transfers between the system data bus and the Servo PWA data bus. Buffers 5U20 and 5U27 are input buffers which are enabled by E0 and E1 from address decoder 5U40. Buffers 5U33 and 5U83 are output buffers which are enabled by E2 and E3 from address decoder 5U40.

5-25 Servo CPU Data Bus

The servo CPU data bus is the 8-bit bidirectional path between servo CPU 5U32, EPROMs 5U24 and 5U31, and RAM 5U26. The servo CPU data bus is linked to the Servo PWA data bus via servo data buffer 5U19, which is enabled by S4 from primary address decoder 5U25. The servo CPU data bus is linked to the AST Servo PWA data bus via AST data buffer 5U46, which is enabled by S5 from primary address decoder 5U25.

5-26 Servo PWA Data Bus

The servo PWA data bus is the 8-bit bidirectional path between the I/O buffers (paragraph 5-21), servo data buffer 5U19, and the Servo PWA I/O ports and programmable interval timers (PITs). The Servo PWA data bus is linked to the servo CPU data bus via servo data buffer 5U19, which is enabled by S4 from primary address decoder 5U25. The Servo PWA data bus is linked to the system data bus via I/O buffers 5U83, 5U20, 5U27, and 5U33 (enabled by E0--E3 from system address decoder 5U40).

5-27 AST Servo PWA Data Bus

The AST Servo PWA data bus is the 8-bit bidirectional path between the AST Servo PWA I/O ports and PITs and the servo CPU via AST data buffer 5U46 and the servo CPU data bus. AST data buffer 5U46 is enabled by S5 from primary address decoder 5U25.

5-28 Address/Control Bus Structure

The servo system address/control bus structure is composed of three major segments plus the portion of the system address/control bus which is internal to the Servo PWA. The three major segments of the address/control bus are:

- Servo CPU address/control bus
- Servo PWA address/control bus
- AST Servo PWA address/control bus

5-29 System Address/Control Bus

The system address/control bus (SBA8—SBA11, SBE, and SB PERIF SEL) enters the Servo PWA at PWA-edge contacts 32 through 37 and is applied to address decoder 5U40. The four decoded outputs of 5U40, E0—E3, enable I/O data buffers 5U83, 5U20, 5U27, and 5U33 which link the system data bus to the Servo PWA data bus.

5-30 Servo CPU Address/Control Bus

The servo CPU address/control bus (A0—A15) is the 16-bit path for address information from servo CPU 5U32 to EPROMs 5U24 and 5U31 and to RAM 5U26. Address bits A13—A15 (and VMA) are broken out of the servo CPU address/control bus and presented to primary address decoder 5U25 which produces S1 and S4—S7. Address bits A1 and A2 are also broken out of the bus and applied to the internal address decoders in each of the six PIT chips on the Servo PWA. The PIT internal decoders select which of the three counters in each PIT is to be accessed. Bits A1, A2, A4—A6, and A8—A10 are also presented to AST address buffer 5U39.

5-31 Servo PWA Address/Control Bus

The Servo PWA address/control bus (A4—A6 and A8—A10) is the 6-bit path for address information between AST address buffer 5U39 and secondary address decoders 5U45, 5U38 and 5U51. Buffer 5U39 is permanently enabled. Its parallel outputs to the Servo PWA address/control bus and the AST Servo PWA address/control bus are differentiated by the assertion of S4 which enables secondary address decoders 5U45, 5U38, and 5U51.

5-32 AST Servo PWA Address/Control Bus

The AST Servo PWA address/control bus (A1, A2, A4—A6, and A8—A10) exits the Servo PWA at the outputs of AST address buffer 5U39. Address bits A4—A6 are decoded (with A8) by secondary address decoder 4U44 on the AST Servo PWA. Bits A4—A6 (with A10) are decoded by secondary decoder 4U43. Decoders 4U44 and 4U43 are enabled by S5 from primary address decoder 5U25. Address bit A9 is not used. Address bits A1 and A2 are also broken out of the bus and applied to internal address decoders in each of the eight PIT chips on the AST Servo PWA. PIT internal decoders select which of the three counters in each PIT is to be accessed.

5-33 Jumpers

There are no jumpers on either the AST Servo or the AST Driver PWAs. The Servo PWA is equipped with jumpers as aids to testing and troubleshooting the servo circuits. Although reference designations J1 through J11 are assigned, the J10 designation is assigned to the accessory diagnostic probe connector. Functions of J1 through J9 and J11 are listed in Table 5-2. Jumper locations are shown in Figure 5-68 at the end of this section.

Table 5-2. Servo PWA Jumpers

Jumper	Position	Function
J1	A-B	Normal.
	Removed	Disconnects control track phase error output.
J2	A-B	Normal.
	Removed	Disconnects input to A/D converter 5U8 for test.
J3	A-B	Normal.
	Removed	Permits use of test voltage input to analog multiplexer 5U2 and A/D converter 5U8.

(Continued next page)

Table 5-2. Servo PWA Jumpers (Continued)

Jumper	Position	Function
J4	A-B	Normal.
	Removed	Disconnects scanner analog velocity (speed) error (for manufacturing test only).
J5	A-B	Normal.
	Removed	Disconnects scanner analog position (phase) error (for manufacturing test only).
J6	A-B	Normal.
	Removed	Disconnects supply reel motor analog error output to reel MDA. See paragraph 7-30 in Section 7
J7	A-B	Normal.
	Removed	Disconnects takeup reel motor analog error output to reel MDA. See paragraph 7-30 in Section 7.
J8	A-B	Normal.
	Removed	Disconnects capstan motor analog error output to capstan MDA.
J9	A-B	Normal.
	Removed	Disconnects 4-MHz (256H) clock input to servo CPU 5U32.
J11	A-B	Normal.
	Removed	Disconnects output of up/down counter analog voltage from output for test.

5-34 Initialization Routine

Servo system CPU 5U32 begins the initialization routine when the control system CPU asserts and then releases system reset. As explained in Section 6 (paragraph 6-10), system reset results from any one of four causes: power-up reset, control system watchdog timeout, manual reset, or power-down reset (decay of +5V supply). The active system reset line keeps the servo system CPU in reset condition. In addition, audio and video recording is inhibited, motor drive amplifiers (MDAs) are inhibited, reel brakes are applied, and the capstan pinch roller is disengaged.

After making initialization tests of its own RAM storage, the control system CPU releases the system reset line. At that time, servo CPU 5U32 begins servo system initialization which is charted in Figure 5-3. The CPU sees the entire servo system as one set of peripherals, regardless of whether components are part of the Servo or AST Servo PWAs.

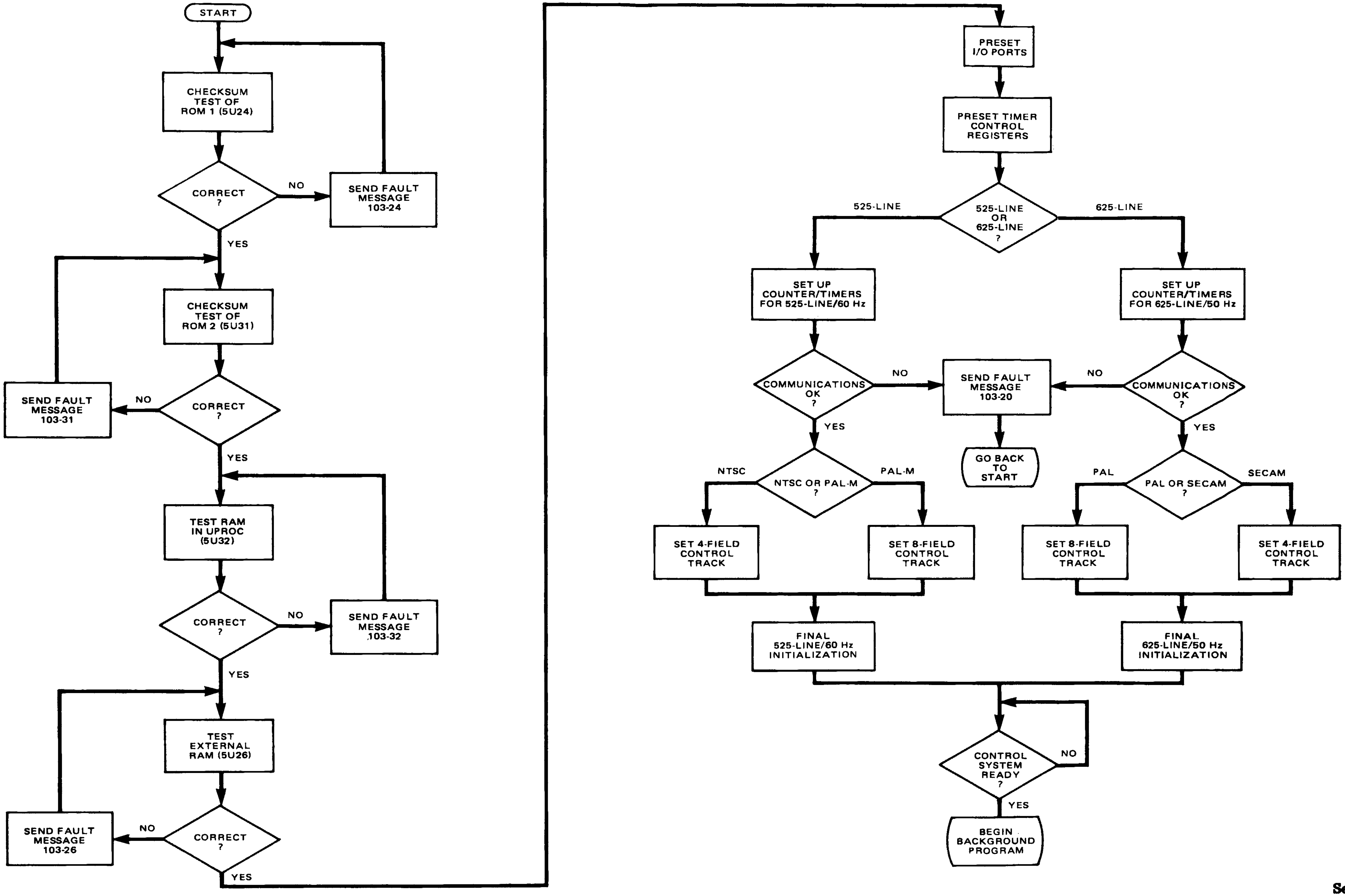

START
CHECKSUM TEST OF ROM 1 (5U24)
CORRECT ?
NO
SEND FAULT MESSAGE 103-24
YES
CHECKSUM TEST OF ROM 2 (5U31)
CORRECT ?
NO
SEND FAULT MESSAGE 103-31
YES
TEST RAM IN UPROC (5U32)
CORRECT ?
NO
SEND FAULT MESSAGE 103-32
YES
TEST EXTERNAL RAM (5U26)
CORRECT ?
NO
SEND FAULT MESSAGE 103-26
YES
PRESET I/O PORTS
PRESET TIMER CONTROL REGISTERS
525-LINE OR 625-LINE ?
525-LINE
625-LINE
SET UP COUNTER/TIMERS FOR 525-LINE/60 Hz
SET UP COUNTER/TIMERS FOR 625-LINE/50 Hz
COMMUNICATIONS OK ?
NO
SEND FAULT MESSAGE 103-20
NO
COMMUNICATIONS OK ?
YES
GO BACK TO START
YES
NTSC
NTSC OR PAL-M ?
PAL-M
PAL
PAL OR SECAM ?
SECAM
SET 4-FIELD CONTROL TRACK
SET 8-FIELD CONTROL TRACK
SET 8-FIELD CONTROL TRACK
SET 4-FIELD CONTROL TRACK
FINAL 525-LINE/60 Hz INITIALIZATION
FINAL 625-LINE/50 Hz INITIALIZATION
CONTROL SYSTEM READY ?
NO
YES
BEGIN BACKGROUND PROGRAM

Figure 5-3.
Servo System
Initialization Routine

Servo CPU 5U32 first tests ROMs 1 and 2 (5U24 and 5U31). It then tests its internal RAM storage and then RAM 5U26. If any of these tests are failed, the CPU continues to loop on the test of the failed memory and the appropriate fault message is sent to the control system for display. Therefore, if looping on the test of ROM 1 occurs (and fault message **103-24** is sent), the CPU has not yet tested the other memory modules or proceeded to the balance of the initialization routine.

Following memory tests, the CPU presets servo system I/O ports. It accesses the programmable interval timers (PITs) and establishes the operating mode of each PIT chip. Next, the CPU presets timer control registers by placing the appropriate initial value in each register. At this point the CPU looks at the 525/625 logic level on the Reference PWA in order to select values which differ between 525- and 625-line systems. Appropriate values are then preset in the PIT timers and counters.

Servo CPU 5U32 then ascertains that the control system send message has been received. If this communications check is failed, indicating a fault in the control system CPU sender or the servo system CPU receiver, fault message **103-20** is sent to the control system for display. The servo CPU will continue to loop on this test, and the initialization routine will not be completed.

The CPU then looks at the previously received message for configuration information. This differentiates between NTSC and PAL-M for 525-line systems, or between PAL and SECAM for 625-line systems. Based on this information, the presetting of initial values in timers and counters is completed.

In one final step, the servo CPU completes the initialization routine. Once a signal has been received from the control system CPU, indicating that it has completed its own initialization routine, the VPR-80 wakes up in stop mode/standby condition, and the servo CPU enters its background routine.

5-35 Background Routine

The background, or main, routine is a sophisticated program which involves interaction of the control system and servo system CPUs. As far as the servo system CPU is concerned, the background routine is composed of eleven independent modules (shown in Figure 5-4) which correspond to primary modes of operation.

The VPR-80 can be commanded directly to exit any current mode and enter any other mode. Recognition and interpretation of a mode change command are done by the control system CPU. When the operator manually enters a command by switch closure, execution of the command is almost entirely in the firmware domain. Control system mode control logic (firmware) cannot issue commands to the audio, video, servo, or transport systems without regard for the current status of each of the other systems. The mode change request is processed by the control system CPU, and all necessary control system outputs are issued under qualifying statements (flags) from the transport and servo systems.

For example, assume that an entrance edit point (cue) is in reverse tape direction, and the CUE switch is pressed while the transport is in full speed forward shuttle

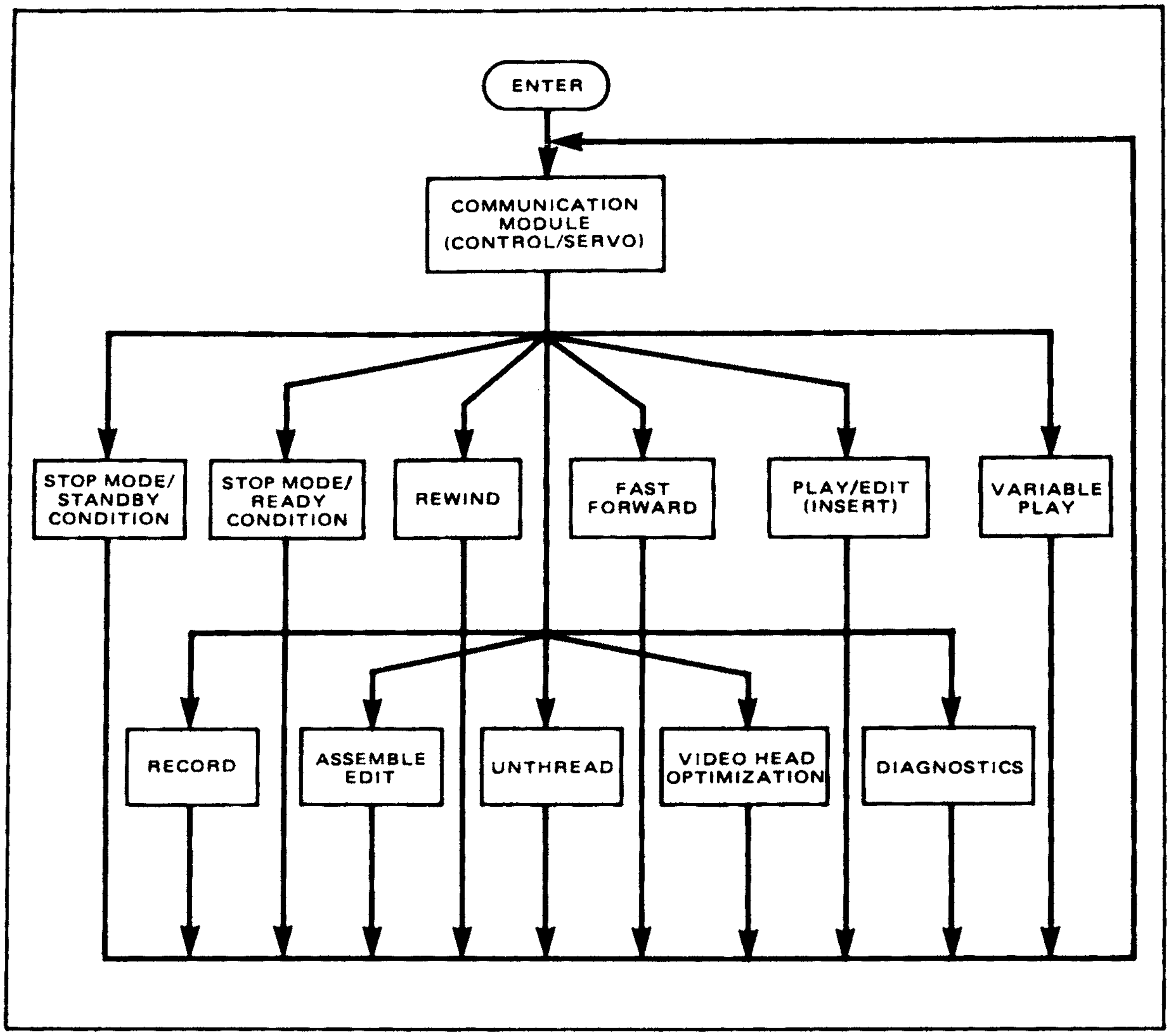


Figure 5-4. Servo System Background Routine

mode. The only hardware changes that are affected immediately are those of turning off the SHUTTLE indicator, turning on the CUE indicator, and removing the effectiveness of the tape speed (shuttle) control knob. Cue mode obviously cannot be entered immediately. The cue mode command must be qualified until shuttle mode can be exited. Firmware logic looks at tape time and direction (tape timer tach) and the relative position of the cue. Forward tape motion must be decelerated to a stop and then started in reverse direction in search of the cue. The shuttle command is not actually terminated and the cue command is not actually initiated by the control system mode control logic until tape comes to a stop. Thus, the cue command is qualified by information from the servo system before its execution can be effected.

When changing from any one of the eleven background modules to another, or at any time that communications with the control system is necessary, all communication is done in the control/servo communication module.

Servo diagnostic tests listed below are also done during all background subroutines. Tests of ROM storage and verification of the control system send message, which are accomplished during the initialization routine, are repeated during background routine.

Servo lock status **(SYSTEM 06)**
Control track lock **(SYSTEM 07)**
Field match/mismatch **(SYSTEM 08)**
Color frame **(SYSTEM 09)**
Edit phase range **(SYSTEM 10)**
Scanner stall **(SYSTEM 11)**
Edit optimize **(SYSTEM 15)**
Tension arm position **(FAULT 103-01)**
Communications with Control PWA (send) **(FAULT 103-20)**
ROM 1 (5U24) **(FAULT 103-24)**
ROM 2 (5U31) **(FAULT 103-31)**
Capstan runaway **(FAULT 103-50)**
Scanner tach **(FAULT 103-73)**

The module in Figure 5-4 designated DIAGNOSTIC is entered when the diagnostic probe accessory is installed in the Control PWA and ports on the Servo or AST Servo PWAs are tested.

5-36 Foreground Routine (Interrupts)

At scanner sync speed, interrupts to the servo system CPU are not prioritized. All interrupts are weighted equally. There are three interrupts:.

- Scanner interrupt: occurs once per scanner revolution
- Delayed scanner interrupt: occurs 128 microseconds after scanner interrupt
- AST interrupt: occurs once per half cycle of AST dither

Scanner and delayed scanner interrupts are derived from the once-around scanner tach, and occur at vertical rate (60 or 50 Hz). The AST interrupt is asserted by a digital counter. The AST interrupt occurs at a 900-Hz rate for 525-line video, or at a 850-Hz rate for 625-line video. Generation of interrupts is shown in Figure 5-5.

The scanner tach pulse, observed at test point 5TP12, asserts interrupt request (IRQ) to servo system CPU 5U32 through gate 5U73-8. The scanner tach pulse also triggers the 128-us tach delay one-shot, 5U77-10. At the same time, the scanner tach flag bit is asserted to the CPU through input data buffer 5U69-13. The CPU recognizes the interrupt by the assertion of scanner tach flag. The CPU then services the scanner interrupt in three steps:

- It inhibits recognition of AST interrupts (which occur at a much higher frequency),
- it clears the scanner interrupt, and
- it enters wait condition until delayed scanner interrupt is received.

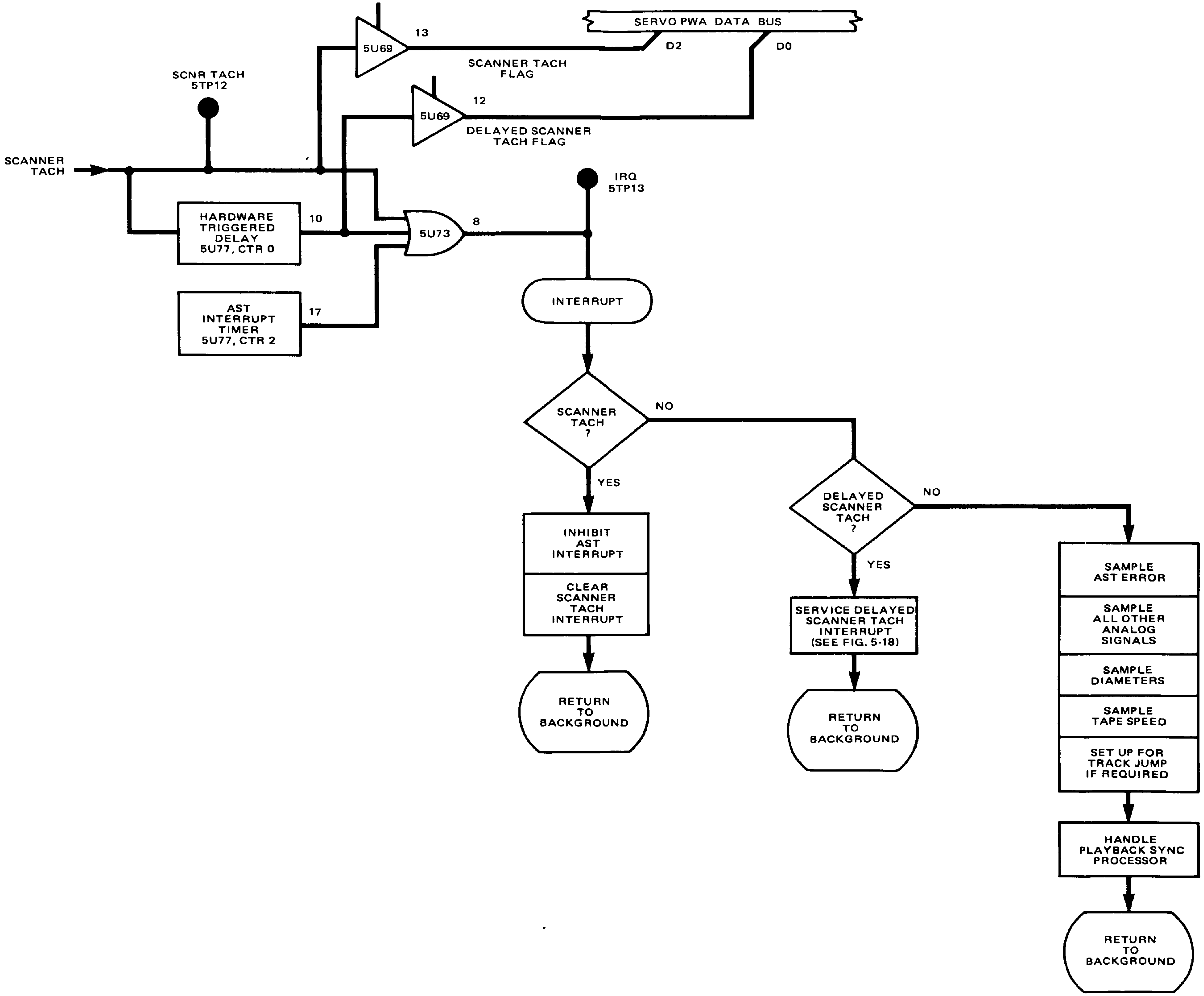


Figure 5-5.
Servo System Foreground Routine (Interrupts)

When digital one-shot 5U77-10 times out (128 µs), it asserts IRQ to the CPU through gate 5U73-8. At the same time, the delayed scanner tach flag is asserted. The CPU thus recognizes delayed scanner interrupt and services it (see paragraph 5-56). The CPU then clears the delayed scanner interrupt and returns to the background program.

AST interrupt is asserted by 5U77-17 which is clocked by E pulses from CPU 5U32. The CPU recognizes the interrupt by the absence of scanner and delayed scanner tach flags. Servicing of AST interrupt is covered in paragraph 5-69. After servicing the AST interrupt, the CPU clears it and returns to the background program.

During scanner run-up interrupts are not synchronous. During run-up, service of an AST interrupt is broken into by occurrence of a scanner interrupt. Once in the scanner interrupt service subroutine, AST interrupts are locked out.

5-37 Reference PWA Circuits

Reference selector circuits on the Reference PWA supply the selected composite sync signal to the reference pulse generator on the AST Servo PWA. Color field 1 identifier circuits on the Reference PWA furnish the color field 1 identification signal to the control track generator on the Servo PWA.

Figures 5-6 (NTSC), 5-7 (PAL-M), and 5-8 (PAL/SECAM) show the reference selector and color field 1 identifier on the Reference PWA. The playback sync processor and the reference pulse generator on the AST Servo PWA are also shown. Data and address/control bus lines between the Servo and AST Servo PWAs are also shown, as are some of the reference pulses furnished to the Servo PWA.

Theory of operation discussions and detailed diagrams of the reference selector and color field 1 identifier are given in Section 3, Part II.

5-38 Reference Pulse Generator

The reference pulse generator furnishes reference vertical and reference frame signals to both the servo and control systems. It also furnishes the reference frame signal back to the Reference PWA, where it is used in the generation of color field 1 reference for the control track logic. The reference pulse generator also furnishes 16H to the audio system for bias and erase frequency generation, 2H to the reel servo, and 256H external clock signal to the servo system CPU.

The reference pulse generator on the AST Servo PWA is shown in Figure 5-9. It is composed of two programmable interval timer (PIT) chips (six individual timers), a digital ramp and sample phase comparator, a voltage-controlled oscillator (VCO), and reference frequency dividers. All of its outputs are synchronized to the selected reference composite sync input. If that input is removed, reference pulse outputs are derived from the VCO without synchronization.

Six individual timers in PIT chips 4U23 and 4U35 are programmed only once during the initialization routine. Some initial values differ between 525- and 625-line standards. PIT 4U23 is enabled by decoded address T1, and PIT 4U35 is enabled by T2.

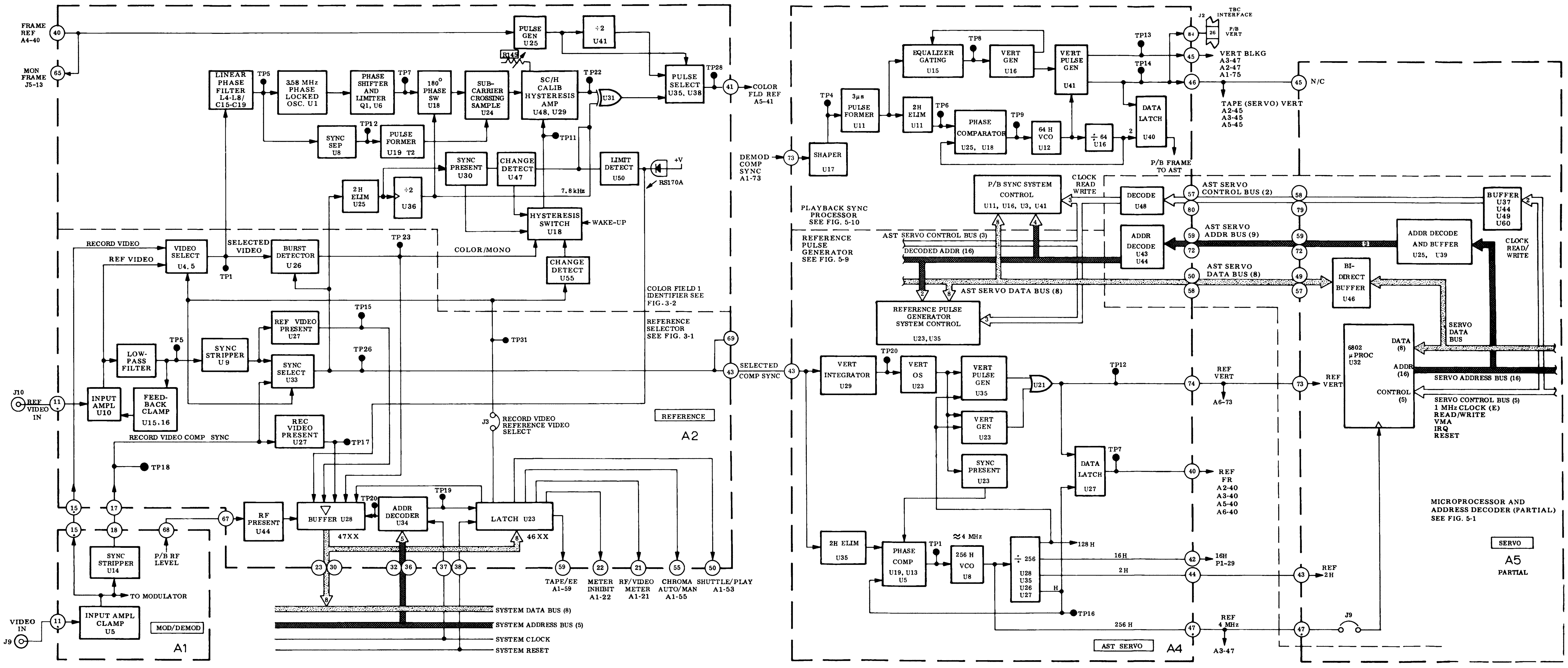


Figure 5-6.
Reference Pulses—PWA 2 (NTSC)

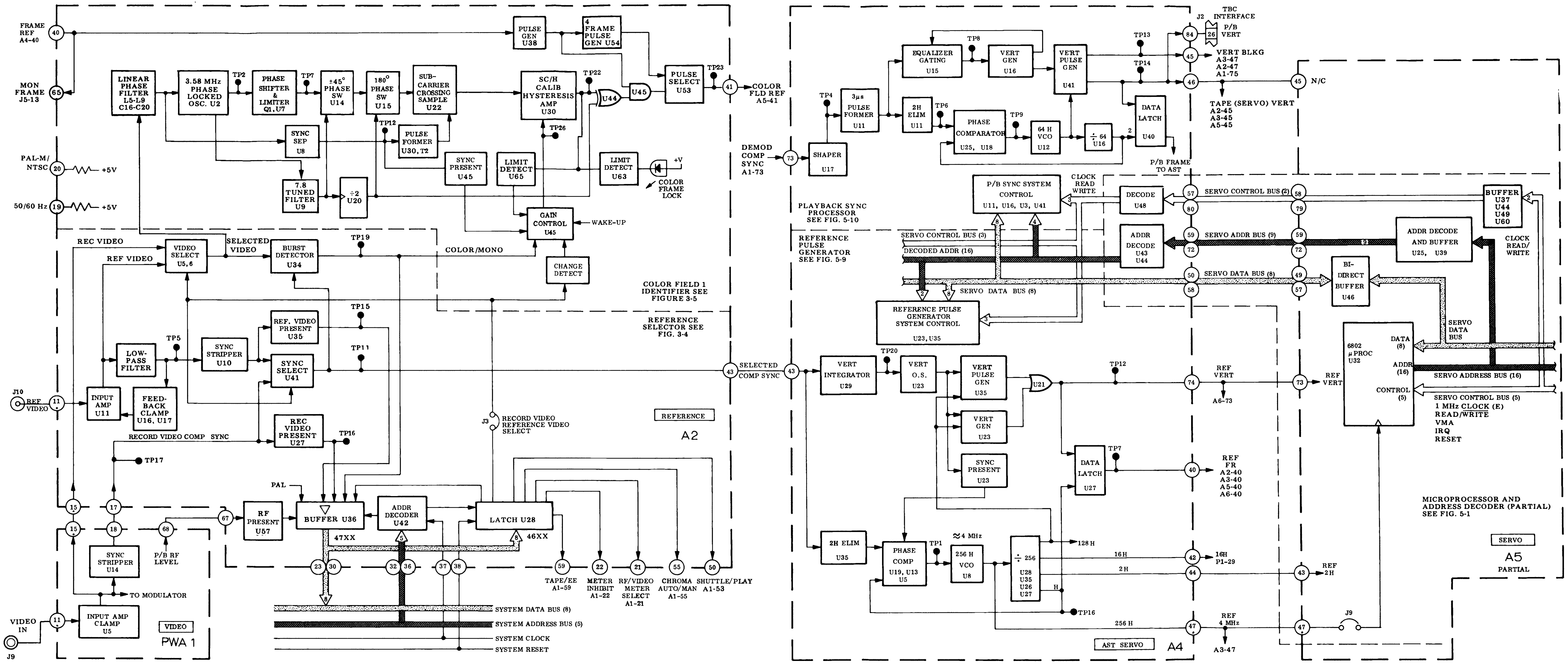


Figure 5-7.
Reference Pulses—PWA 2 (PAL-M)

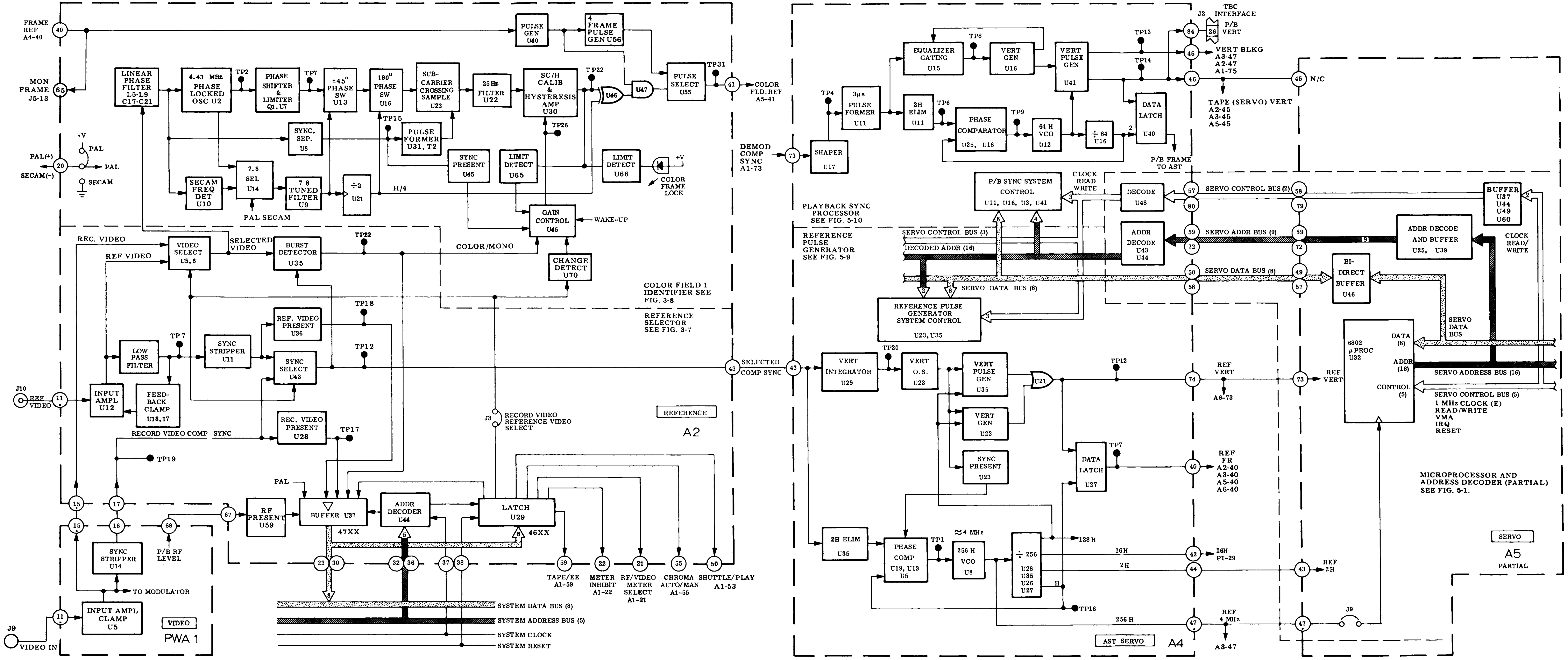


Figure 5-8.
Reference Pulses—PWA 2 (PAL/SECAM)

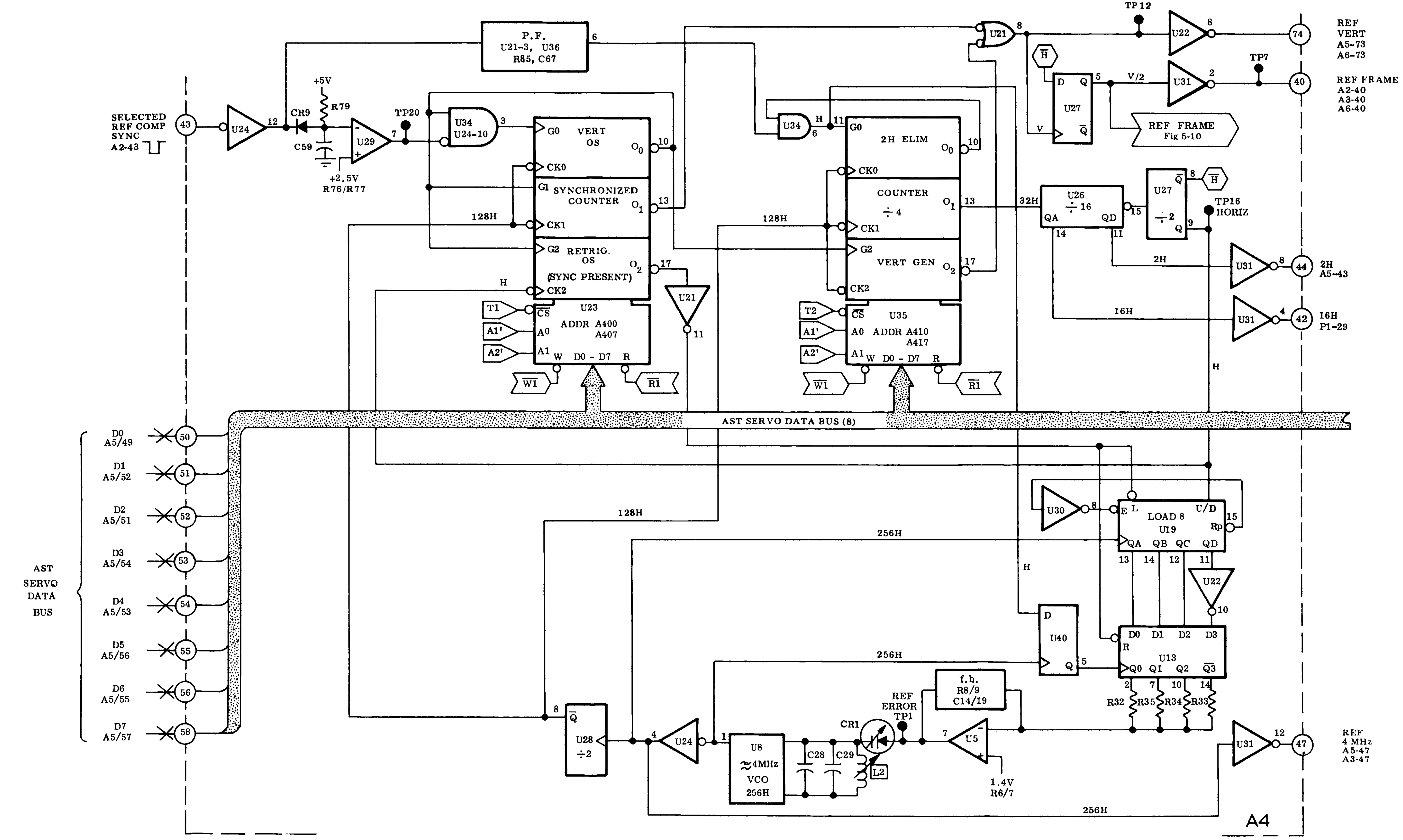


Figure 5-9.
Reference Pulse Generator—PWA 4

The selected reference composite sync input from the reference selector (Reference PWA) enters the AST Servo PWA at connector contact 43. It is applied through two pulse former networks to vertical pulse gate 4U34-3 and horizontal pulse gate 4U34-6.

5-39 Reference Vertical and Frame

Timer 4U23-10 is the vertical one-shot. It is triggered by the vertical interval component of the composite sync, and it is clocked by 128H derived from the VCO. Gate 4U34-3 is enabled in the absence of output from vertical one-shot 4U23-10. The one-shot is triggered by the gate output. Therefore, the feedback arrangement prevents triggering of the vertical one-shot until the next vertical interval. The one-shot acts as a filter by effectively eliminating pulses in the middle of the vertical interval. The filtered V output of 4U23-10 resets counter 4U23-13 and triggers one-shot 4U23-17. It also triggers one-shot 4U35-17.

Counter 4U23-13 is reset by the filtered V output of vertical one-shot 4U23-10, and it is clocked by 128H. This synchronizes counter 4U23-13 with the reference vertical interval. As long as the selected reference composite sync is present, counter 4U23-13 will be held reset throughout most of the field. If a vertical interval is missing, one-shot 4U23-10 will not be triggered and its output will remain high. In that case, counter 4U23-13 will generate pulses at field rate. These pulses then pass through gate 4U21-8 and buffer 4U22-8 to the reference vertical output at connector contact 74.

As long as reference vertical pulses are present, vertical generator one-shot 4U35-17 will be triggered once each field by the output of one-shot 4U23-10 and will generate a pulse. This pulse is fed to gate 4U21-8 where it becomes the reference vertical pulse.

Reference vertical pulses and reference horizontal pulses are compared in 4U27-5 to produce reference frame pulses.

If selected reference composite sync input is removed, vertical generator one-shot 4U35-17 is no longer triggered. Counter 4U23-13 continues to supply reference vertical and frame rate pulses, but they are not synchronized to any external reference.

The REF VERT output is furnished to the tracking one-shot in the Servo PWA control track logic. It is also routed to the Control PWA where it triggers the vertical interrupt (INT 0) to the control system CPU.

REF FRAME output is routed to the color field 1 identifier on the Reference PWA and to the Control PWA where it triggers the control track interrupt (INT 3) to the control system CPU.

5-40 Line Rate Multiples

Line rate (H) multiples are derived from the 256H output of VCO 4U8. VCO output frequency can be shifted +/-2% by the digital ramp and sample phase comparator

(4U19, 4U13, 4U22-10,4R32-4R35, and 4U5-7). On every H pulse from the selected reference composite sync input, the phase comparator output retimes the H rate output of divider 4U27-9 to coincide with the 256H (REF 4MHz) output of the VCO. If selected reference composite sync input is absent, phase comparator output is reset, and the L/C input network to the VCO is forced to its nominal value.

5-41 Phase Comparison with Sync Input. Timer 4U35-10 is the half-line (2H) eliminator one-shot. Its programmed output differs between 525- and 625-line standards. H and 2H rate pulses derived from sync input are presented to gate 4U34-6. The gate output triggers one-shot 4U35-10, and the one-shot output is fed back to inhibit the other gate input. Since the one-shot output period is longer than half the horizontal period, the 2H components of the composite sync input are effectively eliminated. Outputs of gate 4U34-6 are therefore at H rate. The gate output is also applied to the D input of 4U40-5, which retimes the edges of input H to coincide with the edges of the 256H output of the VCO.

Timer 4U23-17 is programmed as a retriggerable one-shot which stays triggered as long as selected reference composite sync input is present. Its programmed value is the same for 525- and 625-line standards. It counts a large number of H pulse outputs from divider 4U27-9 equivalent to 2 or 3 vertical intervals. As long as sync input is present, the output of 4U23-17 remains low. This prevents loading of up/down counter 4U19 and resetting of D latch 4U13.

The ramp and sample phase comparator is composed of 4-bit up/down (U/D) counter 4U19, 4-bit D latch 4U13, inverter 4U22-10, digital-to-analog (D/A) resistor network 4R32--4R35, and summing junction 4U5-7. As long as sync input is present, the inverted output of one-shot 4U23-17 holds a high on the load input of U/D counter 4U19. Thus, the preset count of 8, present at its load inputs, is not loaded into the counter. Inverter 4U22-10 at the output of the 8 bit, however, forces a count of 8 (half scale) into D latch 4U13 when the latch is clocked by H.

Depending on the count present in 4-bit D latch 4U13, the summing junction of D/A converter 4R32--4R35 is at one of 16 voltage levels from 0V to +5V. With the 8 bit present, the output of the D/A converter is +2.5V.

Square-wave, H-rate output of divider 4U27-9 controls the count direction of 4U19 (high = up, low = down). 4U19 is clocked by the 256H output of the VCO, 4U8. Thus, when H is high, the counter will count upward at 256H rate, and vice versa. When a full 16 counts have been made in either direction, the carry output is fed back to inhibit the counter.

Count output of 4U19 is presented broadside to 4-bit D latch 4U13. The purpose of 4U13 is to take a snapshot of the U/D counter contents at H rate. 4U13 is clocked and the contents of the U/D counter are sampled on each positive transition of H by the positive-going Q output of 4U40-5. The sampled count, converted to an analog error voltage by 4R32—4R35, adjusts varactor diode 4CR1. The 256H VCO output frequency is thus adjusted to line up H on the transition of REF 4 MHz (256H).

The maximum count of 15 in 4U19 is equivalent to 15 clock periods of 256H pulses. This is about 4 µs and is the point at which the phase comparator, or phase locked loop, loses lock. In practice, the stored count in 4U13 (and analog error voltage) equals a few hundred nanoseconds. The length of the digital ramp determines the maximum tolerable error between selected reference composite sync and synthesized sync.

5-42 **Sync Input Absent**. If the selected reference composite sync input is removed, the sync detector one-shot, 4U23-17, times out. Its inverted output goes low, causing the count of 8 to be loaded into U/D counter 4U19 and 4-bit D latch 4U13 to be held in reset. Thus, when 4U13 is sampled at H rate by the Q output of 4U40-5, latches are all in reset state, and analog error voltage at test point 4TP1 is forced to a nominal (zero error) value. With no sync input, phase error can neither be determined nor corrected. Thus, the VCO continues supplying 256H pulses at the frequency determined by the uncorrected D/A converter network at its input.

The 256H (REF 4 MHz) output of VCO 4U8 is provided to the Servo PWA where it is the external clock (EXtal) for servo system CPU 5U32. It is also divided to 2 MHz to clock the inner loop reference in the capstan servo and to clock the scanner servo phase error counter. The 256H output of 4U8 is also divided to 128H by 4U28-8.

The 128H output of 4U28-8 clocks synchronized counter 4U23-13 and vertical one-shot 4U23-10. It also clocks half-line eliminator one-shot 4U35-10, 4-to-1 divider 4U35-13, and vertical generator one-shot 4U35-17.

The output of 4-to-1 divider 4U35-13 is 32H. This is further counted down by 4U26 to 16H and 2H. The 16H output is furnished to the Audio PWA where it is further counted down to 125-kHz bias and 79-kHz erase frequencies. The 2H output is routed to the reel servo where it is used to clock tape speed counters.

5-43 Playback Sync Processor

Playback sync processor circuits on PWA 4 are shown in Figure 5-10. The playback sync processor receives demod composite sync and a dropout detection signal from the Mod/Demod PWA and processed scanner tach pulses. It provides vertical interval and tape dropout information to the time-base corrector. It also supplies vertical blanking and tape (servo) vertical pulses to the Reference PWA for insertion of vertical sync in the video output to the picture monitor. An edit phase error signal (derived from comparing reference frame pulses with tape frame pulses) is provided to the Servo PWA, and playback frame information is furnished to the AST servo.

Vertical information for the time-base corrector is derived from artificially generated signals derived from off-tape (demod) composite sync. Demod composite sync rate can vary over a wide range from zero tape speed, in which there is no vertical broad pulse at all, to maximum at 1.5X normal play speed. A phase-locked loop adjusts clock frequency provided to the various timers and counters.

Timing derived from off-tape information is further complicated by the AST servo. Vertical sync is normally considered to be the first part of a video field. This can cause some confusion in a Type C video format VTR because vertical sync is recorded at the last part of the track. Since off-tape video is continuous, this is not a problem in playback until AST logic decides to jump tracks and the normal playback sequence is altered. As a result, the last information on the track before the jump does not represent vertical sync of the track that is about to be played. Furthermore, there are no longer the same number of horizontal video lines between two successive vertical intervals. The servo system CPU supplies and coordinates the necessary recalculations via the AST servo data bus.

Note

> **Servo PWA and AST Servo PWA schematics (1450308 and 1450258) employ the following Ampex convention :**
>
> **Input data buffer and output data latch chips each contain eight circuits. Where possible, they are drawn conventionally in one block as shown in Figure 5-11. However, when it is expedient to show individual circuits in different parts (or on different sheets) of the schematic, they may also be drawn separately. This is also shown in Figure 5-11. Reference designations shown are hypothetical only.**
>
> **When individual circuits are drawn separately, the data bit (D) number is shown adjacent to the data bus, regardless of whether it is an input or an output. Similarly, the port (P) number is shown at the opposite end of the block adjacent to the source (or destination).**

5-44 Horizontal Sync Processing

Development of horizontal and vertical pulses depends first on detection of the first two pre-equalizing pulses (equalizers) within demod composite sync.

Demod composite sync from the Mod/Demod PWA enters the AST Servo PWA at contact 73. In the absence of a tape dropout, gate 4U30-3 is enabled. Gate output is applied to a short time constant integrator composed of 4R60 and 4C46, which filters high-frequency noise. The input signal is then applied to pulse shaper 4U17-7. Shaper output (4TP4 COMP SYNC) triggers timer 0 of PIT chip 4U11 which is a 3-μs digital one-shot. The one-shot is clocked by the buffered 64H output of oscillator 4U7. (Eleven of the 12 individual PIT timers shown in Figure 5-10 are clocked by the buffered 64H output of oscillator 4U7.)

Buffered and inverted 3-μs output at 4U11-10 is fed back to gates 4U30-6 and 4U15-6. This output is narrower than sync but wider than an equalizer pulse. Trailing edges of the six equalizers (HS in Figure 5-10) appear at 4U30-6. This output triggers timer 4U11-13, which is a 48-μs digital one-shot. This output is greater than a half line and less than one line. The one-shot output is applied to gate 4U15-11.

Output of gate 4U15-6 triggers timer 4U11-17 which is also a 48-μs one-shot. This one-shot eliminates the first equalizer. The output (4TP6) is a 48-μs wide negative-

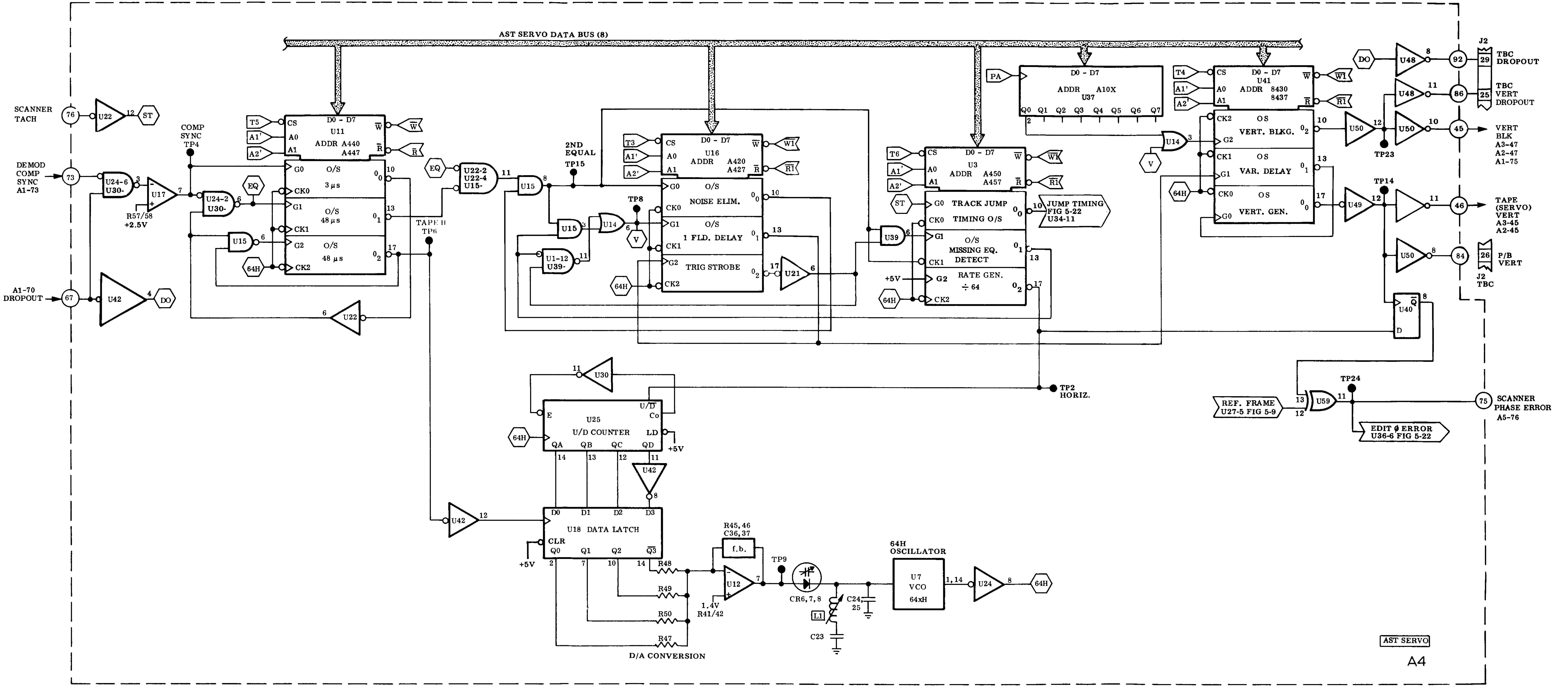


Figure 5-10.
Playback Sync Processor—PWA 4

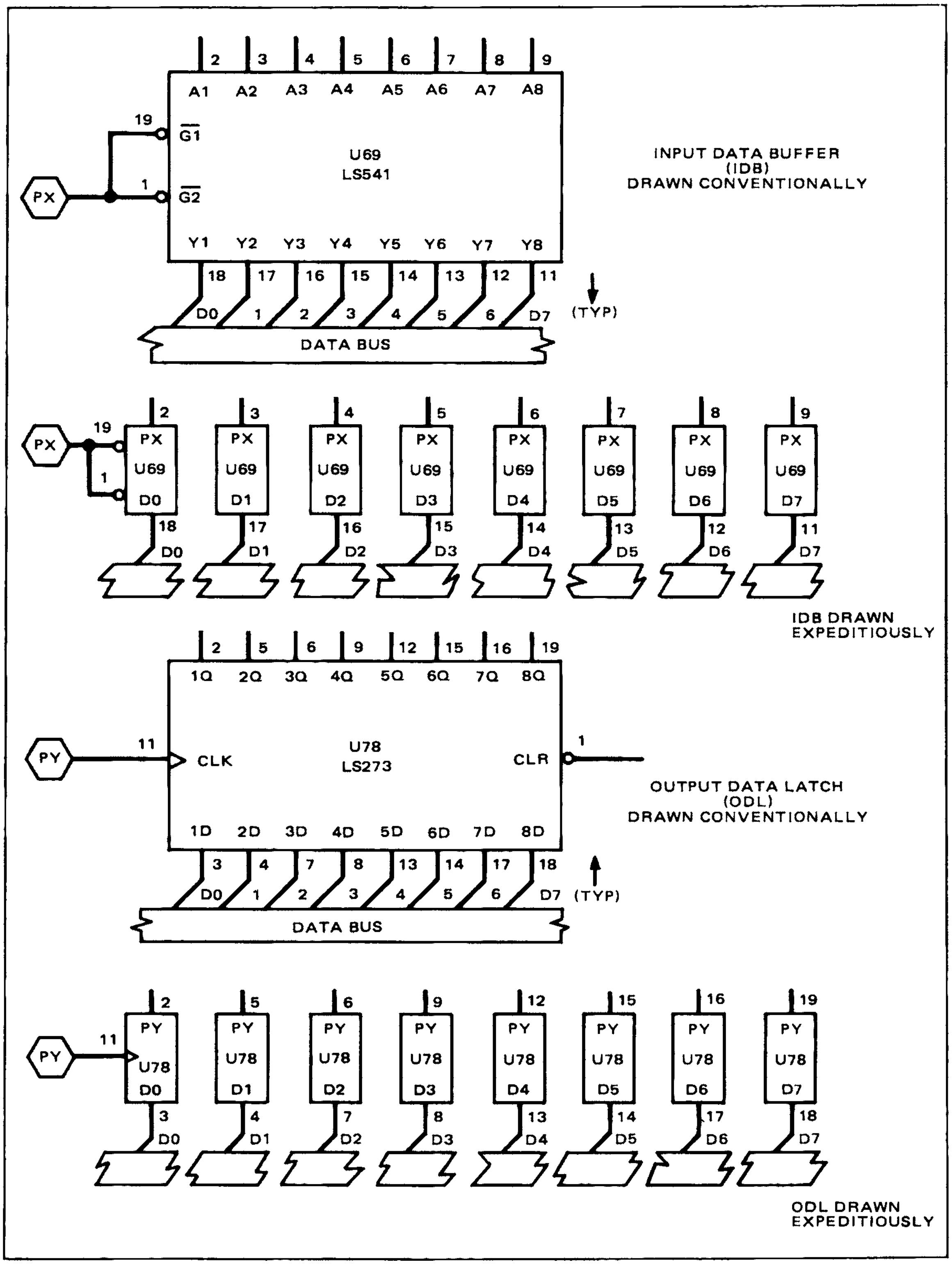


Figure 5-11. Input Data Buffer/Output Data Latch Schematic Conventions

going pulse. This is the tape H signal which clocks quad latch 4U18, thereby sampling phase error between tape H and the H-rate signal synthesized by the playback sync processor.

5-45 Phase Comparison with Tape H. Timer 4U3-17 is a divide-by-64 H-rate generator. The enable input (G2) is hard-wired to +5V, and the timer is clocked by the 64H output of oscillator 4U7. The output at 4U3-17 is thus a synthesized H-rate square wave.

The tape H ramp and sample phase comparator is composed of 4-bit up/down (U/D) counter 4U25, 4-bit D latch 4U18, inverter 4U42-8, digital-to-analog (D/A) resistor network 4R47—4R50, and summing junction integrator 4U12-7. The load input of U/D counter 4U25 is permanently inhibited. Thus, the preset count of 8, present at its load inputs, is never loaded into the counter. Depending on the count present in 4-bit D latch 4U18, the summing junction of D/A converter 4R47—4R50 is at one of 16 voltage levels from 0V to +5V.

Square-wave, H-rate output of divider 4U3-17 controls the count direction of 4U25 (high = up, low = down). 4U25 is clocked by the 64H output of the VCO, 4U7. Thus, when H is high, the counter will count upward at 64H rate, and vice versa. When a full 16 counts have been made in either direction, the carry output is fed back to inhibit the counter.

The count output of 4U25 is presented broadside to 4-bit D latch 4U18. The purpose of 4U18 is to take a snapshot of the U/D counter contents at H rate. 4U18 is clocked and contents of the U/D counter are sampled on each negative-going transition of H by the positive-going output of inverter 4U42-12. The sampled count, converted to an analog error voltage by 4R47—4R50, adjusts varactor diodes 4CR6—4CR8. The 64H VCO output frequency is thus adjusted to line up on the transition of H (4TP2).

The maximum count of 15 in 4U25 is equivalent to 15 clock periods of 64H pulses. This is about 16 µs, and is the point at which the phase comparator, or phase-locked loop, loses lock. In practice, the stored count in 4U18 (and analog error voltage) equals a very few microseconds. Length of the digital ramp determines the maximum tolerable error between tape H and synthesized H.

If tape H drops out, the last count clocked into quad latch 4U18 remains there. With no tape H input, phase error can neither be determined nor corrected. Thus, the VCO continues supplying 64H pulses at the frequency determined by the voltage from the D/A converter network at its input until tape H is restored.

5-46 Vertical Sync Processing

Timer 4U16-10 is a vertical rate one-shot which is triggered by the second equalizer. The six HS pulses (trailing edges of equalizers) and the 48-µs output of 4U11-13 trigger one-shot 4U16-10 through AND gate 4U15-8. The output of one-shot 4U16-10 is fed back to inhibit its trigger input at the AND gate. The output of gate 4U15-8 is the second equalizer (4TP15). The vertical rate output of one-shot 4U16-10 eliminates the rest of the equalizers. Actual programmed output of 4U16-

10 is slightly less than one vertical interval (15.9 µs for 525-line standard, 19.9 µs for 625-line standard).

The second equalizer pulse at 4U15-8 passes through enabled AND gate 4U15-3 and OR gate 4U14-6. The vertical rate output (V) of OR gate 4U14-6 triggers one-field delay one-shot 4U16-13. The second equalizer pulse at 4U15-8 is also applied to AND gate 4U39-6.

Output of one-shot 4U16-13 extends to about three horizontal lines before the start of the next vertical interval. It is therefore a prediction of the next vertical pulse. It triggers variable delay one-shots 4U41-13 and 4U16-17. CPU 5U32 loads values into these one-shots via the data bus on every field. At the time of decision by the AST servo to jump (or not jump) tracks, the CPU loads 4U16-17 and 4U41-13 with new values based on track jump timing. (See paragraph 5-91.) The scheme here is that if the second equalizing pulse is not detected, and therefore cannot trigger one-shot 4U16-13, inverted output of one-shot 4U16-17 will enable one-shot 4U3-13 through AND gate 4U39-6. One-shot 4U3-13 is the missing equalizer one-shot and its output will trigger one-shot 4U16-13 via 4U1-12, gate 4U39-11, and OR gate 4U14-6. Therefore, even if the second equalizing pulse is missing, the output of OR gate 4U14-6 can be maintained at vertical (V) rate, and the output of one-shot 4U16-13 can trigger vertical interval pulses via one-shots 4U41-13/-17.

The vertical rate (V) output of OR gate 4U14-6 clocks vertical blanking pulse generator 4U41-10 through OR gate 4U14-3. The vertical blanking pulse output is buffered and inverted by 4U48-11 where it is routed to the time-base corrector as vertical dropout signal. Output of 4U50-10 is the vertical blanking signal which is routed to the demodulator sync stripper on the Mod/Demod PWA and to the demod video sync insertion circuitry on the Reference PWA. Vertical blanking output signals can also be initiated or disabled by the servo system CPU via output data buffer 4U37-2.

Output of one-shot 4U16-13 enables variable delay one-shot 4U41-13, which is varied by the value loaded into the timer by the servo system CPU. The amount of delay is based on track jump information from the AST servo. (See paragraph 5-91.) One-shot 4U41-13 triggers vertical pulse generator 4U41-17. The buffered output of 4U41-17 (4TP14) is the predicted tape (servo) vertical signal which is routed to the time-base corrector and to demod video sync insertion circuitry on the Reference PWA.

The pulse at 4TP14 goes positive at the start of predicted vertical, and it clocks flip-flop 4U40-8. Synthesized H (4TP2) is applied to the D input of the flip-flop. The result is frame rate square wave at 4U40-8. This is compared with reference frame from 4U27-5 (Figure 5-9) by exclusive OR gate 4U59-11. Output at 4U40-8 is 8 µs (525-line standard) or 10 µs (625-line standard) early with respect to reference frame. Since both inputs are high, exclusive OR gate output (4TP24) is ideally a train of 8-us-wide pulses. This output is routed to the servo where it gates the edit phase error counter. The width of the positive-going pulse is the gauge of edit phase error. Output of exclusive OR gate 4U59-11 is also routed to input data buffer 4U36 in the AST servo. See Figure 5-22.

Off-tape dropout detected on the Mod/Demod PWA causes input at PWA 4 connector contact 67 to go low. This low input inhibits gate 4U30-3 (demod composite sync) and is routed through inverters 4U42-4 and 4U48-8 to the time-base corrector. Details of the dropout signal path are shown in the AST servo block diagram (Figure 5-22).

Processed scanner tach input at PWA 4 connector contact 76 triggers track jump timing one-shot 4U3-10. The output path of 4U3-10 is shown in Figure 5-22.

5-47 Control Track Logic

The VPR-80 generates a control track signal when in nonedit record and assemble edit modes. The control track waveform conforms with either Figure 1 in SMPTE Recommended Practice RP 85-1979* or Figure 8 in EBU Technical Information Sheet No. 7**. The SMPTE document refers to the control track signal as the "tracking-control" signal. The EBU document refers to the control track signal simply as the "control" signal. In the following discussion, this signal is termed the control track (CT) signal and should be considered synonymous with both the SMPTE and EBU terminology.

The CT signal generator and CT monitoring circuits are located on the Servo PWA. CT logic and the capstan servo are shown in Figure 5-12. Most of the CT circuits are shown in the lower part of the diagram. Figure 5-12 also shows CT recording circuits on the Audio PWA. CT recording circuits are explained in Section 4, Part II.

Six signal mnemonics are used in the CT signal logic portion of Figure 5-12.

CAP	Capstan velocity error analog voltage
CF	(This signal is always low— disregard it.)
CT	Control track signal
CT'	Frame rate component of playback CT
C7	Standard (high = SMPTE, low = EBU)
REF	Reference frame (derived from delayed reference vertical)

CT signal generation in accordance with both SMPTE and EBU standards is based on two signals: reference vertical from the reference pulse generator on the AST Servo PWA (Figure 5-9), and color frame reference from the color field 1 identifier on the Reference PWA. Refer to Figures 5-6 and 3-2 (NTSC), Figures 5-7 and 3-5

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*Society of Motion Picture and Television Engineers Recommended Practice RP 85-1979 entitled: Tracking-Control Record for 1-in Type C Helical Scan Video Tape Recording.

**European Broadcasting Union Technical Information Sheet No. 7 entitled: Specifications for a Helical-Scan Non-Segmented Field Television Recording on 25.4 mm (One Inch) Tape (E.B.U. Format C).

(PAL-M), or Figures 5-8 and 3-8 (PAL/SECAM). Reference vertical enters the Servo PWA at connector contact 73. Color frame reference enters the Servo PWA at connector contact 4, as shown in Figure 5-12.

In play modes, the off-tape CT signal is compared with reference frame, 2X frame, and (EBU CT only) 4X frame to regulate capstan speed and maintain color framing.

Both SMPTE and EBU standards specify that CT signal transitions should begin midway through the field period (within tolerances). Tracking delay one-shot 5U23-10 provides this timing. Reference vertical gates 5U23-10 which is clocked by E pulses. The servo system CPU presets a value in 5U23-10 on each vertical interval. The preset value causes the output at 5U23-10 to go low at vertical rate with the nominal half-field delay. If the AST is off, the delay can be modified by the TRACKING control. Absolute value of the delay can also be modified by edit optimization.

5-48 SMPTE Standard

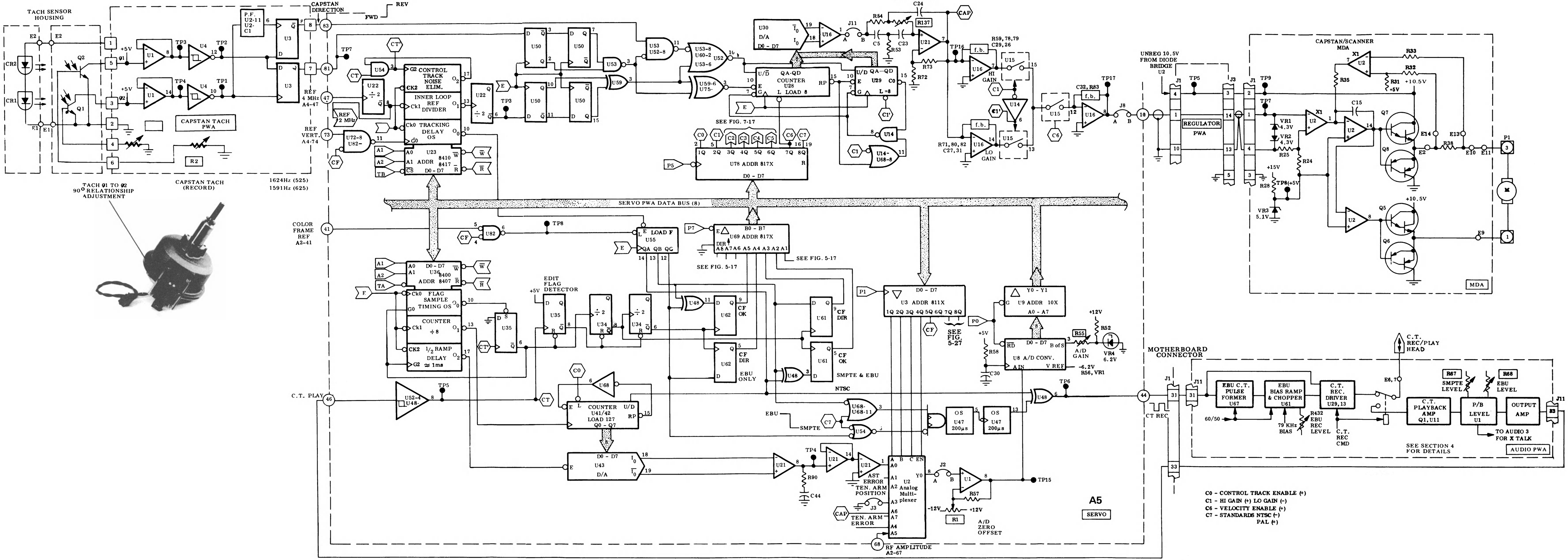
The SMPTE CT signal consists of saturated square waves that alternate in polarity at field rate with an extra pair of transitions added on alternate frames to identify the color frame. The alternate frame identification pulse also identifies field I. See Figure 5-13.

5-49 **SMPTE Control Track Signal Generation**. Divide-by-8 counter 5U55 is loaded with all ONEs (F hex) by the color frame reference pulse, and it is clocked by E pulses. Counting is inhibited unless the enable input is low. The delayed vertical rate output of one-shot 5U23-10 supplies the enabling input. The counter is enabled for only one clock cycle at a time. Thus, the three outputs of 5U55 are divided vertical rate and all are phased to reference color frame. The QA output is frame rate (delayed reference vertical divided by 2), and the QB output is one-half frame rate. (The QC output is not used for SMPTE CT signal.)

The QA output (REF) of counter 5U55 is applied to exclusive OR gate 5U48-6. Output of gate 5U48-6 is modulated by QA and QB outputs of 5U55 to form the SMPTE CT waveform shown in Figure 5-13.

For SMPTE standard, the C7 output of output data latch 5U78 is always low. This steady state level holds the output of OR gate 5U54-6 low, thus satisfying half of the input AND gate to one-shot 5U47-5.

The QB output of 5U55 is applied to OR gate 5U68-3. The OR gate performs an AND gate function due to the presence of C7 (low) at 5U68-11. When the QB output of 5U55 goes low, the high output of gate 5U68-3 satisfies the other half of the input AND gate to one-shot 5U47-5. One-shots 5U47-5 and 5U47-13 are thus triggered in tandem. Output of one-shot 5U47-13 is applied to exclusive OR gate 5U48-6. Exclusive OR gate output is the CT waveform which is routed to the CT record electronics on the Audio PWA (see paragraphs 4-15 and 4-16 in Section 4, Part II).



C0 - CONTROL TRACK ENABLE (+)
C1 - HI GAIN (+) LO GAIN (-)
C6 - VELOCITY ENABLE (+)
C7 - STANDARDS NTSC (-)
PAL (+)

Figure 5-12.
Control Track Logic and
Capstan Servo—PWA 5

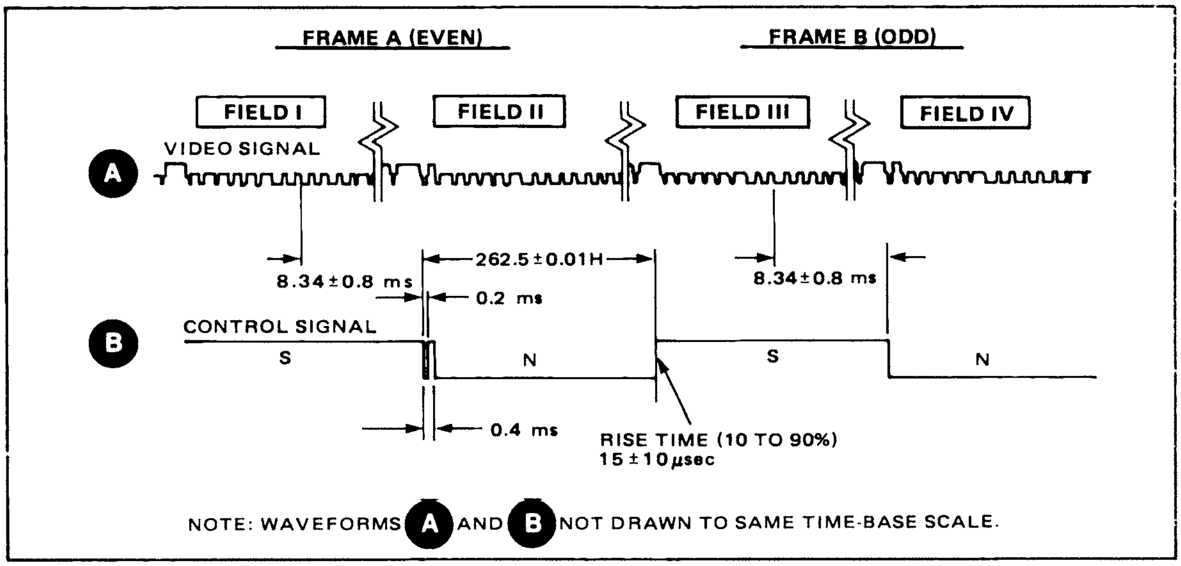


Figure 5-13. SMPTE Control Track Format

5-50 SMPTE Control Track Lock. During play modes, the off-tape CT signal is examined to ensure proper color framing. Off-tape control track is compared to reference control track at frame rate intervals, or twice per color frame.

The CT playback input from the Audio PWA enters the Servo PWA at connector contact 46. The playback signal is applied to input amplifier and pulse shaper 5U52-4 and 5U48-8. Output at test point 5TP5 is playback CT which is applied through enabled AND gate 5U54-3 to trigger CT noise eliminator one-shot 5U23-17. The one-shot eliminates the playback CT transitions between frame rate transitions (including the color frame edit flag). The result is a 30-Hz frame rate signal (CT') at 5U54-3. Timing relationships are shown in Figure 5-14. The CT' output of AND gate 5U54-3 is the filtered frame rate pulse which drives the timing logic. CT', which is about 1 µs wide, clocks edit flag detection enable flip-flop 5U35-6. The signal at 5U35-6 removes the reset from edit flag detector 5U35-8, clocks V/4 divider 5U34-8, triggers half-ramp delay one-shot 5U36-17, and triggers flag sample timing one-shot 5U36-10.

Flip-flop 5U35-6 acts as a gate to allow the edit (color frame) flag to be detected. The CT' pulse clocks 5U35-6 high. At the same time, it triggers edit flag sample timing one-shot 5U36-10. That one-shot determines how long the output of 5U35-6 will be high. It is during this time that edit flag detector 5U35-8 can be clocked low by the edit flag.

Output of 5U36-10 forces 5U35-6 low until it is clocked high by the next positive-going edge of CT'. The resulting output of V/4 divider 5U34-8 is a 15-Hz square wave which is changing state on the positive-going edges of CT'. The 15-Hz square wave (high for one frame, low for one frame) clocks flip-flops 5U61-5 and 5U61-9.

The QA output of 5U55 is reference 30Hz. The QB output of 5U55 is reference 15 Hz. Both are phased to the color frame reference input. Reference 30 Hz and

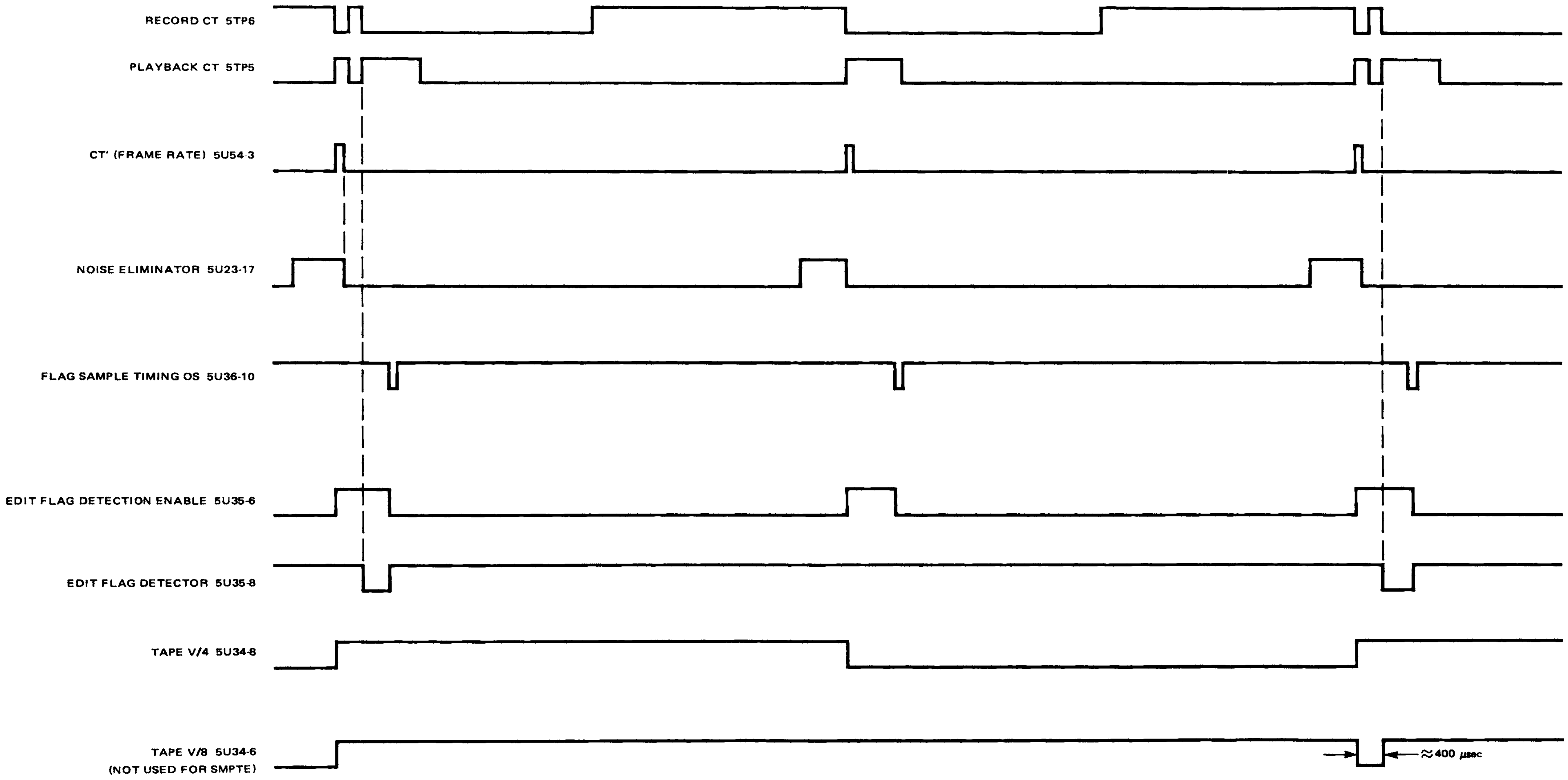


Figure 5-14.
SMPTE Control Track Playback Timing

reference 15 Hz are applied to exclusive OR gate 5U48-3. Exclusive OR gate output is applied to the D input of 5U61-5.

When 5U61-5 is clocked by the 15-Hz square wave from 5U34-8, output at 5U61-5 will be high if color framing is within a correction window. This information is sent to the CPU via input data buffer 5U69. If color framing is not within this window, the output at 5U61-5 will be low. If the output is low, the CPU will cause the capstan servo to slow down or speed up the capstan to bring color frame within the correction range of the control track phase comparator, or color frame window.

Reference 15 Hz from 5U55 is presented to the D input of flip-flop 5U61-9, and the flip-flop is clocked by 15 Hz derived from playback control track (5U34-8). The output level of 5U61-9 tells which is the faster way to correct the capstan toward color framing. High output indicates a capstan speedup would be the faster way. Low output indicates slowing the capstan would be the faster way. This information is also supplied to the CPU via input data buffer 5U69. This coarse correction brings color framing into the color frame window, so that the remaining phase error can be measured (and cancelled) by the control track phase comparator.

The CT phase comparator is a digital ramp-and-sample arrangement composed of up/down counter 5U41/42, digital-to-analog converter (DAC) 5U43 and 5U21-8/-14/-1. The count direction of 5U41/42 is governed by the reference 30-Hz QA output of 5U55. The counter is clocked by the 2H output of 5U36-13, and the half-scale count of 127 is loaded into the counter when C0 from output data latch 5U78 is asserted (low) by the CPU. C0 is high (not asserted) when the capstan servo is not in velocity lock. This inhibits the control track phase comparator while the capstan servo is correcting to the color frame window and for a short time after correction has been completed.

Counter 5U41/42 counts upward during one frame (QA output of 5U55 high), and then down during the next frame (QA output of 5U55 low). When the counter reaches the full count of 255, the carry output is fed back to the enable input to inhibit further counting.

Counter contents are presented broadside to DAC 5U43. The DAC analog output is enabled by the output of half-ramp delay one-shot 5U36-17. When enabled, the analog output of DAC 5U43 is presented through 5U21-8/-14/-1 to one input of analog multiplexer 5U2.

Other analog inputs to multiplexer 5U2 are: AST error, tension arm position, capstan servo velocity error, and tension arm error. The four least significant bit outputs of output data buffer 5U3 select the multiplexer input for application to analog-to-digital converter ADC 5U8. Digitized control track phase error is supplied to the CPU via input data buffer 5U9. The CPU responds by correcting the inner loop reference of the capstan servo. See paragraph 5-64.

Gain adjustment of ADC 5U8 is provided by 5R55. (See paragraph 5-134.) Zero offset adjustment is provided by 5R1 at the input of ADC 5U8. (See paragraph 5-135.)

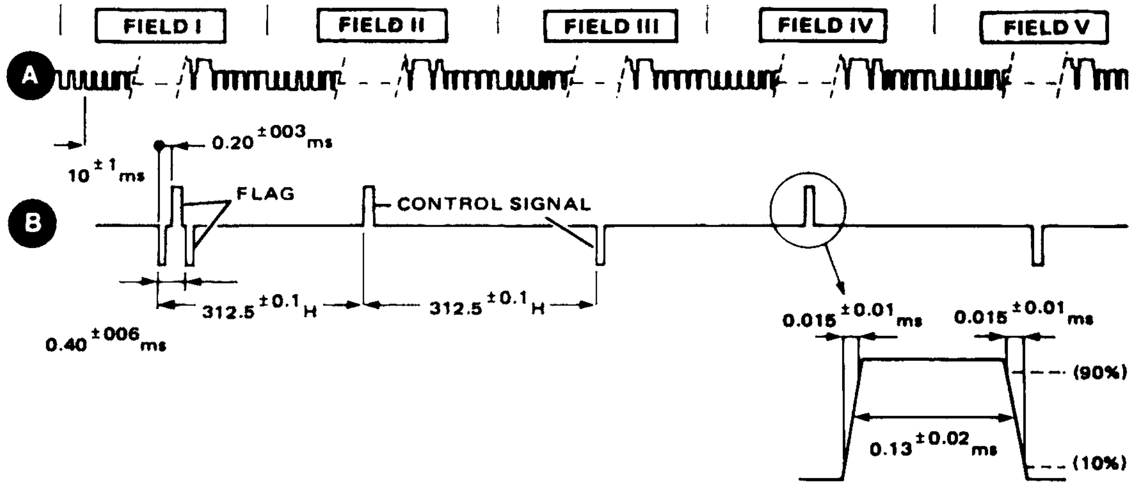
5-51 EBU Standard

The EBU control track signal consists of a series of alternating polarity pulses with an extra pulse added to identify the PAL eight-field color frame sequence. See Figure 5-15.

5-52 EBU Control Track Signal Generation. Divide-by-8 counter 5U55 is loaded with all ONEs (F hex) by the color frame reference pulse, and it is clocked by 1-MHz E pulses. Counting is inhibited unless the enable input is low. The delayed vertical rate output of one-shot 5U23-10 supplies enabling input. Thus, the three outputs of 5U55 are divided vertical rate and all are phased to reference color frame. The QA output is frame rate (delayed reference vertical divided by 2), and the QC output is one-quarter frame rate (6.25 Hz). (The QB output is not used in recording the EBU CT signal.)

The QA output (REF) of counter 5U55 is applied to exclusive OR gate 5U48-6. The output of gate 5U48-6 is modulated by the QA and QC outputs of 5U55 to form the basis of the EBU CT waveform shown in Figure 5-15.

For EBU standard, the C7 output of output data latch 5U78 is always high. Thus, the output of gate 5U68-11 is low, and the output of gate 5U68-3 is high. The steady state high output of 5U68-3 satisfies one half of the input AND gate to one-shot 5U47-5.



NOTES: 1. THE FIGURE SHOWS THE TRACKING CONTROL WAVEFORM AND TIMING. AN EDIT PULSE IS INCLUDED WHICH IDENTIFIES THE PAL EIGHT-FIELD SEQUENCE. THE PAL/SECAM FOUR-FIELD SEQUENCE CAN BE DERIVED FROM THIS INFORMATION.

2. WAVEFORMS Ⓐ AND Ⓑ NOT DRAWN TO SAME TIME-BASE SCALE.

Figure 5-15. EBU Control Track Format

The QC output of 5U55 is applied to one input of OR gate 5U54-6. This OR gate performs an AND gate function due to the presence of C7 (high) at the other input. When the QC output of 5U55 goes low, the low output of gate 5U54-6 satisfies the other half of the input AND gate to one-shot 5U47-5. One-shots 5U47-5 and 5U47-13 are thus triggered in tandem. The output of one-shot 5U47-13 is applied to exclusive OR gate 5U48-6. The exclusive OR gate output is the basic CT signal which is routed to the CT record electronics on the Audio PWA (see paragraphs 4-15 and 4-17 in Section 4, Part II).

5-53 EBU Control Track Lock. During play modes, the off-tape CT signal is examined to ensure proper color framing. Off-tape control track is compared to reference control track at frame rate intervals, or four times per color frame.

The CT playback input from the Audio PWA enters the Servo PWA at connector contact 46. The playback signal is applied to input amplifier and pulse shaper 5U52-4 and 5U48-8. Output at test point 5TP5 is playback CT which is applied through enabled AND gate 5U54-3 to trigger CT noise eliminator one-shot 5U23-17. The one-shot eliminates playback CT transitions between frame rate transitions (including the color frame edit flag). The result is a 25-Hz frame rate signal (CT') at 5U54-3. Timing relationships are shown in Figure 5-16. The CT' output of AND gate 5U54-3 is the filtered frame rate pulse which drives the timing logic. CT', which is about 1 µs wide, clocks edit flag detection enable flip-flop 5U35-6. The signal at 5U35-6 removes the reset from edit flag detector 5U35-8, clocks V/4 divider 5U34-8, triggers half-ramp delay one-shot 5U36-17, and triggers flag sample timing one-shot 5U36-10. The V/4 output at 5U34-8 is divided to V/8 at the output of 5U34-6.

Flip-flop 5U35-6 acts as a gate to allow the edit (color frame) flag to be detected. The CT' pulse clocks 5U35-6 high. At the same time, it triggers edit flag sample timing one-shot 5U36-10. That one-shot determines how long the output of 5U35-6 will be high. It is during that time that edit flag detector 5U35-8 can be clocked low by the edit flag.

Output of 5U36-10 forces 5U35-6 low until it is clocked high by the next positive-going edge of CT'. The resulting output of V/4 divider 5U34-8 is a 12.5-Hz square wave which is changing state on the positive-going edges of CT'. The V/4 square wave (high for one frame, low for one frame) clocks flip-flops 5U61-5 and 5U61-9. The 12.5-Hz square wave output of 5U34-8 is divided to a 6.25-Hz (V/8) square wave at 5U34-6. The V/8 square wave clocks flip-flops 5U62-5 and 5U62-9.

The QA output of 5U55 is reference 25 Hz, the QB output is reference 12.5 Hz, and the QC output is reference 6.25 Hz. All are phased to the color frame reference input. Reference 25 Hz and reference 12.5 Hz are applied to exclusive OR gate 5U48-3. The exclusive OR gate output is applied to the D input of 5U61-5. Reference 12.5 Hz and reference 6.25 Hz are applied to exclusive OR gate 5U48-11. The exclusive OR gate output is applied to the D input of 5U62-9.

When 5U61-5 is clocked by the 12.5-Hz square wave from 5U34-8, output at 5U61-5 will be high if color framing is within a correction window. This information is sent

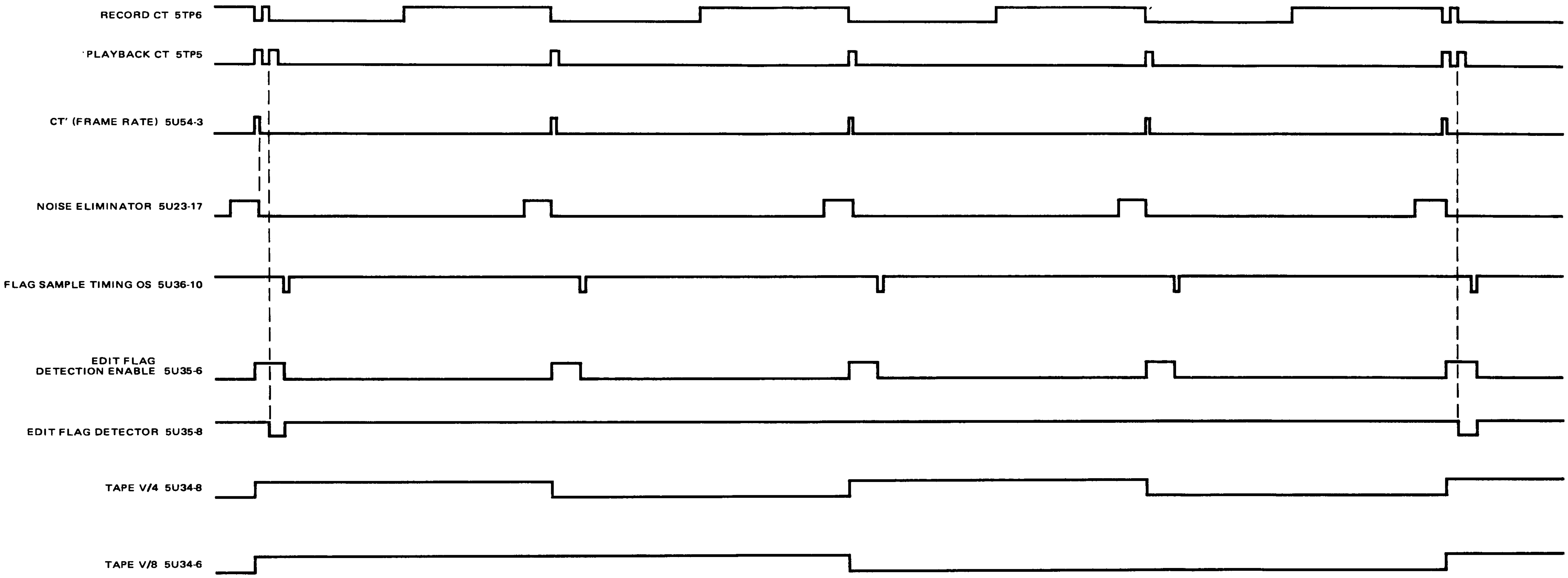


Figure 5-16.
EBU Control Track Playback Timing

to the CPU via input data buffer 5U69. If color framing is not within this window, output at 5U61-5 will be low. If output is low, the CPU will cause the capstan servo to slow down or speed up the capstan to bring color frame within correction range of the control track phase comparator, or color frame window.

Reference 12.5 Hz from 5U55 is presented to the D input of flip-flop 5U61-9, and the flip-flop is clocked by 12.5 Hz derived from playback control track (5U34-8). The output level of 5U61-9 tells which is the faster way to correct the capstan toward color framing. High output indicates a capstan speedup would be the faster way. Low output indicates slowing the capstan would be the faster way. This information is also supplied to the CPU via input data buffer 5U69. This coarse correction brings color framing into the color frame window, so that the remaining phase error can be measured (and cancelled) by the control track phase comparator.

Reference 6.25 Hz from 5U55 steers flip-flops 5U62-5/-9 and the V/8 output of 5U34-6 clocks the flip-flops in the same fashion to provide color frame window and to the CPU via input data buffer 5U69. If color framing is not within this window, direction to color frame lock information. Thus, control track lock is checked and adjusted, if necessary, four times per color frame.

The CT phase comparator is a digital ramp-and-sample arrangement composed of up/down counter 5U41/42, digital-to-analog converter (DAC) 5U43, and 5U21-8/-14/-1. The count direction of 5U41/42 is governed by the reference 25-Hz QA output of 5U55. The counter is clocked by the 2H output of 5U36-13, and the half-scale count of 127 is loaded into the counter when C0 from output data latch 5U78 is asserted (low) by the CPU. C0 is high (not asserted) when the capstan servo is not in velocity lock. This inhibits the control track phase comparator while the capstan servo is correcting to the color frame window, and for a short time after the correction has been completed.

Counter 5U41/42 counts upward during one frame (QA output of 5U55 high), and then down during the next frame (QA output of 5U55 low). When the counter reaches the full count of 255 the carry output is fed back to the enable input to inhibit further counting.

Counter contents are presented broadside to DAC 5U43. The DAC analog output is enabled by the output of half-ramp delay one-shot 5U36-17. When enabled, analog output of DAC 5U43 is presented through 5U21-8/-14/-1 to one input of analog multiplexer 5U2.

Other analog inputs to multiplexer 5U2 are: AST error, tension arm position, capstan servo velocity error, and tension arm error. The four least significant bit outputs of output data buffer 5U3 select the multiplexer input for application to analog-to-digital converter ADC 5U8. Digitized control track phase error is supplied to the CPU via input data buffer 5U9. The CPU responds by correcting the inner loop reference of the capstan servo. See paragraph 5-64.

Gain adjustment of ADC 5U8 is provided by 5R55. (See paragraph 5-134.) Zero offset adjustment is provided by 5R1 at the input of ADC 5U8. (See paragraph 5-135.)

5-54 Scanner Servo

The servo system CPU has three sources of program interrupt: scanner tach, delayed scanner tach, and AST interrupts. Refer to paragraph 5-36 and Figure 5-5.

Scanner tach interrupt is hardware-triggered by a processed tach pulse which occurs once per scanner revolution. The same tach pulse also triggers a one-shot which causes delayed scanner tach interrupt when the one-shot times out 128 µs later. Since AST interrupts occur at a much faster rate than scanner interrupts, the hardware-triggered scanner tach interrupt inhibits further recognition of AST interrupts until service of the delayed scanner tach interrupt has been completed.

Adjustment of the tach, which is the only scanner maintenance adjustment, is included in the VPR-80 interchange procedures. Refer to paragraph 4-29 in Section 4, Part I of this manual.

The scanner service routine is essentially composed of examining scanner velocity and phase errors which may have crept in since the previous tach pulse, and then developing corresponding corrections which are applied to the scanner motor through D/A converters and the scanner motor drive amplifier (MDA).

During edit play mode, the edit phase error from the playback sync processor is monitored. If edit phase error exceeds ±15 us, the operator is warned that edit optimization is required.

Figure 5-17 is the scanner servo block diagram. The following mnemonics are used in Figure 5-17.

Servo-initiated signals:

S0—Delayed tach flag
S1—Slow speed flag
S2—Scanner tach flag

CPU-initiated signals:

C2—Clear delayed tach and slow speed flags
C3—Clear AST interrupt
C4—Clear scanner tach interrupt
C5—Scanner servo enable

5-55 Scanner Tach Interrupt

The C5 output of output data latch 5U78 is applied to the D input of flip-flop 5U79-8/-9. When C5 is low, the scanner servo is enabled. Scanner tach pulses are applied to the Servo PWA at connector contact 91. Tach pulses, which rise from +2 to +8 Vdc at test point 5TP33, clock flip-flop 5U79-8/-9. The scanner tach flag (S2) output at 5U79-9 goes low. The low scanner tach flag bit (S2) is placed on the Servo PWA data bus via input data buffer 5U69. S2 initiates scanner tach interrupt (5TP13) through gates 5U73-11 and 5U73-8. CPU 5U32 recognizes the scanner tach interrupt by the assertion of the scanner tach flag. The CPU completes the current service of AST interrupt and inhibits further recognition of AST interrupts.

S2 is also routed to the AST Servo PWA via PWA contact 75. This output triggers track jump timing one-shot 4U3-10 (Figure 5-22).

The rising edge of the output at 5U79-8 triggers tach delay one-shot 5U77-10, which is clocked by E (1 MHz). CPU 5U32 then asserts C4. The C4 output of output data latch 5U78 clears scanner tach interrupt by setting flip-flop 5U79-8/-9 in preparation for the next scanner tach pulse.

Another input to gates 5U73-11/-8 is the AST interrupt. Timer 5U77-17 is permanently enabled and it is clocked by the 1-MHz E signal. The output signal at 5U77-17 is twice dither frequency (900 Hz for 525-line video, or 850 Hz for 625-line video). When this signal is divided by 5U80-5, the 450-Hz (525-line video) or 425-Hz (625-line video) AST interrupts are initiated through gates 5U73-11/-8. Further AST interrupts are inhibited by holding C3 high until delayed scanner tach interrupt has been cleared.

5-56 Delayed Scanner Tach Interrupt

When tach delay one-shot 5U77-10 times out, the output of flip-flop 5U79-5 (S0) goes low. S0 initiates the delayed scanner tach interrupt through gates 5U73-11/-8. S0 (delayed tach flag) is also placed on the Servo PWA data bus via input data buffer 5U69 for interrupt recognition by the CPU. When service of the delayed scanner tach interrupt has been completed, the CPU drives C2 low, which clears the interrupt by setting 5U79-5 in preparation for the next delayed scanner tach interrupt.,

The balance of the scanner servo operation is completely under control of the CPU and its firmware, and is therefore not apparent by looking at Figure 5-17. The scanner service routine is charted in Figure 5-18.

5-57 Velocity Loop

When the VPR-80 enters ready condition of stop mode, the scanner motor starts and the scanner servo brings it up to lock speed which is field rate (3000 rpm for 50-Hz line frequency, or 3600 rpm for 60-Hz line frequency). The servo system CPU asserts C5, thereby enabling delayed scanner tach interrupts and the scanner service routine diagrammed in Figure 5-18.

Velocity counter 5U77-13 is clocked by 1-MHz E pulses. It is a 16-bit ramp generator which is triggered by the CPU upon recognition of delayed tach flag (S0). Following scanner tach interrupt (recognition of S2), the CPU presets a count in 5U77-13. The counter is enabled and the ramp starts from this count upon recognition of S0. The preset count is the equivalent (in microseconds) of slightly less than one field period. (Absolute value of the preset count depends upon video standard which is indicated by the logic level from the Reference PWA at 5U52-2.) The CPU samples the count value in 5U77-13 upon recognition of the next delayed tach flag (S0).

During scanner motor run-up, counter 5U77-13 reaches full count long before (and several times before) the next assertion of S0 when the CPU samples the counter. S1 (slow speed flag) is asserted at U80-9 each time full count is reached. S1 tells

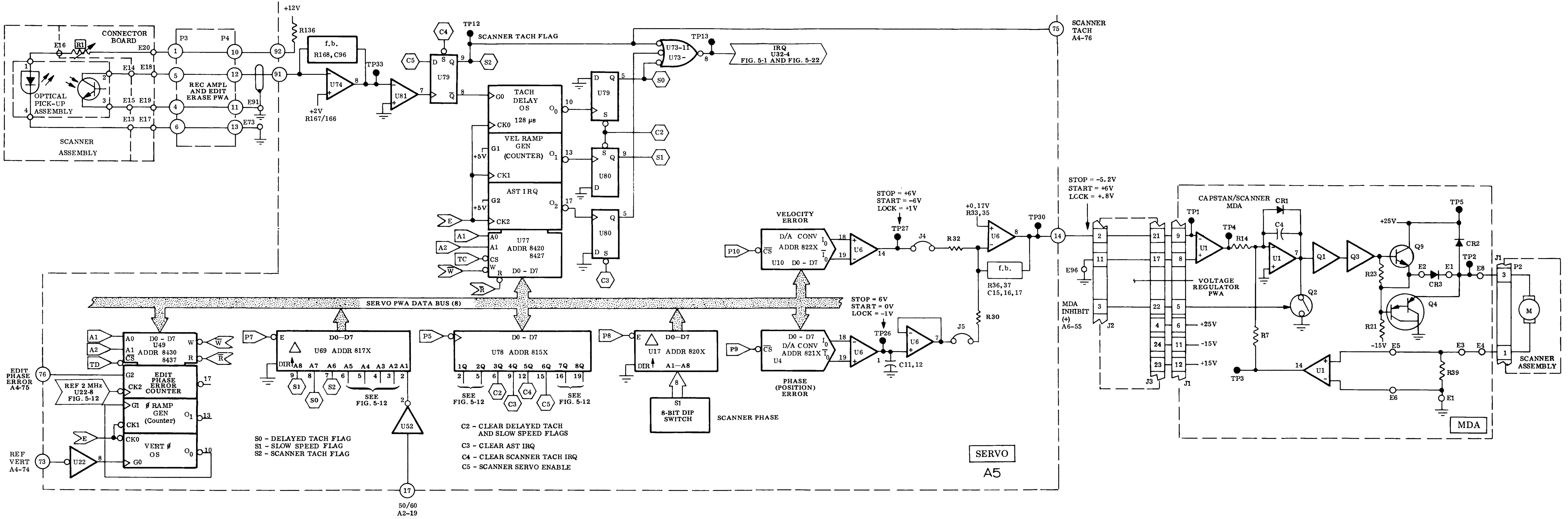
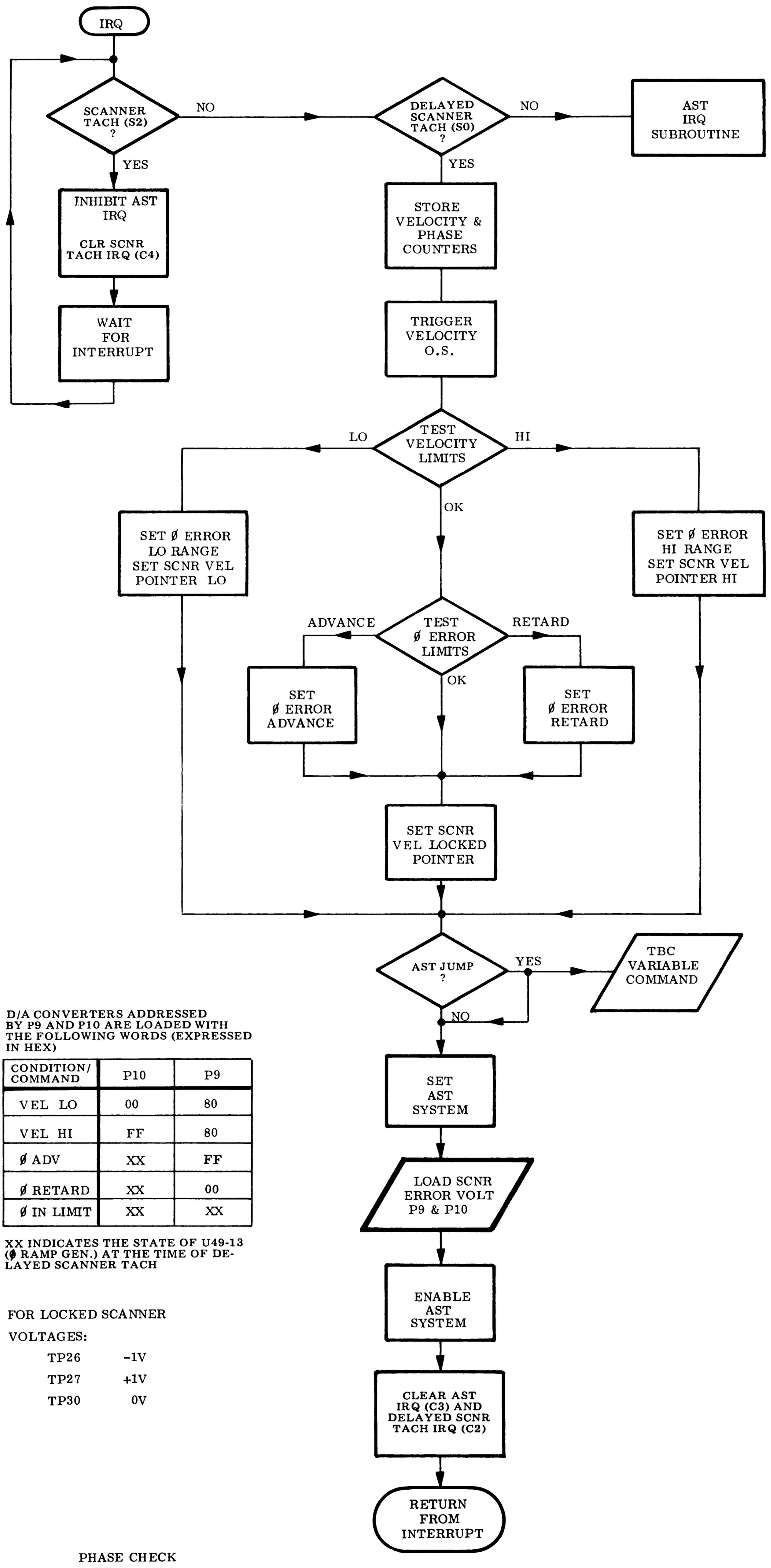


Figure 5-17.
Scanner Servo and MDA—PWA5



NOTE: D/A CONVERTERS ADDRESSED BY P9 AND P10 ARE LOADED WITH THE FOLLOWING WORDS (EXPRESSED IN HEX)

CONDITION/ COMMAND	P10	P9
VEL LO	00	80
VEL HI	FF	80
ø ADV	XX	FF
ø RETARD	XX	00
ø IN LIMIT	XX	XX

XX INDICATES THE STATE OF U49-13 (ø RAMP GEN.) AT THE TIME OF DELAYED SCANNER TACH

FOR LOCKED SCANNER
VOLTAGES:

TP26	-1V
TP27	+1V
TP30	0V

PHASE CHECK

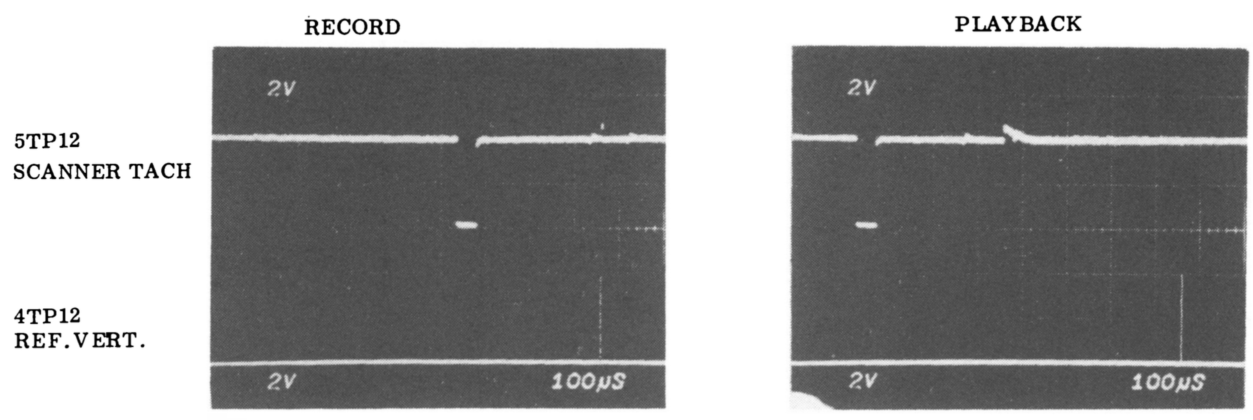


Figure 5-18.
Delayed Scanner
Tach Interrupt Flowchart

the CPU that low velocity limit has been grossly exceeded, and the CPU responds by setting scanner velocity pointer low and placing the maximum low velocity error word (00 hex) in digital-to-analog converter (DAC) 5U10 via the Servo PWA data bus. Corresponding analog correction voltage is applied through 5U6-14 to the 5R32/5R30 junction where velocity correction voltage is summed with phase correction voltage. At scanner motor startup, voltage at test point 5TP27 is -6V. Velocity error words from the CPU drive this voltage toward +1V at the maximum rate as long as S1 (slow speed flag) inputs from 5U80-9 are received via input data buffer 5U69.

If, after starting, the scanner motor cannot achieve 900 rpm within 5 seconds, the SYSTEM indicator is lighted, and the **scanner stall** indication (system code 11) is brought up for display. The SYSTEM indicator is also lighted (system code 11) if the scanner is unable to achieve velocity lock within 5 seconds *after* reaching 900 rpm. In either case, the control system will force the VPR-80 to stop mode/standby condition.

CPU 5U32 samples the accumulated count in velocity ramp generator 5U77-13 when S0 (delayed tach flag) is recognized. It then clears, presets, and restarts the counter. As the scanner picks up speed, the interval between samples decreases to the point where the counter does not have time to reach full count before the next sample is taken at S0 time. Thus, S1 ceases to be asserted at 5U80-9.

The sampled count in 5U77-13 is stored and compared with the narrow range of counts which correspond to lock speed. The high end of the range is the low velocity limit, and the low end of the range is the high velocity limit. As the high end of the count range (low velocity limit) is approached, the CPU asserts correspondingly decreased velocity error words to DAC 5U10. At lock speed (near zero velocity error), voltage at test point 5TP27 is +1V.

If scanner motor speed increases to the point where high velocity limit is exceeded (sampled count in 5U77-13 is too small), the CPU sets scanner velocity pointer high and asserts a velocity error word to DAC 5U10 which slows the scanner motor.

When either high or low velocity limit has been exceeded, the CPU looks at the status of the AST servo before applying the velocity error word to DAC 5U10. If the AST servo is about to make a track jump in the next vertical interval, the CPU sets normal/variable logic level output to the TBC low (variable). Variable command simply puts the TBC on notice that track jump is about to occur. (See paragraph 5-94.) The TBC interprets this input as slow-motion command and turns on the color processor because it may have to invert chroma. When track jump has been completed, AST and scanner servo corrections are applied.

Once the scanner motor has achieved lock speed, and the accumulated count in velocity ramp generator 5U77-13 is within set limits when sampled at S0 time, the SERVO indicator on the secondary control panel is turned off. Scanner motor speed corrections thereafter are very small, and chances of losing velocity servo lock are negligible, unless a mechanical problem tends to slow the scanner. There is no provision for manually entered adjustment in the velocity loop.

5-58 Phase (Position) Loop

The scanner phase (position) loop is not activated during the early part of scanner runup. The phase loop is turned on only after slow speed flags (S1) are no longer generated. The phase loop also uses a digital ramp generator, 5U49-13, which is clocked by E (1-MHz) pulses. The phase ramp generator is enabled after a preset delay following reference vertical, and the accumulated ramp value is sampled and stored by the CPU upon recognition of delayed tach flag (S0). The CPU then applies proportional corrections to the scanner MDA through DAC 5U4.

When in edit play mode, the edit phase error input from the playback sync processor is also monitored. If this error exceeds ±15 µs, an additional correction is applied to the scanner MDA.

5-59 Nonedit Modes. The preset value in one-shot 5U49-10 provides the delay before the phase ramp generator is enabled. Vertical phase one-shot 5U49-10 is clocked by 1-Mhz E and is triggered by reference vertical from the reference pulse generator on the AST Servo PWA (Figure 5-9). The nominal value preset in 5U49-10 is equivalent in microseconds to one-half field period. However, when in play mode, this value can be modified by H/2 increments which are manually entered with the first five sections of DIP switch 5S1 (SCANNER PHASE). The number of H/2 increments entered (in binary) depends on the particular time-base corrector used. H/2 values (i.e., 8H for the TBC-80) are given in the *VPR-80 Installation and Operation* manual. The CPU does not read the H/2 setting of switch 5S1 when in record mode. Absolute value (in microseconds) of the count preset in 5U49-10 depends upon video standard. The 50/60-Hz information is supplied by 5U52-2 through input data buffer 5U69.

Phase ramp generator 5U49-13 is enabled when vertical one-shot 5U49-10 times out. The count in 5U49-13 advances in 1-µs increments. When the CPU recognizes S0, the count in 5U49-13 is sampled and stored. The CPU also resets counter 5U49-13 at this time. The CPU then compares the sampled count against a narrow range of counts, which is equivalent to correct phase relationship between delayed scanner tach and reference vertical. If the sampled count is within the narrow range, no correction is necessary, and the CPU sets the scanner velocity locked pointer. If delayed scanner tach is too early (sampled count is too small), the CPU sets phase error retard. If delayed scanner tach is too late (sampled count is too large), the CPU sets phase error advance.

After checking AST servo status to see if a track jump is to be made in the next vertical interval and asserting TBC variable command if required, the CPU applies the corresponding scanner phase correction word to DAC 5U4 via the Servo PWA data bus. Analog phase correction voltage is applied to the 5R30/5R32 junction where it is summed with velocity correction voltage.

When the scanner motor starts, test point 5TP26 is at zero volts. This is corrected toward -1V which is seen there when the motor reaches phase lock velocity.

The edit phase error input at PWA connector contact 76 is disregarded by the CPU unless the VPR-80 is in edit mode.

5-60 Edit Modes. In edit modes, the scanner phase error is corrected as in nonedit modes, and there is one added feature. The scanner edit error input from the playback sync processor (Figure 5-10) is monitored, and if edit phase tolerance is exceeded, the necessity for edit optimization is indicated.

Ideally, the edit phase error input should be a positive pulse of no more than 15-µs width, occurring at frame rate. The width of this pulse is monitored by the CPU during edit playback (during preroll period). If there is more than 15-µs difference between the edit phase of the VTR which made the recording and the edit phase of the VPR-80 on which the tape is being edited, the SYSTEM indicator is lighted. The **edit phase range exceeded** indication (system code **10**) is brought up for display.

When system code **10** is indicated, the VTR operator should press the EDIT OPTIMIZE switch to initiate the automatic edit optimization sequence. Logic which controls the edit optimization sequence first tracks the head to the tape, thus peaking the playback rf, and then rephases the scanner tach to the timing of the video on the tape. (Control track is also rephased.) If the edit phase on the tape is outside the tolerance range for rephasing the scanner tach, the SYSTEM indicator is again lighted. The **unable to edit optimize** indication (system code **15**) is brought up for display.

The edit phase error input from exclusive OR gate 4U59-11 (Figure 5-10) triggers edit phase error counter 5U49-17. Counter 5U49-17 is clocked by reference 2 MHz from divider 5U22-8 (Figure 5-12). The CPU samples and stores the accumulated count in 5U49-17 upon recognition of S0. If less than 20 clock pulses are counted, no correction is necessary. If more than 20 clock pulses are counted, system code **10** is brought up for display, telling the VTR operator that the edit phase is exceeded and that edit optimize sequence should be initiated.

5-61 Scanner MDA

When both velocity and phase loops are locked, summing junction 5R30/5R32 is at zero volts. This level is biased by 5U6-8 so that the summed error voltage output to the scanner MDA at 5TP30 is +0.8V at scanner servo lock.

Test point 5TP30 is at +6V when the scanner is started. This output overdrives the scanner motor to lock speed. Since the motor cannot withstand overdrive voltage for very long without damage, runup time to lock speed is monitored, and excessive runup time (system code 11) causes the motor to be turned off.

When the scanner motor is turned off, the scanner servo output to the MDA (5TP30) goes to -5.2V.

Operation of the scanner MDA is explained in detail in paragraph 7-5, Part II.

5-62 Capstan Servo

The capstan tach, capstan servo circuits on PWA5, and the MDA are shown in Figure 5-12.

5-63 Capstan Tach

Capstan tach is composed of the tach sensor housing, the tach disk on the capstan motor, and the Capstan Tach PWA. The tach sensor housing is a caliper with two LEDs (CR1/CR2) on one side and two phototransistors (Q1/Q2) on the other side. The tach disk, which passes through the space between them, is composed of two rows of concentric, radial light barriers. Light barrier rows are offset by 90°.

Phase 1 and 2 tach outputs of the sensor housing are processed on the Capstan Tach PWA to provide a single tach output frequency and a logic level which denotes tape travel direction. Waveforms of the phase 1 and 2 inputs can be optimized with R2 and R3 (see paragraph 5-137). A mechanical adjustment is provided for the 90° phase offset between the phase 1 and 2 inputs (see paragraph 5-138).

The single tach output and the capstan direction logic level are routed to the capstan servo through connector contacts 81 and 83 of the Servo PWA. The direction signal is low when the tape travel is forward and high when it is in reverse. Tach output frequency is 1624 Hz at play and record speed for 525-line video (1591 Hz for 625-line video).

5-64 Inner Loop Reference

Instantaneous capstan motor speed is governed by driving the capstan so that tach frequency coincides with the CPU-generated inner loop reference (ILR) frequency. The ILR frequency is generated as follows.

Reference 4 MHz from the reference pulse generator on the AST Servo PWA (Figure 5-9) is applied to divider 5U22-8. The reference 2 MHz output of 5U22-8 clocks ILR divider 5U23-13 which is permanently enabled. The servo system CPU loads a preset count in 5U22-13 during each vertical interval via the data bus. As the ILR divider is clocked through full count, the output at 5U23-13 clocks divider 5U22-6. The divider output (5TP3) is the ILR frequency. Thus, the ILR frequency is continuously variable at vertical rate. The CPU calculates reference frequency based upon parameters of the commanded mode, mode change commands, and mode control qualifiers (see paragraph 6-7 in Section 6), and the digitized value of the tape speed (shuttle/variable play) control analog output.

ILR frequency and capstan tach outputs are applied to quad latch 5U50. Latch circuits are clocked by 1-MHz E pulses. Latch outputs and tape direction logic level are routed to the combinational network composed of AND and exclusive OR gates 5U52, 5U53, 5U59, 5U60, and 5U75. These gates control the enabling and count direction of two 4-bit up/down counters, 5U28 and 5U29. The instantaneous count contents of these counters is the digital equivalent of capstan velocity error. A half-scale count of 8 in counter 5U28 is the equivalent of zero velocity error.

5-65 Tach/Reference Comparison

Count direction of up/down counters 5U28 and 5U29 is governed by the output of gate 5U52-10 (high = count up, low = count down). These counters are also clocked by 1-MHz E pulses. The up/down counter enable and gate inputs (pins 10 and 7) must both be low to permit counting. The output of inverter 5U75-3 inhibits counting as long as tach and ILR frequency coincide at exclusive OR gate 5U59-6. When one leads the other, counting is enabled. When in velocity lock, the counter toggles around the half-scale count of 8. The gate input of 5U28 remains high unless counter 5U29 is driven to full count. The carry output of 5U28 (pin 15) goes low, enabling 5U29 (at pin 10) when 5U28 reaches full count. If 5U29 reaches full count, all further counting is inhibited. Contents of the up/down counters are applied to digital-to-analog converter (DAC) 5U30. The DAC output is applied through integrator 5U21-7 to two parallel amplifiers: high-gain amplifier 5U16-7, and low-gain amplifier 5U16-14.

5-66 High/Low Gain Selection

The CPU applies two commands to the capstan servo through output data latch 5U78: C1 and C6. C1 selects either high- or low-gain amplifier (high = high-gain, low = low-gain). C1 is high when the VPR-80 is in record mode, play mode, or when higher than normal play speed is commanded in variable play mode. High-gain amplifier 5U16-7 (gain of 2) is selected by closing switch 5U15-15. At the same time C1' (which is C1 inverted) opens switch 5U15-13, cutting off the output of low-gain amplifier 5U16-14.

C1 is low when the capstan motor is running up to speed and when slow-motion is commanded when the VPR-80 is in variable play mode. When C1 is low, low-gain amplifier 5U16-14 (gain of one-sixteenth) is connected to the capstan servo output through switch 5U15-13, and the output of high-gain amplifier 5U16-7 is cut off by switch 5U15-15.

The level of C1' at inverter 5U14-6 controls the presetting of counter 5U29. When C1' is low (high gain is selected), a half-scale count of 8 is preset in both 5U28 and 5U29. When C1' is high (low gain is selected), a count of 8 is preset in counter 5U28 only.

The C6 command from the CPU (high = capstan servo enabled, low = capstan servo inhibited) is high when the VPR-80 is in any mode except stop or shuttle. Thus, switch 5U15-12 is closed, connecting the output of either the low- or high-gain amplifier to the capstan servo output. The C6 commands also loads the half-scale count of 8 in counter 5U28, regardless of gain selction by C1.

5-67 Tach Filter

At record and normal play speeds, analog output of DAC 5U30 contains a ripple caused by tach frequency (1624 Hz or 1591 Hz). The notch filter composed of 5U21-7, 5R137, 5R54, 5R53, 5C5, and 5C23 is provided to minimize the tach frequency component in the capstan error output signal at 5TP17. Adjustment of the capstan tach filter with 5R137 is explained in paragraph 5-139.

5-68 Capstan MDA

Operation of the capstan MDA is explained in paragraph 7-4 in Section 7. The capstan motor is not braked dynamically. The motor is stopped when the capstan servo momentarily generates an error output that causes a reverse drive current to be applied to the motor.

5-69 AST Servo

When the scanner is turning at lock speed (3600 or 3000 rpm), the video record/play head is applying 1000 Gs of force on a tape track 5 mils (0.127mm) wide and almost 17 inches (43 cm) long. In normal play mode and with the scanner and capstan servos in both phase and velocity lock, the head completes the playback of one helical track (one field) and is relatively moved to begin playback of the next field on the following track. In terms of time, the move from one track to the next occurs during the vertical interval. In terms of space, the move occurs when the omega-wrapped tape is not in contact with the scanner. Head-to-tape speed is the sum of the servo-locked tape and head (scanner) speeds. Therefore, at normal play tape speed, mistracking error is limited to a function of head wear and scanner geometry.

If, however, tape speed is reduced from normal play speed to still-frame playback, the head-to-tape speed is reduced until it is composed solely of the head speed. Without Automatic Scan Tracking (AST*), the result is inevitable mistracking as shown by the heavy black line in Figure 5-19. Without AST, the head travels farther into the guardband as tape speed is reduced, and helical noise bars appear in the picture.

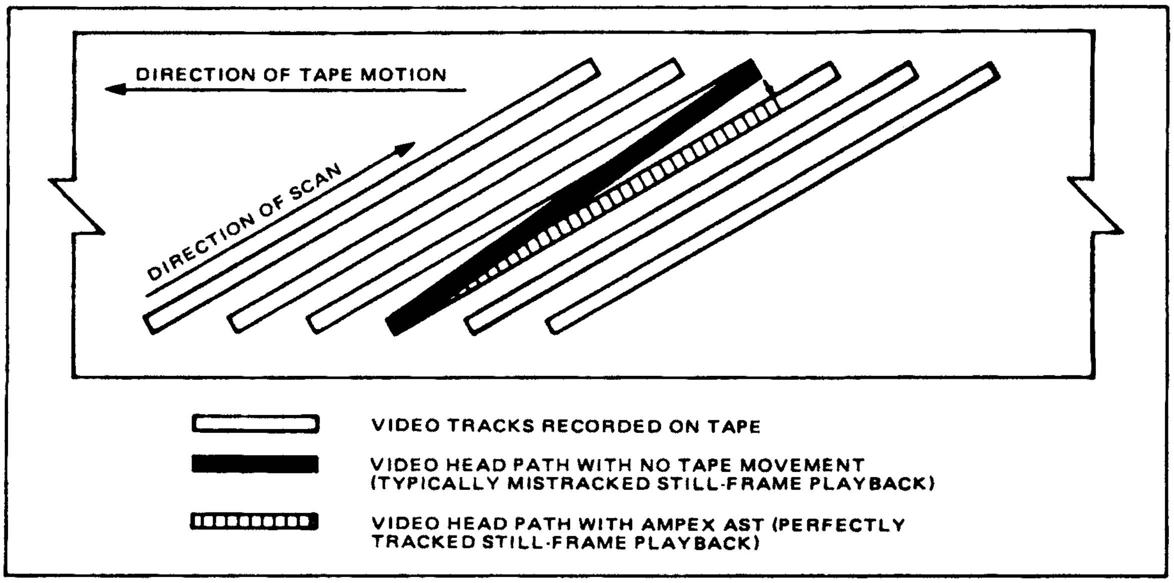

DIRECTION OF TAPE MOTION
DIRECTION OF SCAN
VIDEO TRACKS RECORDED ON TAPE
VIDEO HEAD PATH WITH NO TAPE MOVEMENT (TYPICALLY MISTRACKED STILL-FRAME PLAYBACK)
VIDEO HEAD PATH WITH AMPEX AST (PERFECTLY TRACKED STILL-FRAME PLAYBACK)

Figure 5-19. Type C Helical Video Head Paths

The AST servo keeps the video head in the center of the helical track by flexure of the bimorphic deflector element upon which the head is mounted. The deflector element is composed of layers of piezoelectric ceramic bonded in a sandwich-type construction on each side of a brass (ground) electrode. Gold plated nickel electrodes are bonded to outside surfaces of the piezoelectric ceramic layers. A sectional view of this construction is shown in Figure 5-20. The ceramic layers (and

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*TM Ampex Corporation

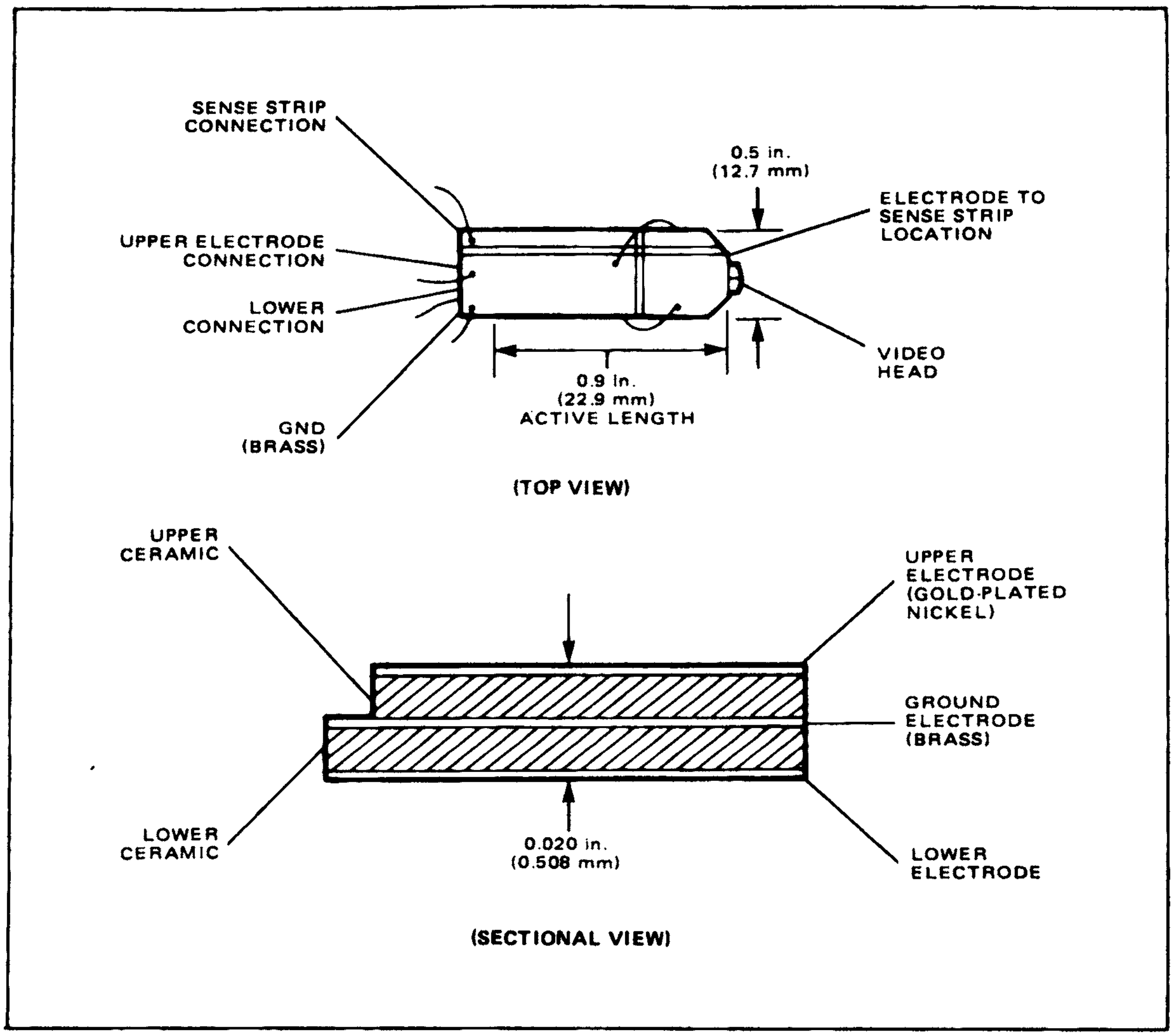


Figure 5-20. Bimorphic Deflector Element Construction

their electrodes) bend when voltage is applied. Thus, the head, affixed to the bimorphic element, is caused to deflect and thereby describe a different track. The head can be deflected 0.5 mm, or ± one track. When the head reaches the limits of deflection, the AST servo causes the head to jump to the adjacent track during the next vertical interval, and color framing is maintained.

Tracking guidance is provided by dithering the head and comparing the dither phase with the amplitude and phase errors of recorded video. Both error amplitude and direction are determined without impairing the video signal.

An exploded view of the Ampex AST head assembly is shown in Figure 5-21. Note that both upper and lower nickel electrodes are split lengthwise and across the width. The wider lengthwise portion is used to deflect the head. The narrow legthwise portion is the sense strip which indicates the degree of deflection to the AST servo and also provides a means of electrical damping.

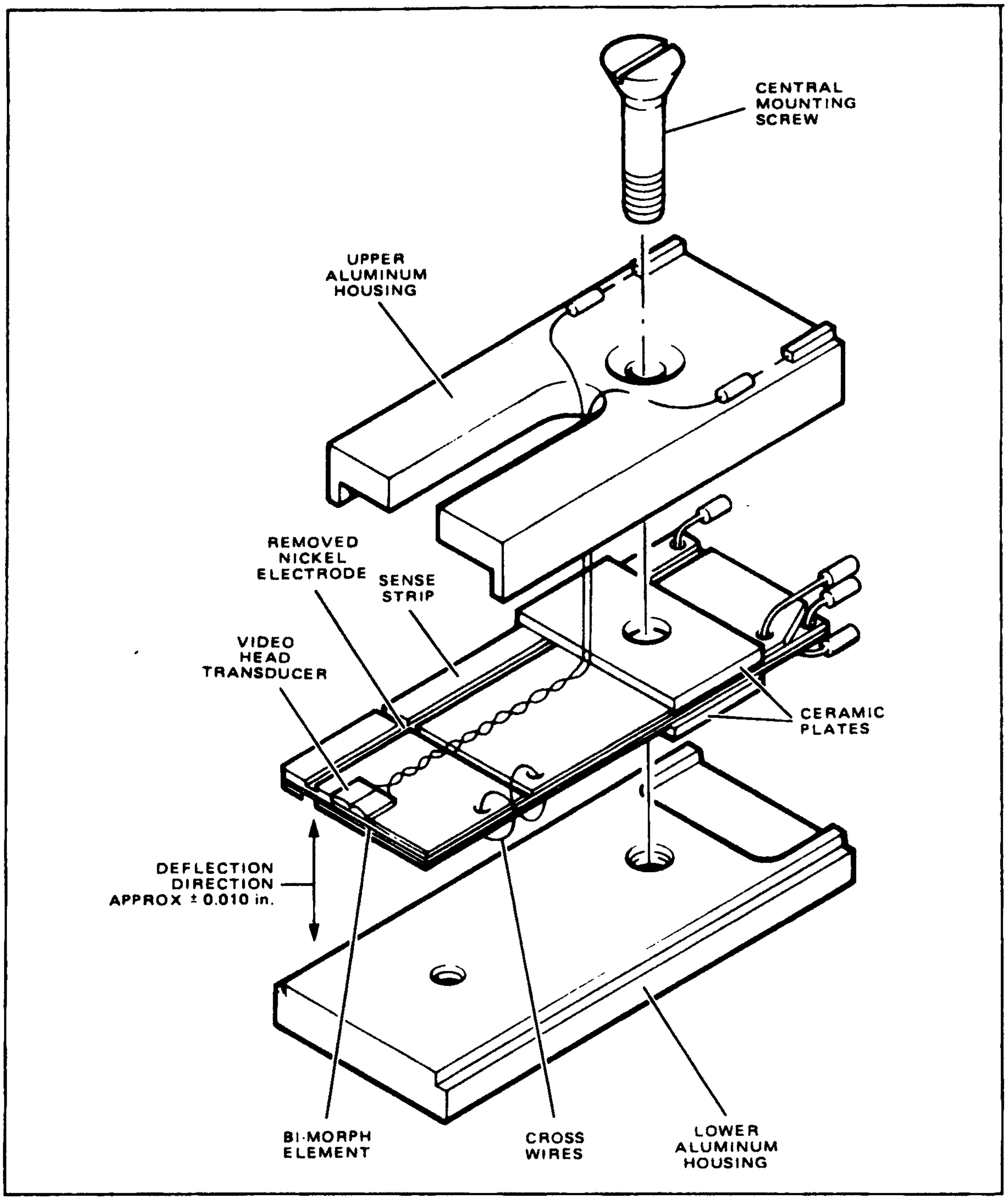


Figure 5-21. Exploded View of AST Head Assembly

At normal playback speeds the AST element theoretically does no work. However, as an AST element (and head) deflect to extremes in slow-motion playback, zenith errors appear. The head begins to lose contact with the tape as the element is deflected. Therefore, the nickel electrodes are split crosswise and inputs to electrode segments near the head are reversed. Thus, the element articulates in an "S" curve as it deflects. This recurving maintains correct head-to-tape contact at all degrees of flexure.

The piezoelectric elements must be polarized, and in normal operation positive and negative voltages cause up and down deflection. To prevent depolarization, a separate deflection voltage of the proper polarity is used for each electrode of the bimorphic deflector. This insures that piezoelectric elements are never driven in the opposite direction of polarization.

The AST servo is three servos in one. The first is a static (dc) servo which takes care of elevation differences between record and reproduce heads. The second is for dynamic (ac) correction, which actively follows the video track. The third is look-ahead logic which compares the instantaneous head position with the next position. This logic decides when it is time to leave one track and jump to the next track in the vertical interval.

5-70 General

The VPR-80 AST servo is composed of logic on the AST Servo PWA, the AST Driver PWA, and the single AST head assembly on the scanner. RF amplitude and dropout information are supplied by demodulator and dropout detector circuits on the Mod/Demod PWA. The AST servo is diagrammed in Figure 5-22 which also shows the analog multiplexer, A/D converter, bidirectional data buffers, and CPU on the Servo PWA.

The AST playback head assembly is vibrated transversely to the tape track (dithered) at 450 Hz (525-line video) or 425 Hz (625-line video). This modulates playback rf to provide tracking error information. Playback rf is routed to the Preamplifier PWA, the Mod/Demod PWA, then to the AST Servo PWA. Tracking error detection is accomplished by envelope detection and then synchronous detection (sampling) at the dither frequency. The error signal is passed through a low-pass filter to provide a dc-error component, which is then applied to the AST head through error integration circuitry. The low-pass filter output includes ac dynamic tracking error components. The servo system CPU analyzes the composite error signal and provides both ac and dc corrections to the servo through D/A converters. The dc error component corresponds to the general track angle and average tracking error. The ac component corrects errors in the helical track straightness. The ac error is associated with tape interchange and repeats synchronously with each revolution of the scanner.

Ac and dc analog correction signals are summed with the dither frequency and with a mechanical damping component. The resulting servo correction signal is applied to the AST Driver PWA. This PWA provides drive to the flexure element to correct head position and to maintain dither frequency vibration. The sense strip on the flexure element provides a velocity signal for the AST Driver PWA to facilitate electronically damping mechanical resonance of the flexure elements. Paragraphs 5-70 through 5-77 provide background information on basic AST concepts. Paragraphs 5-78 through 5-95 describe various circuit functions of the AST servo.

The following mnemonics (which have not been previously identified in connection with another servo) are used on Figure 5-22:

AC—AC error

A3—Forward/Back (over/under play speed)

A5—Track jump enable

B7—AST enable/inhibit (high = AST operation enabled, low = AST operation inhibited

DC—DC error

DI—Dither (450 Hz for 525-line video; 425 Hz for 625-line video)

DO—Vertical dropout

ON—AST control (high = AST off, low = AST on)

VR—Reference voltage for ± drive centering on AST Driver PWA

5-71 Error Detection

A decrease in the video rf envelope indicates that the head is off track, but it does not indicate the direction of the error. Sinusoidally vibrating the head across the track, at dither frequency, provides direction information.

5-72 DC Error. Figure 5-23 shows the basic dc error detection method for AST tracking errors. With the head on track, the dither signal deflects it off track an equal amount in both directions, and the detected rf envelope is the same for each half cycle of dither frequency. This signal is then synchronously detected at dither frequency; polarities of alternate half-cycles are reversed synchronously with polarity changes in the dither signal. The resulting error waveform is passed through a low-pass filter to eliminate the dither component and provide an average dc error value. With the head on track the error is zero.

With the head to the right of the track, it will be deflected for a greater average error to the right side, than to the left, resulting in a filtered dc error component. With the head to the left of the track, deflections will cause an average dc error of opposite polarity. See paragraph 5-85.

5-73 AC Error. The composite error signal contains errors of a dynamic nature which are the result of tape interchange (playback of a tape recorded on a different VTR). These errors are caused by slight mechanical differences between the record VTR and the scanner of the playback VTR. This component, termed ac error, recurs regularly with each revolution of the scanner. Thus, ac errors appear at field rate and its harmonics. The ac error changes over the period in which the head is scanning each field track, but the pattern of ac errors is repetitive from one field to the next with only minor fluctuations. See paragraph 5-86.

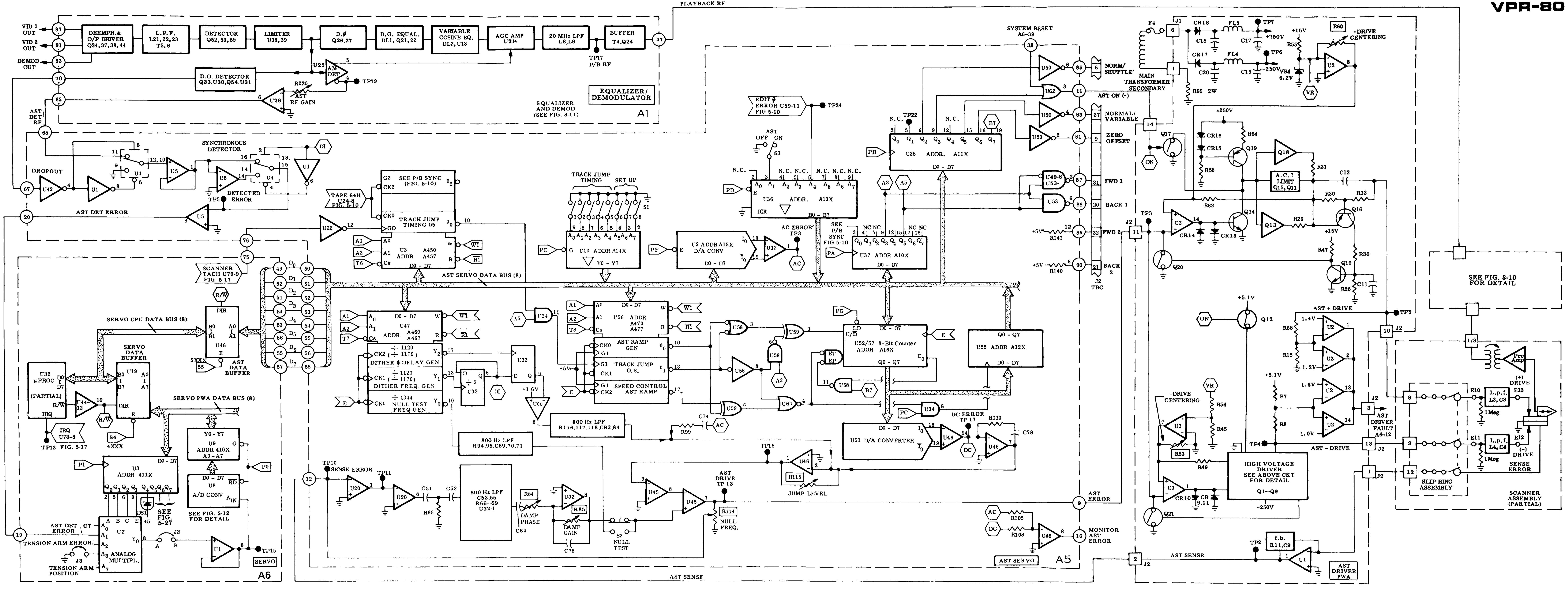


Figure 5-22.
AST Servo (PWA4) and AST Driver PWA

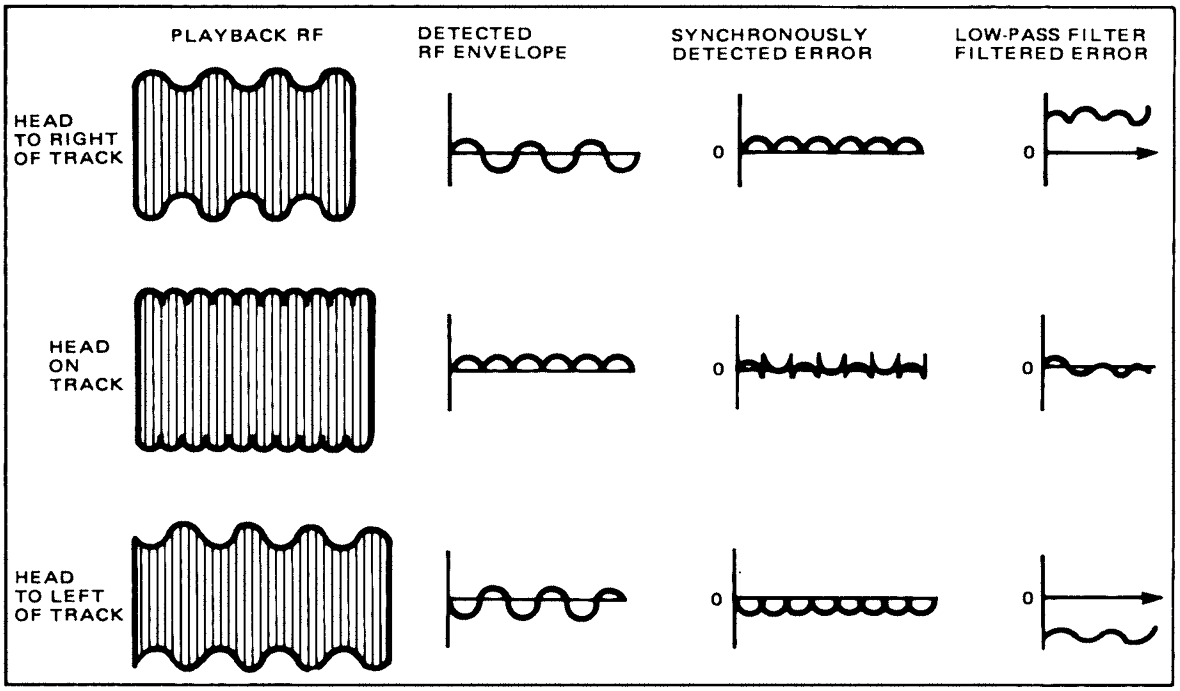


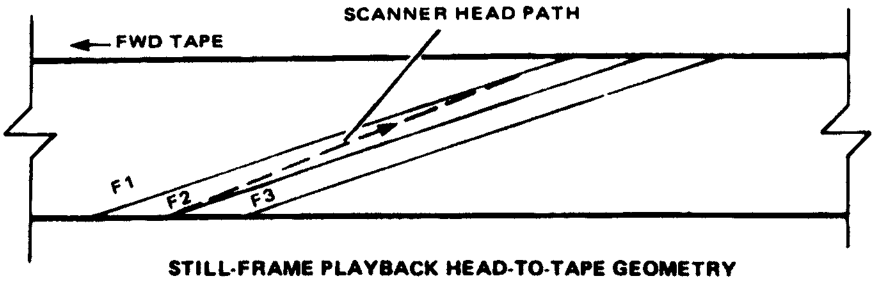
Figure 5-23. Detecting AST DC Error

5-74 AST Head Deflection

Figure 5-24A shows head-to-tape geometry considerations for still-frame operation. F1, F2, and F3 denote recorded field tracks. The dotted line is the path of the scanning head, in the direction indicated, with tape stopped and AST system disabled. During normal speed play, tape moves at a velocity that keeps track F2 coincident with the dotted line scanning path. In still-frame operation the head must be moved toward F2 at the rate of one track-to-track distance per scan, to stay on track. When the head reaches the end of the F2 track, it must be reset to its original position before starting the next scan of F2. This is done during vertical interval dropout.

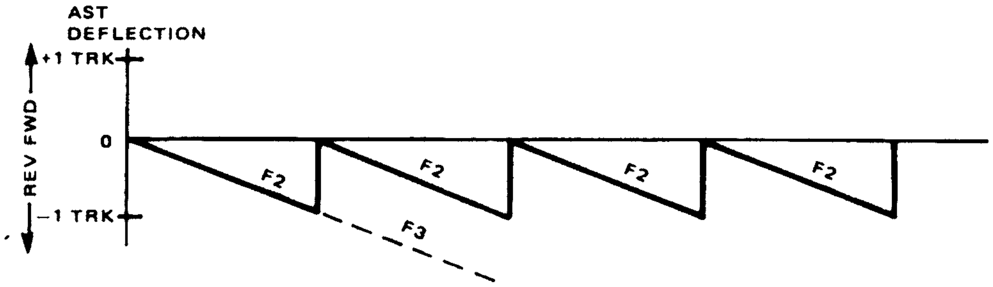
5-75 **Still-Frame Playback.** Figure 5-24B shows head deflection which is opposite to tape direction, for keeping the head on the F2 track in still-frame operation. A digital ramp generator provides the sawtooth drive signal for this deflection. At the end of each field scan of F2 the head must be reset by one track or it would start the next scan at the F3 track.

5-76 **Slow-Motion Playback.** Figure 5-24C shows head deflection for 1/5-speed, slow-motion playback. Slope of the deflection is only 80% of that for still-frame operation, as the track moves 0.2 of a track-to-track distance per scan. However, a reset deflection is always a full track-to-track distance. Therefore the deflection path gradually moves upward in the direction of tape movement. Finally, the F2 track has moved as far as the head deflector is able to track it. The AST track reset logic in the CPU checks about 1 ms before the end of each track scan to see if correction voltage is greater than zero. When it is, reset is inhibited and the head moves on to scan F3.



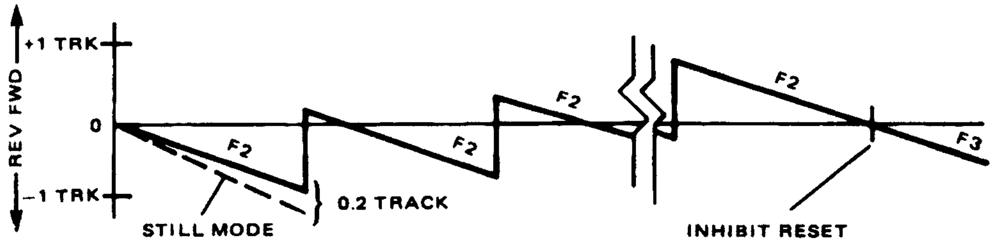
STILL-FRAME PLAYBACK HEAD-TO-TAPE GEOMETRY

A



STILL-FRAME PLAYBACK HEAD DEFLECTION

B



ONE-FIFTH PLAY SPEED HEAD DEFLECTION

C

Figure 5-24. Head-to-Tape Geometry and Head Deflection

5-77 Fast Playback. For forward speeds greater than X1, deflection slope in the forward direction is needed. For a X1.1 speed, for example, slope will be gradual and about 10 tracks will be scanned before the head deflection limit is reached. The CPU initiates a one-track reset in the opposite direction when the plus one track limit is reached.

5-78 AST Interrupt

Refer back to Figure 5-5 which is the servo system interrupt generation flowchart. The AST interrupt occurs at a rate of 900 Hz (525-line standard) or 850 Hz (625-line standard) which is twice the dither frequency. AST interrupts are inhibited by the undelayed scanner tach interrupt until completion of the delayed scanner tach interrupt service routine, as explained in paragraph 5-36.

During an AST interrupt, CPU 5U32 samples the following values via multiplexer 5U2 and A/D converter 5U8:

- Control track error: see paragraph 5-47
- AST detected error: see paragraph 5-83
- Tension arm error: see paragraph 5-96
- RF amplitude: refer to paragraph 3-33
- Capstan error: see paragraph 5-47
- Tensión arm position: see paragraph 5-96

In addition, CPU 5U32 samples tape pack diameters and tape speed (see paragraph 5-96). Once per field the CPU also enters new values (based on AST track jump information) into playback sync processor one-shots which control TBC vertical and vertical blanking pulses (see paragraph 5-91).

5-79 Dither Generation

Dither frequency for 525-line video is 450 Hz, and for 625-line video, it is 425 Hz. Two dither frequency signals are generated: one drives the synchronous switch, and the other (90° phase shifted) is the dither component of the AST error output which drives the AST head flexure element.

Timer 4U47-13 and divider 4U33-6 (shown in Figure 5-22) compose the dither frequency generator for driving synchronous detector switch 4U4-13/-15. Timer 4U47-13 divides E pulses from the servo system CPU by either 1120 (525-line standard) or 1176 (625-line standard). Flip-flop 4U33-6 then divides the output of 4U47-13 by two to the dither frequency (DI). The DI signal drives switch 4U4-13/-15 which first routes the uninverted AST detected rf signal and then the inverted signal to the Servo PWA for digitizing and examination by the CPU. See paragraph 5-83.

Timer 4U47-17 and divider 4U33-9 compose the dither phase delay generator for driving the AST flexure element. These components operate in identical fashion as timer 4U47-13 and divider 4U33-6. Dither output at 4U33-6 is routed through 4U60-8 and low-pass filter 4R116--118/4C83/4C84. These components shift the dither frequency signal 90° and convert the signal from square wave to sine wave. The signal is inserted in the composite AST error output signal to deflect the AST head assembly sinusoidally.

The E pulse rate is 64H. In 525-line standard, H = 15734.264 Hz, and 64H = 1006992.8 Hz (nominal 1 MHz). Thus, for 525-line video, 64H divided by 1120 = 899.1 Hz which when divided by 2 = 449.55 Hz. This is the nominal 450-Hz dither frequency for 525-line video.

In 625-line standard, H = 15625 Hz, and 64H = 1 MHz. Thus, for 625-line video, 64H divided by 1176 = 850.34 Hz, which when divided by 2 = 425.17 Hz. This is the nominal 425-Hz dither frequency for 625-line video.

5-80 Synchronous Error Detection

The AST-detected error signal is derived from the playback video rf envelope. A detector switch, driven by square wave dither pulses, samples the output of an AM detector in both inverted and noninverted form. The AST error signal, thus inverted on each half of the dither cycyle, is examined by the CPU at twice dither rate.

5-81 **AM Detector.** As shown in Figure 5-22, the playback rf signal from the Preamplifier PWA and Record Amplifier and Edit Erase PWA is routed to connector contact 47 of the Mod/Demod PWA. It is first buffered by 1T4 and 1Q24. The signal at test point 1TP27 is the monitoring point for the VIDEO/RF meter. The signal at this point is also routed to the Reference PWA as playback rf level.

After buffering, playback rf is applied to the low-pass filter composed of 1L8, 1L9, 1C91—1C95, and 1T3. This filter eliminates frequencies above 14.5 MHz which are noise from the scanner and are not part of the off-tape rf signal. Filtered rf is then routed through the AGC amplifier, equalizers, and dropout detector to AM detector 1U25.

Detector 1U25 detects peaks of the rf envelope and furnishes dc outputs. The output at 1U25-5 is fed back to AGC amplifier 1U21. This feedback path is closed during the scan of each video track, but is switched open during dropout intervals. Otherwise, a loop transient would occur as the envelope detector tried to follow the dropout pulse. Inverted output at 1U25-4 (1TP19) is applied through 1R220 and 1U26-6 to synchronous detector switch 4U4-13/15 through dropout switch 4U4-10/-12 on the AST Servo PWA. RF output to dropout and synchronous detector switches is a 3.5-Vp-p signal. The rf gain is adjusted to this level by 1R220.

5-82 **Dropout Switch.** Dropout detection signal output at connector contact 70 of the Mod/Demod PWA is a TTL low. The dropout signal is applied to the two driving inputs of analog switch 4U4-10/12. Thus, AST-detected rf output of 1U26-6 is grounded by switch 4U4-10/-12 during every dropout interval. This prevents the large dropout transition from being applied to buffers 4U5-1/-14 and the synchronous detector. The dropout detection signal is also routed to the TBC (as shown in Figure 5-10).

5-83 Sample Pulse Generation. The dither (DI) output of divider 4U33-6 is applied to the two driving inputs of synchronous detector switch 4U4-13/-15. AST-detected rf output of dropout switch 4U4-10/-12 is applied through 4U5-1 to one signal input side of switch 4U4-13/-15. This is the noninverted signal. AST-detected rf output of 4U5-1 is inverted by 4U5-14 and applied to the other signal input side of switch 4U4-13/-15. Thus, the polarity of the AST detected rf is inverted on every half cycle of dither. This chopped signal is the AST DETECTED ERROR (4TP5) which has both ac and dc components. It is inverted by integrator 4U5-8 and routed to the Servo PWA.

AST interrupts are generated at twice dither frequency. Therefore, the AST-detected error is sampled twice during each dither cycle. Noninverted and inverted segments of the integrated error signal are sampled by multiplexer 5U2, digitized by A/D converter 5U8, and placed on the Servo PWA data bus for examination by CPU 5U32.

5-84 Error Signal Generation

Most of the timing and calculations involved in generation of the AST error output voltage to the AST Driver PWA are controlled by the servo system CPU and its firmware. Therefore, Figure 5-22 shows only hardware-controlled functions which affect error output.

There are three primary components of the composite AST error output signal: ramp, position error, and dynamic error. Each of these components is independently determined. The ramp is an open-loop sawtooth waveform which is based solely on tape speed. Position error and dynamic (or ac) error are generated by the CPU and are based on AST-detected error.

Error output also includes dither and sense error, but they are not part of track position correction. Dither is a driving signal which is discussed separately in paragraph 5-79. The sense error is produced by an inner servo loop which is solely for compensation of the AST deflector element. The sense error loop is explained in paragraph 5-87.

All sampling of head position with respect to the helical track is done by the synchronous detector (paragraph 5-80). This sampling is done at twice dither rate, and samples are digitized for examination by the CPU.

Absolute value of the commanded head position is represented by the instantaneous count (000--255) contained in up/down counter 4U52/57. Counter contents are sampled by the CPU via input data latch 4U55. The sampling rate is 14 samples per field period for 525-line video or 16 samples per field period for 625-line video.

5-85 DC Error. The dc error is made up of the first two components of the AST error signal: ramp and position error. Ramp signal and position error are both generated by the CPU and manifested in the contents of up/down counter 4U52/57. Contents of counter 4U52/57 are the digital representation of instantaneous dc error.

The servo system CPU generates the digital ramp which (with position error corrections) describes the AST dc error over the scan of each helical track. The origin of the ramp is established by presetting counter 4U52/57. The origin of the ramp and its slope angle are based solely on tape speed information from the tape speed counter in the reel servo. See paragraph 5-100 and Figure 5-27.

Counter 4U52/57 is enabled by two logic lows (ET and EP) at its enable input AND gate, and it is clocked by E pulses. Up/down count direction is governed by the logic level of the A3 output of data latch 4U37-9. When high, A3 indicates that tape speed is higher than normal: when low, A3 indicates slow-motion playback.

The EP enabling input is low as long as the counter has not reached a full count of 255 and as long as the B7 output of data latch 4U38 is asserted (high). The B7 logic level is high except when AST operation is turned off, either manually with switch 4S3 or by the CPU based on mode of operation (edit play or record). This is one of many on/off control inputs to the AST servo.

The ramp is constructed by the AST ramp generator, the speed control timer (4U56-10/-17), and their associated output gating network. These circuits control the logic level at the ET-enabling input of 4U52/57. Values preset in these timers are determined by the CPU and are based upon tape speed. Ramp generator circuits have no knowledge of either head position or error. Their only controlling input is tape speed.

Ramp generator 4U56-10 and speed control timer 4U56-17 are permanently enabled. Outputs of 4U56-10 and 4U56-17 are applied to exclusive OR gate 4U59-6. The high output of 4U59-6, inverted by gate 4U61-4, enables counter 4U52/57 to count up or down. The output frequency of speed control timer 4U56-17 is directly proportional to the output rate of the tape timer tach. Output frequency of AST ramp generator 4U56-10 is the same regardless of tape speed. Changing contents of counter 4U52/57 are the digital representation of the commanded ramp.

The contents of counter 4U52/57 are applied in parallel to D/A converter 4U51. The analog output of 4U46-14 is the dc component of the AST error output to the AST Driver PWA.

Corrections to the ramp for position error are based on the AST-detected error signal from the synchronous detector. Input data latch 4U55 is clocked 14 (or 16) times per field. Thus, the commanded head position, as described by the contents of 4U52/57, is sampled.

Figure 5-25 shows 14 samples of actual head position with respect to a one-field segment of the AST ramp. Sample times are shown in line A. The 14-head position errors (shown in line B) are averaged by the CPU over the field period. Then, based on the computed average position error, counter 4U52/57 is reloaded with an adjusted value. The position correction word is loaded into 4U52/57 immediately following the last sample in each field. Degree of correction is limited to one bit per field.

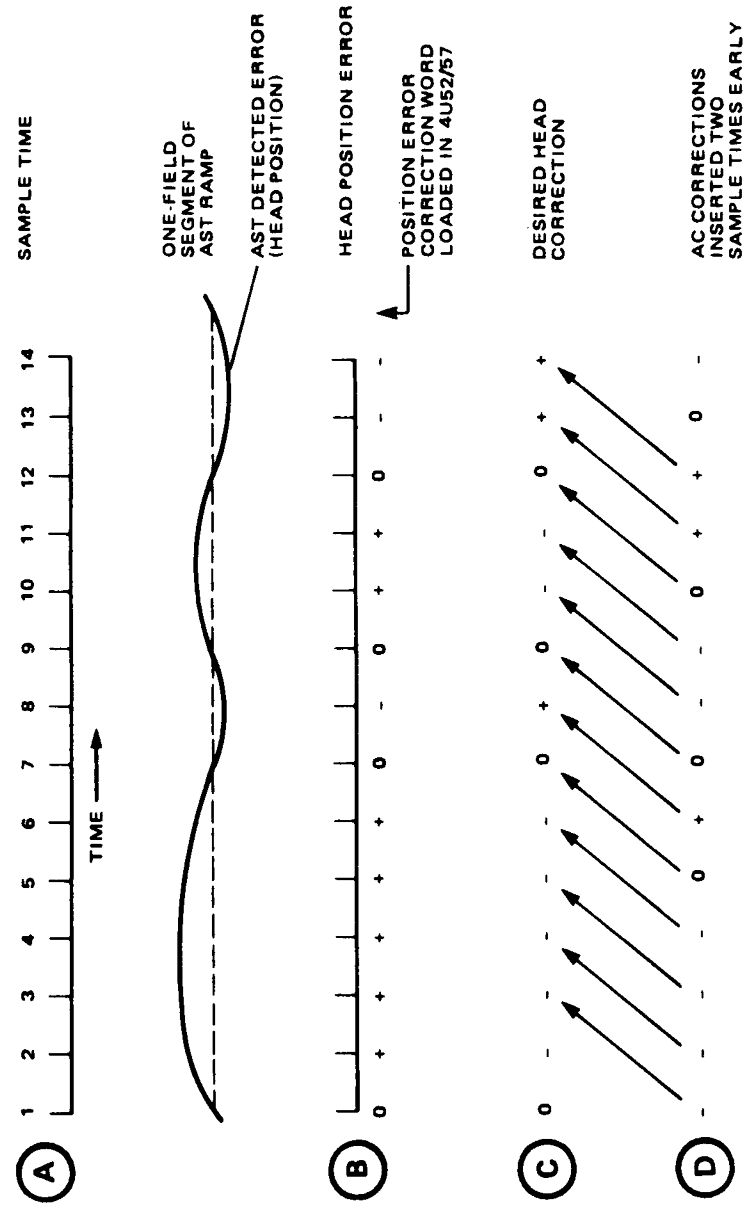


Figure 5-25. AST Position Error and AC Error Corrections

5-86 AC Error. AC error correction is based upon the same 14 (or 16) samples taken for dc error correction; however, samples are handled quite differently. Each error sample is averaged with the corresponding error sample taken over the preceding 15 fields. For example, sample number 7 is averaged with sample number 7 in each of the preceding 15 fields. Therefore, 16 error averages are held in memory and are continually updated to correct track straightness. Track straightness errors do not change significantly from field to field. They are mechanically induced, and the pattern repeats at field rate with only minor fluctuations.

AC corrections for each sampled point in the field, based upon an average of errors at the same point in each field period, are generated by the CPU. Correction words are written into D/A converter (DAC) 4U2 which injects a corresponding analog voltage into the composite AST error output up to 14 (or 16) times per field. Insertion of ac error correction voltage is made at 4U46-2.

The deflector element cannot be expected to respond instantaneously to an ac correction. Some lead time is required to allow the deflector element to respond, and, fortunately, the repetitive nature of track straightness errors enables a look-ahead capability. Therefore, the CPU writes each ac correction word into DAC 4U2 two sample times ahead of the sample time for which the average error is calculated. This is shown in line D of Figure 5-25. Thus, predicted track straightness error is simultaneously offset by ac correction.

5-87 Sense Error

Sense error return from the AST head is fed back through the AST Driver PWA to connector contact 12 of the AST Servo PWA. The AST sense error feedback loop from the sense strip on the deflector element is an inner damping loop to minimize mechanical ringing of the deflector element. It is not part of head position correction.

The sense error feedback loop will oscillate on its own unless properly compensated. Therefore, null frequency, gain, and phase adjustments are provided for loop compensation. Because of very slight physical differences in each AST head (resulting in slight differences in mechanical resonance), these compensation adjustments must be checked and readjusted whenever an AST head is replaced.

The AST sense error signal (4TP10) is buffered and inverted twice by 4U20-1/-8. It is then applied to a lead network for phase compensation (4C51/4C52/4R65). Output of this network is applied to an 800-Hz low-pass filter composed of 4U32-1 and associated components. The filter applies electronic damping for the mechanical resonance of the AST deflector element. It is an active implementation of a low-pass filter. Filter output is routed through 4R84 (damping phase adjustment) to integrator 4U32-8. Potentiometer 4R85 in the integrator feedback path is the damping gain adjustment. Output of 4U32-8 is applied, through null test switch 4S2, to 4U45-7 where it is summed into the composite AST error output to the AST Driver PWA.

The sense error signal input is also routed to the wiper of null frequency adjustment 4R114. Timer 4U47-10 counts 64H (E) pulses down to a nominal 750-Hz output (749.25 Hz for 525-line video, or 744.0 Hz for 625-line video). The 750-Hz output is applied to a 800-Hz low-pass filter which converts the square wave output to near sine wave. When null test switch 4S2 is pressed, the 750-Hz signal is inserted in the AST error output in place of the sense error feedback signal. Null frequency adjustment 4R114 is used to minimize amplitude of this signal at 4TP11 (buffered sense error input). This adjustment must be made before adjustment of damping phase (4R84) or damping gain (4R85).

Figure 5-26 shows an idealized open-loop frequency response curve of the AST head assembly in which first- and second-order resonances occur at 400 Hz and 2.5 kHz, respectively, and null is at 750 Hz. The damping loop is designed to minimize mechanical ringing of a head assembly with these ideal characteristics. Resonant and null frequency responses vary between individual head assemblies. Therefore, injecting a 750-Hz test signal and then adjusting the open-loop null response artificially moves the entire frequency response curve of a replacement head assembly to match the idealized curve.

After the null frequency adjustment has been made, interactive gain and phase adjustments of the loop can be made. (See paragraphs 5-129 and 5-130.)

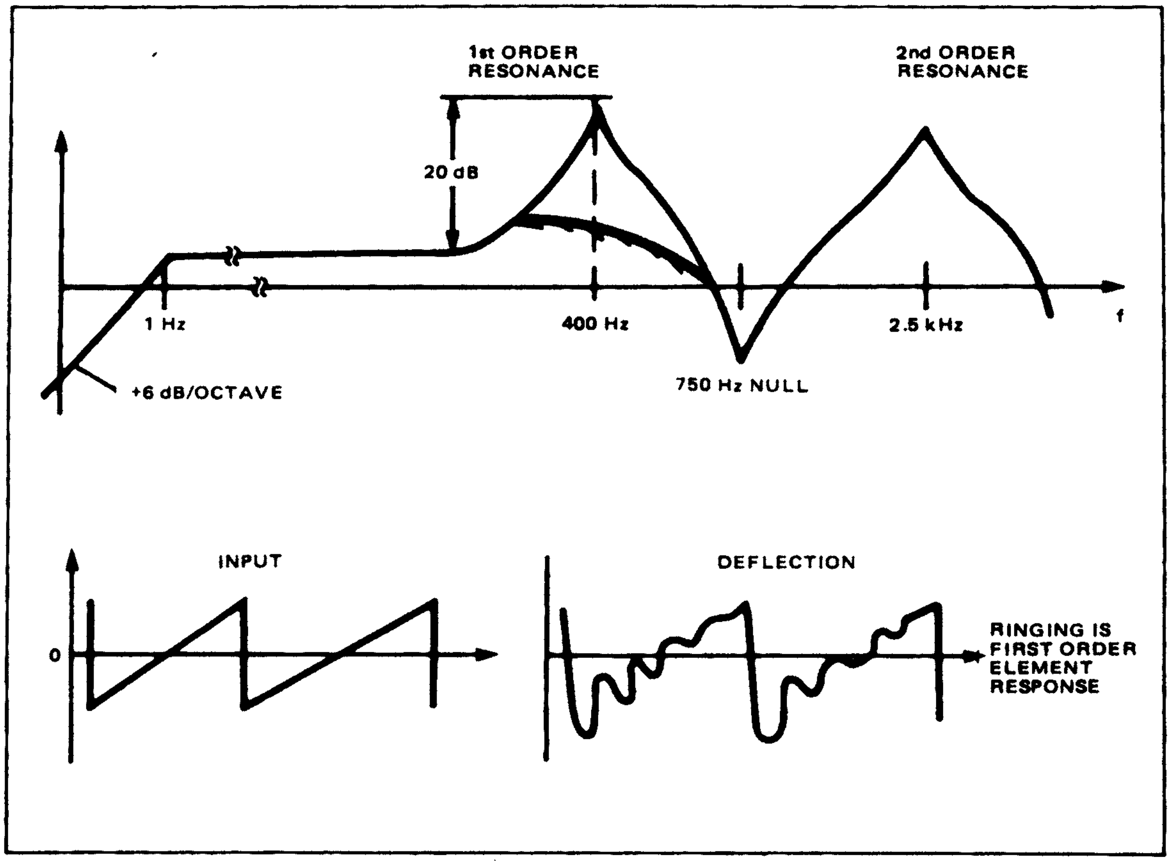


Figure 5-26. Ideal Open-Loop Frequency Response of AST Head

5-88 Track Jump Logic

Almost all track jump logic is managed by the servo system CPU, 5U32, and consequently there is very little hardware-implemented logic which can be shown in Figure 5-22. The track jump logic decides when a jump is necessary, exactly when to make the jump (in which specific vertical interval), and how far (how many tracks) to jump. The CPU also manages coordination of the track jump with the time-base corrector and the playback sync processor.

Every number in the necessary computation (except scanner speed) changes over tape speed range from still-frame playback to 1.5X normal play speed. In still-frame playback, the same basic ramp is repeatedly contructed as the same helical track is played continuously. At faster than normal play speeds, tracks are skipped, and in slow-motion playback, the same track is played a number of times inversely proportional to the tape speed. In each case, the CPU must calculate the rate of track jump to maintain usable playback video rf.

5-89 **Track Jump Control.** The 8-bit word in up/down counter 4U52/57 is the digital representation of AST head position at any given time. CPU 5U32 samples the head position word in 4U52/57 either 14 times per field (525-line video) or 16 times per field (625-line video). Sampling is done by clocking input data latch 4U55 through gate 4U34-8.

The half-scale count of 128 (80 hex) indicates the center position of the AST head. Center-to-center distance between adjacent helical tracks is equivalent to 64 bits in the head position word. Thus, the CPU calculates when to jump tracks by comparing the AST head deflection with the AST detected error samples from the synchronous detector.

When the AST head is near its limit of deflection, and AST-detected error indicates diminishing rf amplitude, the CPU causes the A5 output of output data latch 4U37-15 to go high. When A5 is high, a track jump is enabled. A5 is routed to AND gate 4U34-11. Track jump is initiated when timing logic (track jump timing one-shot 4U3-10) supplies the other high input to AND gate 4U34-11 at the calculated time.

5-90 **Track Jump Timing.** The output period of track jump timing one-shot 4U3-10 determines when track jump will occur. The output period of track jump one-shot 4U56-13 determines how far the AST head will jump.

The JUMP LEVEL control, 4R115, provides an analog adjustment of how far the AST head will jump in response to commands from the AST servo digital logic. This control provides a linear gain adjustment of the AST error output to the AST Driver PWA. Adjustment of 4R115 is made while observing the playback rf envelope. The jump track gain adjustment procedure, which is spelled out in paragraph 5-131, ensures that the AST head will be centered on the next helical track after a track jump. Adjustment of 4R115 must be made before making digital adjustment of jump track timing.

The output period of one-shot 4U3-10 depends in part upon the setting of sections 1—5 of TRACK JUMP TIMING switch 4S1. Sections 1—5 of 4S1 are used to construct a 5-bit word in which each bit (switch) is worth one line period (H). The CPU reads the setting of the TRACK JUMP TIMING switches by addressing input data buffer 4U10. The procedure for setting these switches while observing the playback rf envelope is spelled out in paragraph 5-132.

One-shot 4U3-10 is triggered by the scanner tach flag pulse (S2) from flip-flop 5U79-9 shown in Figure 5-17.

The maximum delay value which can be manually entered with 4S1 is 32H, but any manually entered value is combined with other timing offsets calculated by the CPU and loaded into track jump timing one-shot 4U3-10. Calculations which produce the value loaded into 4U3-10 are quite complicated and of academic interest only. The output period of 4U3-10 ranges from one line to almost a full-field period. Length of the one-shot period depends upon whether the calculated track jump time occurs before or after the next scanner tach flag pulse. If the track jump is to occur before the next scanner tach flag pulse, delay is calculated from the previous field. If the track jump is to occur after the next scanner tach flag pulse, delay is simply calculated from the tach flag pulse.

When the output of one-shot 4U3-10 expires (goes high), it triggers the track jump one-shot, 4U56-13 through gate 4U34-11 which is enabled by A5. The output period of 4U56-13 determines how far the AST head will jump. The CPU calculates the necessary output period and loads the appropriate value in 4U56-13 via the AST servo data bus.

Output of one-shot 4U56-13 is applied through the gating network at the count direction and enabling inputs of counter 4U52/57. This causes an appropriate value to be added algebraically to contents of counter 4U52/57 where a jump of one track equals 64 bits. When the digital jump value is algebraically added to the contents of 4U52/57, the analog output of DAC 4U51 and its output circuits 4U46-14/-7 suddenly shifts the AST error output level to the AST Driver PWA, causing a track jump of the commanded distance at the calculated time. Previous adjustment of jump track gain with 4R115 ensures that the AST head will be centered on the new track after a track jump.

5-91 **Playback Sync.** At the time of decision to jump (or not jump) tracks, CPU 5U32 loads new values in playback sync processor one-shots 4U16-17 and 4U41-13 via the AST servo data bus. These one-shots are shown in Figure 5-10. The task of one-shot 4U16-17 is to predict when the second equalizing pulse will occur in the next field.

The value loaded into 4U16-17 is based upon the track jump decision made for the previous field. There are three basic choices, depending on whether no track jump was made, a forward track jump was made, or a backward track jump was made.

The value loaded into one-shot 4U41-13 is based upon more complicated considerations. The value depends on not only what track jump decision was made for the previous field, but also on what jump decision is made for the next field. Combined decisions result in an algebraic sum which is loaded into 4U41-13. One-shot 4U41-13 provides a trigger delay for one-shot 4U41-10. The output of the latter one-shot is the predicted tape (servo) vertical signal which is routed to the time-base corrector and to the demod video sync insertion circuitry on the Reference PWA.

5-92 Color Framing. Edit phase error input from 4U59-11 (Figure 5-10) is routed to input data buffer 4U36. This signal is a comparison of playback frame and reference frame periods. As an exclusive OR gate output, it is low when frame periods are coincident (same level), and it is high when there is no coincidence (different levels). The edit phase error signal serves two purposes.

First, the signal tells the scanner servo how playback video relates to reference video timing. The relationship indicates edit phase error. This information is used by the edit optimize logic. See paragraph 5-95.

Second, the edit phase error signal is used to determine whether the AST head is centered on the correct track (field), thus maintaining proper color framing. The edit phase error signal serves this purpose in normal play mode and following edit optimization. In variable play mode, some fields are repeated (or skipped), and therefore it is understood that incorrect fields will be played periodically. The VPR-80 takes no action on this, and the necessary corrections are applied by the TBC.

After achieving control track lock in normal play mode, the AST head must move to the correct track (field). That determination is made by the edit phase error signal. The width of the pulse indicates timing difference between playback video and reference video timing. The signal at 4TP24 is a pulse 6.5 to 8H (lines) wide, depending upon the particular TBC used. If it is a whole field wide minus the 6.5 to 8 lines, then the AST head is centered on an incorrect track, and there is no color framing. In this case, the SYSTEM indicator will light, and system code **08** (not field matched) will be brought up for display. See paragraph 5-95.

5-93 AST Driver PWA

The AST Driver PWA is mounted behind the control panel assembly as shown in Figure 5-28. The main power transformer supplies high-voltage ac from which the positive and negative (±) AST deflector element drive voltages are derived. As shown in Figure 5-22, the AST error signal and the AST on/off control from the AST Servo PWA enter the PWA at J2-11 and J2-14, respectively. The AST sense feedback signal from the deflector element to the sense error input of the AST Servo PWA simply crosses through the AST Driver PWA where the only circuit actions on it are inversion and buffering.

The VPR-80 power supply transformer furnishes 220 Vac to the AST Driver PWA at J1-1/-6. The ac input is half-wave rectified and filtered. Positive and negative 250 Vac are derived at test points TP7 and TP6, respectively. The dc voltage level tolerance at these points is ±30 Vdc. Separate positive and negative drive voltage centering adjustments are provided. Centering adjustments R60 and R53 are used to provide positive and negative 125 Vdc at TP5 and TP4, respectively. Tolerance on these voltage levels is ±2 Vdc. (See paragraph 5-128.)

AST on/off control input (OR-gated with system reset) from the AST Servo PWA is applied to the bases of transistors Q17 and Q12. AST operation can thus be turned off either manually with switch 4S3, automatically by the CPU depending on mode of operation, or by system reset. When AST operation is turned off, drive voltage modulation by the AST error input is inhibited; however, balanced, static drive voltages remain present on the deflector element.

The (+) drive voltage is compared with a reference voltage by U2-1/-2. The (−) drive voltage is compared with a reference voltage by U2-13/-14, and both comparator outputs are joined at a common summing junction. If either 125V drive voltage exceeds ±2 Vdc tolerance, or if absolute values of positive and negative drive voltages are not within 0.2 Vdc of each other, the logic level at J2-3 (TP1) goes low. This output is routed to the Control PWA. In edit play and record modes, the low comparator output causes fault indication **101-02** (AST driver high voltage fault) to be brought up for display.

5-94 Outputs to Time-Base Corrector

Five of the 10 outputs to the TBC are from the AST Servo PWA. These outputs, shown in Figure 5-22, are:

- Normal/shuttle
- Normal/variable
- Zero offset
- Forward 1
- Back 1

Other outputs to the TBC are:

- Vertical dropout (Figure 5-10)
- Playback vertical (Figure 5-10)
- Dropout (Figure 5-10)
- Tape direction (Figure 6-7)
- Tape tach (Figure 6-7)

The NORMAL/SHUTTLE logic level from output data latch 4U38 via 4U50-6 is not an AST system output, but a control system output. SHUTTLE is asserted (low) when the VPR-80 is in either shuttle or cue mode. Logic level is high (NORMAL) in all other modes.

The NORMAL/VARIABLE logic level from output data latch 4U38 via 4U50-4 is also not an AST system output. It is derived from the capstan servo. Logic level is high (NORMAL) in all modes except slow motion and faster-than-normal playback. VARIABLE is asserted (low) along with either FORWARD 1 or BACK 1 (see below).

When VARIABLE is asserted, it signifies to the TBC that video is not being sent at a regular rate and that track jumps are required.

The ZERO OFFSET signal from output data latch 4U38 via 4U50-2 shifts output vertical timing of the TBC in H/2 (half-line) increments. Total delay time (offset) is determined by setting sections 1–5 of the SCANNER PHASE switch (5S1) on the Servo PWA. (Refer to Table 3-6 in Section 3, Part I.) The setting of switch 5S1 depends upon the type or model of TBC used with the VPR-80. When the TBC-80 is used, switch 5S1 is set to produce an offset delay of 6.5 to 8 lines.

FORWARD 1 and BACK 1 outputs to the TBC are derived from the A3 and A5 outputs of data latch 4U37. (Refer to paragraph 5-70.) Either FORWARD 1 or BACK 1 is asserted (low) when in slow motion or faster then normal playback mode. The VARIABLE signal is asserted at the same time (see above).

FORWARD 1 is asserted (low) at gate 4U53-3 when playback speed is faster than normal. It moves the write pointer in the TBC memory control forward to keep TBC memory read and write clocks in a synchronous state.

BACK 1 is asserted (low) at gate 4U53-6 when in slow-motion playback. It moves the write pointer in the TBC memory control backward to keep TBC memory read and write clocks in a synchronous state.

FORWARD 2 and BACK 2 logic level outputs are not used in the VPR-80. These outputs are held high.

TBC logic assumes normal playback speed unless notified otherwise by the VARIABLE output of the VPR-80. The VARIABLE signal tells the TBC that playback video is not being sent at a regular rate. At the same time, assertion of either FORWARD or BACK 1 indicates whether tape is moving faster or slower than normal play speed. NORMAL is asserted at normal play speed wherein data is clocked into the TBC memory, and then 6.5 to 8 lines later it is clocked out with synchronous operation. If synchronism between write-in and read-out clocks is lost, FORWARD 1 or BACK 1 causes the appropriate adjustment to be made in the write clock.

For example, if 260 lines are written in the same time that 262 lines are read out (slow motion), FORWARD advances the write clock to match the read clock and keep in sync with reference. Similarly, if tape is moving at faster than normal play speed, lines will have to be skipped to keep in sync because H-rate pulses are coming into the TBC faster than reference. Since data tends to be written into the TBC memory faster than it is being read out, BACK 1 causes the write clock to skip lines.

5-95 Edit Optimization

Edit optimization is necessary to cancel mechanical hysteresis in the AST deflector element. It is required when making interchange edits (on a tape recorded by a different VTR).

Edit optimization is initiated both automatically and manually. Edit optimization is initiated automatically by the servo system CPU if the VPR-80 is in normal playback mode when AST operation is turned off manually with switch 4S3. If the editor is on, AST operation is turned off and edit optimization is initiated automatically at the start of edit play mode.

When system code **10** (edit phase range exceeded) is indicated, the VTR operator should press the EDIT OPTIMIZE switch to initiate the automatic edit optimization sequence. Manual initiation is enabled only in edit play mode.

The edit optimization procedure recenters the AST head on the helical video track and then rephases the scanner tach to the control track on tape, thus peaking the playback rf.

The recentering process laterally displaces the head from the track to the maximum excursion of the deflector element. Displacement is made first to one side of the track and then to the other. This is repeated several times and each succeeding displacement decreases in amplitude until the head is recentered on the track as indicated by maximum rf. This ringing of the AST head deflector element is accomplished in approximately 60 ms.

Scanner tach is then rephased to timing of the video on tape. (Control track is also rephased.) If the edit phase on tape is outside tolerance range for rephasing scanner tach, the SYSTEM indicator is lighted. The **unable to edit optimize** indication (system code **15**) is brought up for display.

If the AST head has been recentered on an incorrect track (field), and there is no color framing, the SYSTEM indicator will light. System code **08 (not field matched)** will be brought up for display.

5-96 Reel Servo

Takeup and supply reel servos maintain proper tape tensions applicable to the commanded mode of operation and tape speed. Digitized tension arm position voltage, summed with applicable reference voltage, is continuously made available to the servo system CPU. The CPU generates error correction words which are converted to analog form and supplied to reel MDAs as error voltages. Takeup and supply reel servos also continuously supply the CPU with reel speeds and calculated tape pack diameters. In addition, tape speed information is furnished to the AST servo. Tape speed is calculated from information supplied by the tape timer tach processor.

Figure 5-27 shows reel servo components on the Servo PWA. Figure 5-27 also shows reel MDAs and Reel Tach PWAs. LED and Photo Potentiometer PWAs, which are part of the tension arm assembly, are also shown.

The following mnemonics (which have not been previously identified in connection with another servo) are used on Figure 5-27:

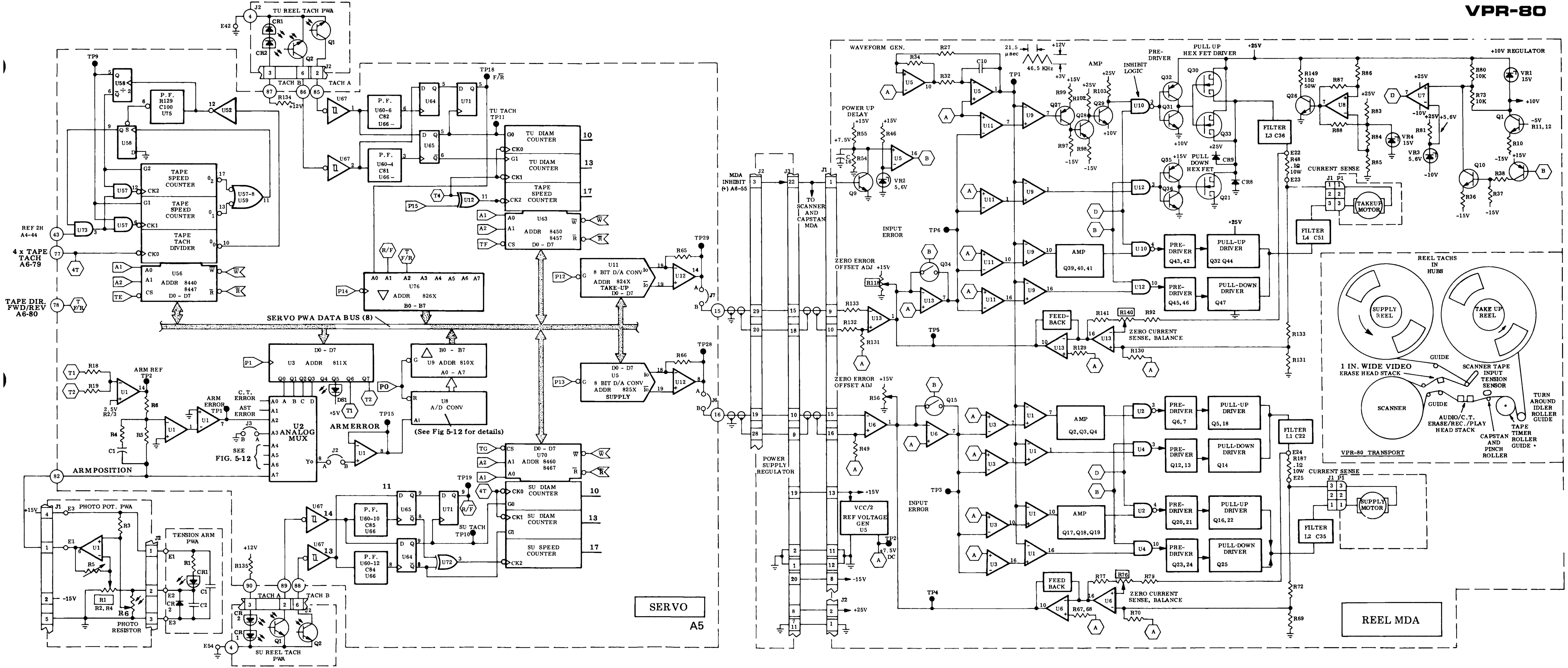


Figure 5-27.
Reel Servo and MDA—PWA5

F/R	Tape direction (high = forward, low = reverse) from takeup reel servo
R/F	Tape direction (high = reverse, low = forward) from supply reel servo
SU	Supply
TU	Takeup
T F/R	Tape direction (high = forward, low = reverse) from Control PWA
T1, T2	Bits of reference tape tension word
4T	Four times tape timer tach frequency

5-97 Reel Tachometers

Supply and takeup reel tachs are identical. They are located behind reel hubs within the reel motor assemblies.

Each tach is two-phase, and is composed of a 16-tooth tach ring and a Reel Tach PWA. The tach ring is part of the turntable assembly. As the turntable revolves, the tach ring teeth pass through two LED/phototransistor calipers on the Reel Tach PWA. Calipers are spaced 60° apart. Resulting light interruptions turn off phototransistors Q1 and Q2 and produce reel tach A and B pulses.

Supply reel A tach and B pulses are routed to Schmitt-trigger buffers 5U67-13/-14. Shaped tach pulses are then applied to the supply reel tach processor composed of 5U60, 5U64, 5U65, 5U71, and 5U72. The tach processor furnishes the supply reel direction signal. This is R/F at 5TP19, where R = reverse, or clockwise rotation, and F = forward, or counterclockwise rotation. This logic level (R = high, F = low) is made available to the servo system CPU at input data buffer 5U76.

The tape direction signal (T F/R) from the control system is also made available to the CPU at input data buffer 5U76. Thus, the CPU can sample control system tape direction and reel direction signals at one time with one decoded address. This is necessary to implement mode change commands which involve a change in tape direction. See paragraph 6-7 on mode control qualification.

Takeup reel tach and tach processor theory is identical with one exception. Reel direction signal logic levels are the opposite. This is F/R at 5TP18, where (F = high and R = low).

The supply reel tach processor also drives supply reel diameter counters and the reel speed counter.

5-98 Tape Pack Diameters

Diameter of the tape pack on each reel is continually calculated and made available to the servo system CPU. The CPU uses tape pack diameter and reel speed information to implement end-of-tape (EOT) logic. The EOT point at each end of the tape prevents the tape from running completely off the reel. The takeup reel EOT point is used to implement unthread mode.

Supply reel tach processor outputs at 5U64-8/-9 enable supply reel diameter counters 5U70-10/-13. The counters are clocked by 4T pulses from the tape timer tach processor (Figure 6-7). The frequency of 4T pulses is 600 Hz at normal play speed.

Counter contents are sampled by the CPU via the Servo PWA data bus. Tape pack diameter is calculated from the number of 4T pulses accumulated in a single revolution of the reel. The calculation is based upon standard NAB* reel hub diameter (4.5 in., or 82.5 mm).

The two diameter counters are alternately clocked. Counter 5U70-10 is clocked on one complete revolution of the supply reel, while the contents of counter 5U70-13 are static. On the next complete revolution of the supply reel counter, 5U70-13 is clocked, and the contents of counter 5U70-10 are static.

Takeup reel tape pack diameter counters, 5U63-10/-13, operate in identical fashion.

5-99 Reel Speed Counter

The supply reel speed counter 5U70-17 is permanently enabled and is clocked by the exclusively OR-gated outputs of 5U64-8 and 5U65-8 in the supply reel tach processor. The CPU continually samples the count contents of 5U70-17 via the data bus. The CPU calculates reel speed on the number of accumulated counts in 5U70-17 per sampling interval. This information is used in implementation of mode change commands from the control system. See paragraph 6-7 on mode control qualification.

5-100 Tape Speed Counter

The tape speed counter logic is composed of 5U56-10/-13/-17 and the associated gating and switching network. Reference 2H pulses from the reference pulse generator (Figure 5-9) are the basic clock input to tape speed counters 5U56-13 and 5U56-17. The 4X tape tach output of the tape timer tach processor (Figure 6-7) clocks tape tach divider 5U56-10. This is a divide-by-5 circuit at normal play speed. The inverted tape tach divider output clocks divider 5U58-5/-6. Output of this divide-by-2 circuit alternately gates reference 2H clock pulses to tape speed counters 5U56-13/-17. Thus, the two tape speed counters are alternately clocked and sampled by the CPU via the data bus.

The CPU generates the AST ramp based on tape speed information from these counters. Refer to paragraph 5-85 and Figure 5-22. This tape speed information is also backup for control system calculations of tape speed based on the output of tape velocity counter 6U27-13 (see Figure 6-7).

5-101 Tension Arm Assembly

The tension arm assembly is instrumented with a photopotentiometer/LED position detector which provides the CPU with arm position (and therefore, tape tension) information. The Photopotentiometer and Tension Arm (LED) PWAs, shown in the lower left-hand corner of Figure 5-27, are located within the tension arm assembly. The light from LED CR1 acts as the wiper of photopot R6 as the tension arm moves through its arc of travel. Output of U1-6 on the Photopotentiometer PWA is routed to connector contact 82 on the Servo PWA. This is arm position voltage, and it varies between -6 Vdc at one extreme of tension arm travel and +6 Vdc at the other extreme. It is zero volts when the tension arm is in the center (at rest) position.

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*National Association of Broadcasters

Resistor R5 provides adjustment of arm position voltages at the extremes of travel. Resistor R1 is the adjustment for zero volts at the center position. See paragraph 5-141. These adjustments are interactive, and arm position voltage is measured at contact 82 the Servo PWA.

Tension arm position voltage is applied to one input of multiplexer 5U2 where voltage is sampled. Arm position voltage is digitized by A/D converter 5U8 and made available to the CPU at input data buffer 5U9. Arm position analog voltage is also routed to the inverting input of 5U1-1 where it is summed with tension arm reference voltage.

Tension arm reference voltage is the analog summation of the reference tension word from the CPU. Reference tension is a 2-bit word (T1, T2), and it is based on the commanded mode of operation. Bits T1 and T2 appear at the Q6 and Q7 outputs of output data latch 5U3. They are converted to analog form by 5U1-14. Arm reference voltage (5TP2) is summed with arm position voltage (contact 82) to produce arm error voltage (5TP1). Arm error voltage is also sampled by 5U2, digitized by 5U8, and routed to the CPU via 5U9.

Four reference tension words define four basic tape tension offsets to arm position voltage. Reference tension words are shown in Table 5-3.

Table 5-3. Reference Tension

Reference Tension Word		Definition
T2	T1	
0	0	Low tension (stop mode, ready condition)
0	1	Medium low tension (play, slow-motion, and record modes)
1	0	Medium high tension (fast play mode)
1	1	High tension (shuttle mode)

5-102 Reel MDAs

The servo system CPU maintains proper tape tensions by examining arm position and arm error samples at input data buffer 5U9. The CPU then calculates appropriate supply and takeup reel speed corrections. The CPU places correction words on the data bus and then addresses D/A converters (DACs) 5U5 and 5U11. DAC 5U5 and 5U12-8 produce an analog error correction voltage (5TP28) for the supply reel MDA. DAC 5U11 and 5U12-14 produce an analog error correction voltage (5TP29) for the takeup reel MDA.

Operation of reel MDAs is explained in detail in paragraph 7-6, Part II.

5-103 REMOVAL/INSTALLATION

The following paragraphs give information on removing and reinstalling the AST Driver PWA, and tension arm, scanner, and capstan assemblies.

5-104 AST Driver PWA

The AST Driver PWA, shown in Figure 5-28, is located behind the control panel assembly. Remove it and reinstall it as follows:

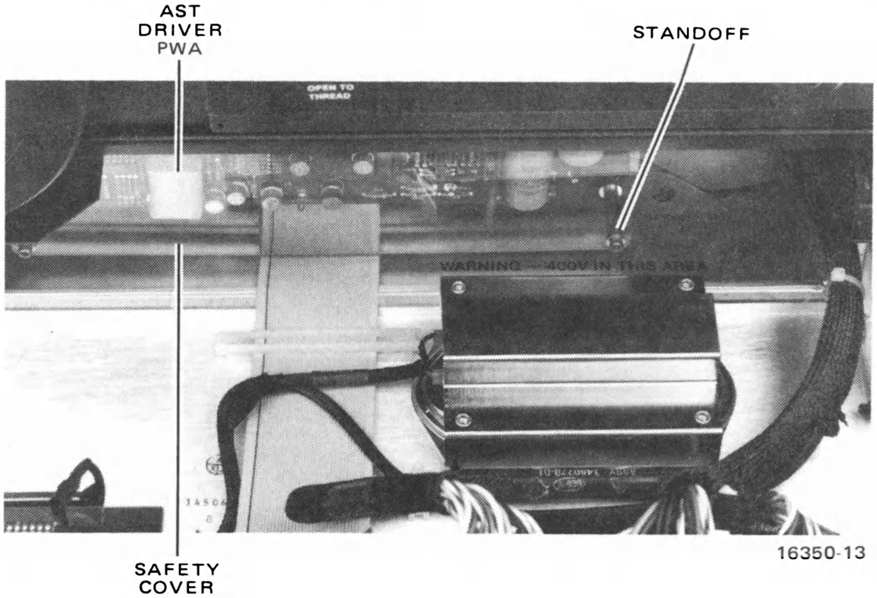


Figure 5-28. Removing AST Driver PWA

WARNING

BE CERTAIN THAT VPR-80 POWER IS OFF BEFORE REMOVING AST DRIVER PWA. THIS PWA USES HIGH VOLTAGE (250 Vdc).

STEP 1 With power off, open hinged transport cover and release catches so cover hangs below control panel.

STEP 2 Remove two screws (one from each side of the control panel) and pivot control panel forward so that AST Driver PWA is accessible.

STEP 3 The plastic safety cover in front of the PWA is mounted on four standoffs. Disengage cover from each of the four standoffs by placing two fingers beneath cover and pressing thumb on standoff.

STEP 4 Disconnect AST connectors P1 and P2 from the PWA.

STEP 5 Using a short cross-recessed screwdriver, remove four crosshead screws that secure PWA to mounting panel and remove PWA.

STEP 6 Reinstall PWA.

5-105 Tension Arm Assembly

If the tension arm assembly needs service, return it to the factory or authorized service center for repair. Remove tension arm assembly from transport (and reinstall it) as follows:

STEP 1 Remove longitudinal head cover and transport trim as outlined in Part I, paragraph 4-12.

STEP 2 With power off, loosen two captive screws at rear of cabinet, and lower rear door assembly as shown in Figure 4-3, Part I.

STEP 3 Disengage four captive screws securing Audio PWA assembly (includes shield).

STEP 4 Detach Audio PWA assembly and lay it back to gain access to rear of tension arm assembly.

STEP 5 Disconnect cable P1 from rear of tension arm assembly.

STEP 6 At the front of the transport, disconnect spring from spring anchor at location shown in Figure 5-29.

STEP 7 Remove three screws that secure tension arm assembly to transport.

STEP 8 Move tension arm to the left so that plastic roller attached to tension arm is in a nonengaged position with respect to slotted plate. See Figure 5-29. Then lift tension arm assembly out from front of transport.

STEP 9 Reinstall tension arm assembly.

5-106 Scanner Assembly

Remove scanner assembly from transport (and reinstall it) as follows:

STEP 1 Remove longitudinal head cover and transport trim as outlined in paragraph 4-12, Part I.

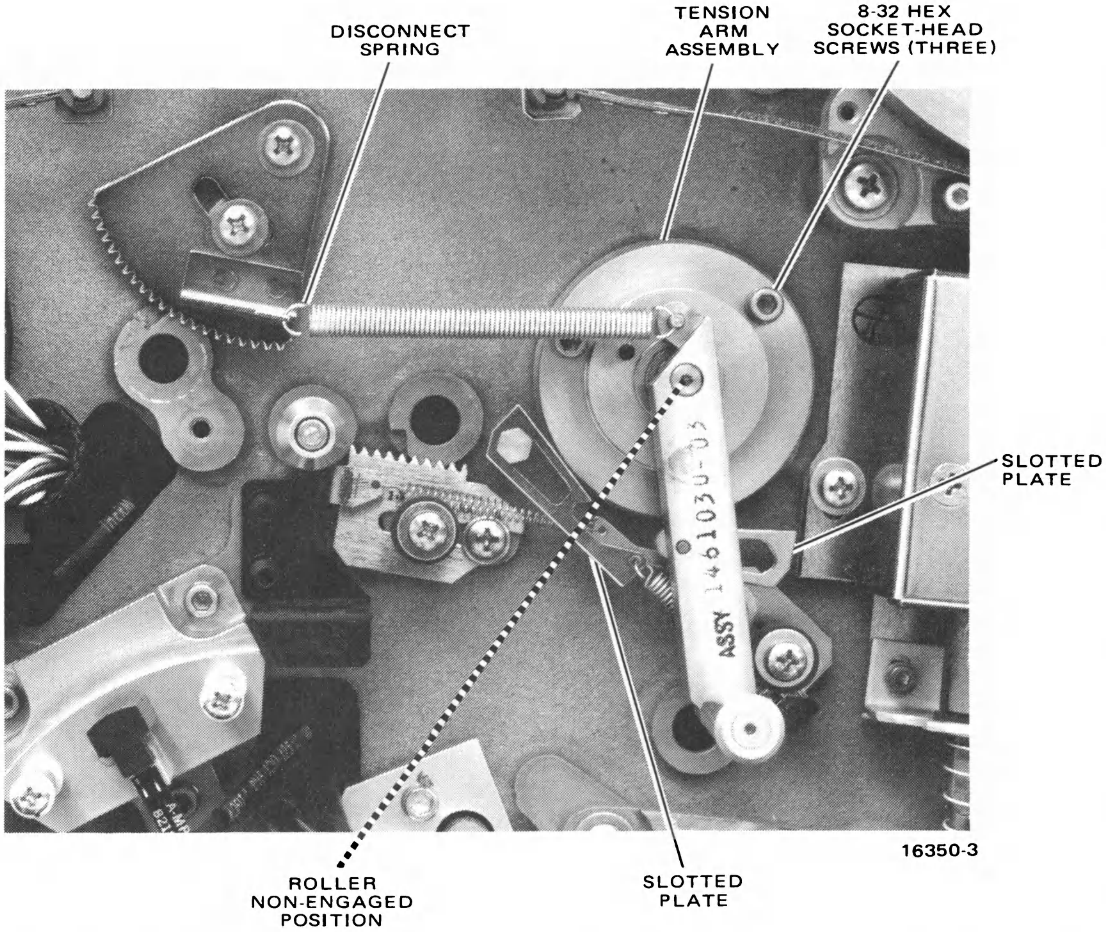


Figure 5-29. Removing Tension Arm Assembly

STEP 2 Remove three screws and washers securing shield over Record Amplifier and Edit Erase PWA, and detach shield. See Figure 5-30.

STEP 3 Disconnect three connectors at Record Amplifier and Edit Erase PWA.

STEP 4 Remove three screws and washers securing scanner base to transport casting.

CAUTION

WHEN HANDLING SCANNER ASSEMBLY, BE CAREFUL NOT TO TOUCH PROTRUDING HEAD TIPS.

STEP 5 Rotate scanner to clear control panel and carefully lift scanner out of well in transport casting just far enough to permit scanner rear connectors to be reached.

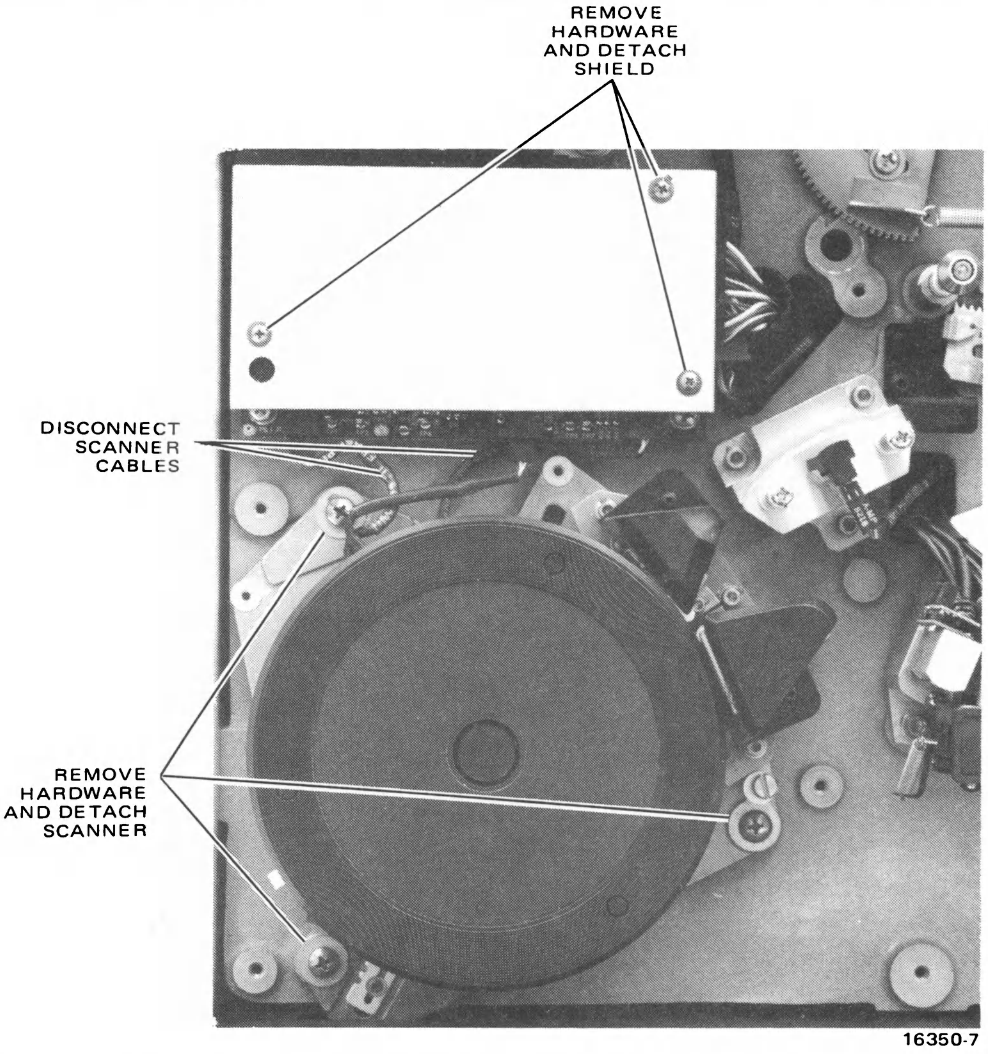

REMOVE HARDWARE AND DETACH SHIELD
DISCONNECT SCANNER CABLES
REMOVE HARDWARE AND DETACH SCANNER
16350-7

Figure 5-30. Removing Scanner Assembly

STEP 6 Disconnect two connectors at rear of scanner to free scanner assembly from transport. When scanner assembly is removed from transport, it can safely rest on motor cover.

STEP 7 Reinstall scanner in reverse order of removal. When installing scanner into transport casting, ensure that scanner mounts flush to casting with no interfering components between mating surfaces.

Note

If scanner assembly is replaced with another scanner assembly, interchangeability must be ensured as outlined in paragraph 4-21, Part I.

5-107 Capstan Assembly

Remove capstan assembly from transport (and reinstall it) as follows:

STEP 1 Remove longitudinal head cover and transport trim as outlined in paragraph 4-12, Part I.

STEP 2 Loosen two captive screws at rear of cabinet, and lower card cage assembly, as shown in Figure 4-3, Part I.

STEP 3 Disengage four captive screws securing Audio PWA assembly (includes shield). See Figure 5-31.

STEP 4 Cut two cable tie wraps on left-hand side of cabinet which secure cables to Audio PWA. See Figure 5-31.

STEP 5 Detach Audio PWA assembly and lay it back to gain access to the rear of the capstan assembly.

STEP 6 Disconnect cable (P1 CAPSTAN) from capstan/scanner MDA. See Figure 5-32.

STEP 7 Detach capstan motor connector (J1) from connector mounting plate.

STEP 8 Disconnect Capstan Tach PWA connector (P2).

CAUTION

BE PARTICULARLY CAREFUL WHEN REMOVING THE CAPSTAN MOTOR. THE URETHANE COATING ON THE CAPSTAN SHAFT MUST NOT BE DAMAGED IN ANY WAY; OTHERWISE, SHAFT MUST BE REPLACED.

STEP 9 To protect capstan shaft, temporarily cover it with a snug piece of tubing. Tubing inside diameter should be 0.375 in. (9.525 mm).

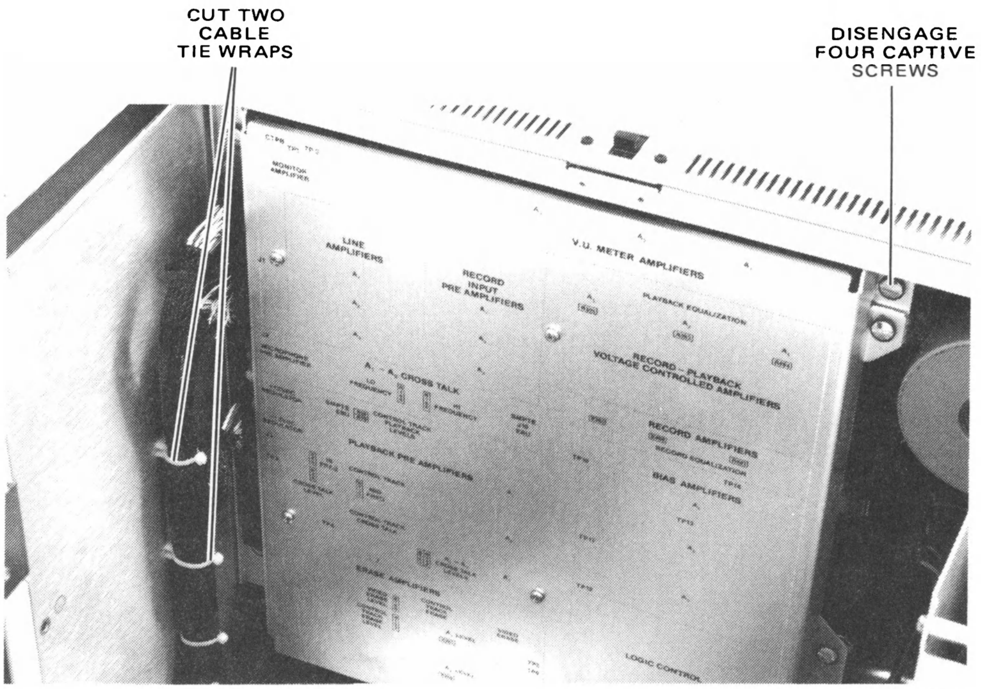
STEP 10 From the front of the transport, remove three socket-head screws securing capstan assembly. See Figure 5-33. Remove capstan assembly at rear of transport.

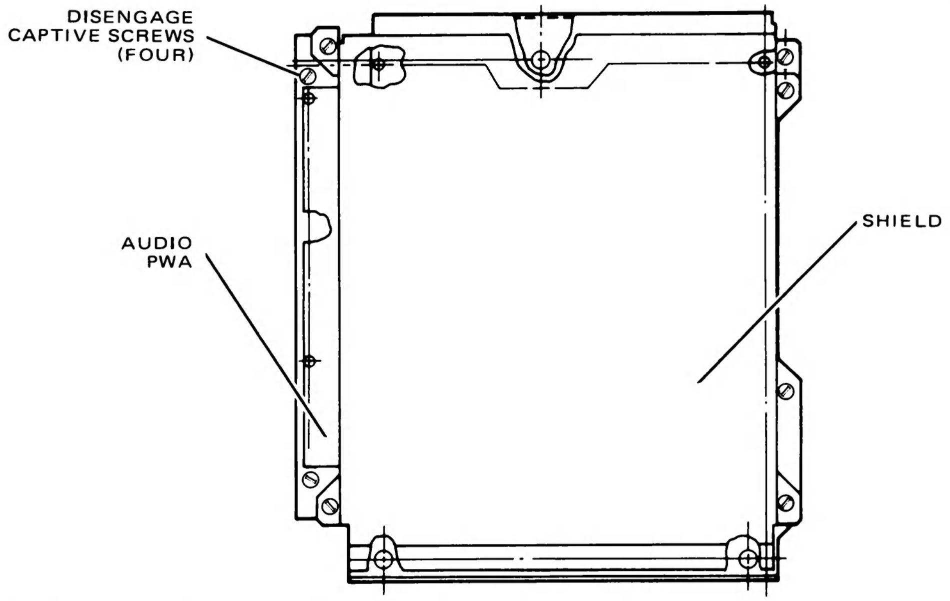
To reinstall capstan assembly, proceed as follows:

STEP 11 Reinstall capstan assembly on transport casting, and secure with the three screws which were removed in step 10.

STEP 12 Reconnect connectors which were detached in steps 6, 7, and 8.

STEP 13 Reinstall Audio PWA assembly which was disengaged in step 3. Secure cables with tie wraps.





REFERENCE DRAWING NO. 1450280-01G

Figure 5-31. Removing Capstan Assembly–Steps 3 and 4

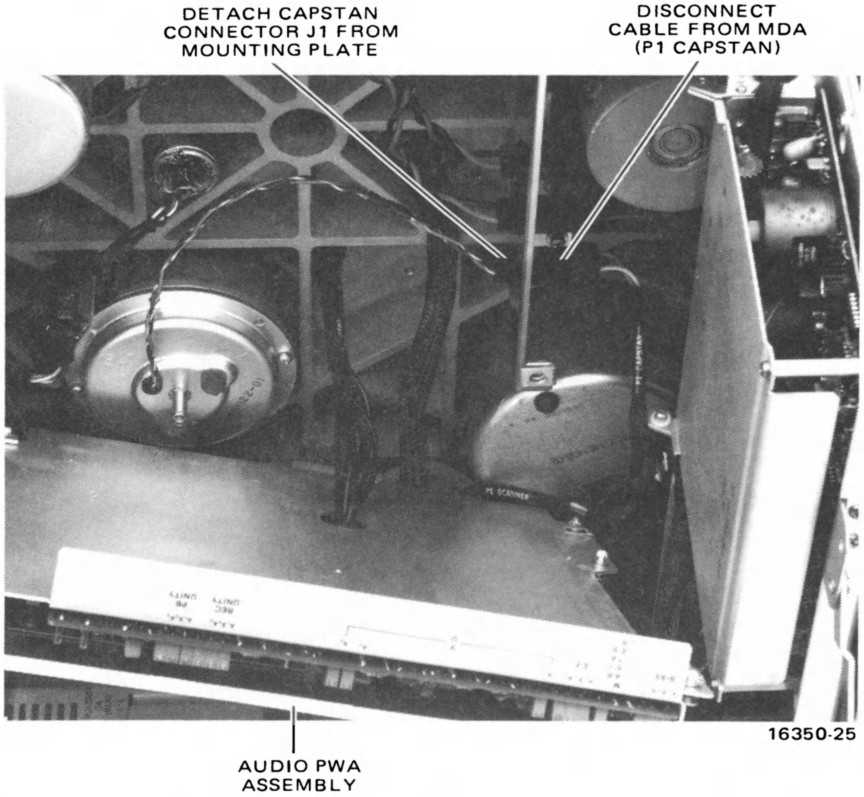

DETACH CAPSTAN CONNECTOR J1 FROM MOUNTING PLATE
DISCONNECT CABLE FROM MDA (P1 CAPSTAN)
16350-25
AUDIO PWA ASSEMBLY

Figure 5-32. Removing Capstan Assembly—Steps 6, 7, and 8

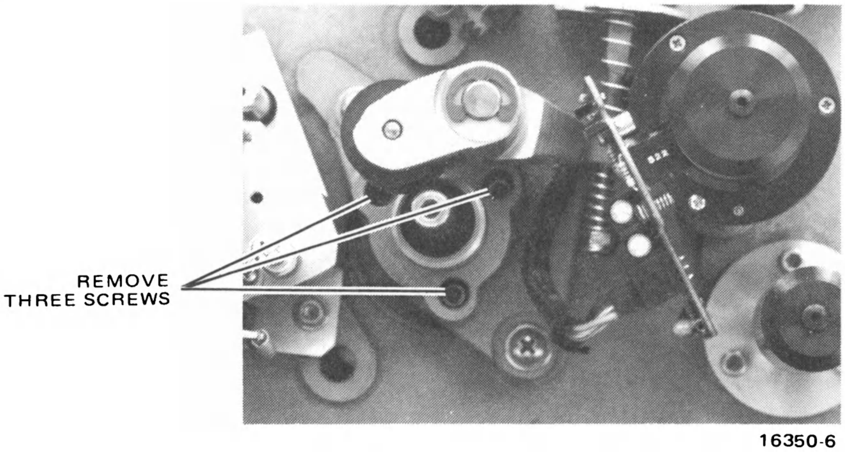


Figure 5-33. Removing Capstan Assembly—Step 10

STEP 14 Raise card cage assembly to its normal operating position, and close rear door assembly.

STEP 15 Reinstall head cover and transport trim.

5-108 PART REPLACEMENT

The following paragraphs provide instructions for replacement of detail parts within scanner and capstan assemblies.

5-109 Scanner Assembly

The following paragraphs cover replacement of parts within the scanner assembly. Instructions for replacement of heads, slip-ring brushes, slip rings, motor brushes, motor rotor, and components on the Preamplifier PWA are given.

5-110 Head Replacement

It is not necessary to remove scanner assembly from the transport to replace scanner heads.

CAUTION

IF THE AST RECORD/PLAY HEAD IS REPLACED, AST ALIGNMENT PROCEDURES MUST BE PERFORMED. SEE PARAGRAPH 5-127.

Table 5-4 lists scanner head part numbers. Figure 5-34 shows location of head assemblies, three head registration lock/release screws, and head securing devices.

Table 5-4. Scanner Head Part Numbers

Head Description	Ampex Part No.
Automatic Scan Track (AST) Head, 60 Hz	1451200
Automatic Scan Track (AST) Head, 50 Hz	1451220
Video Erase Head, 60 Hz	1401160
Video Erase Head, 50 Hz	1401165
Video Dummy Head	1451210
Sync Dummy Head	1401170

The AST record/play head, video erase head, and video dummy head are each secured with a bridge clamp. The three sync dummy heads are held in place using a connector brace secured by a single screw. A lip is provided on each bridge clamp to support the signal connector and counteract centrifugal force resulting from scanner rotation.

To replace a head, proceed as follows:

STEP 1 Remove power from VPR-80.

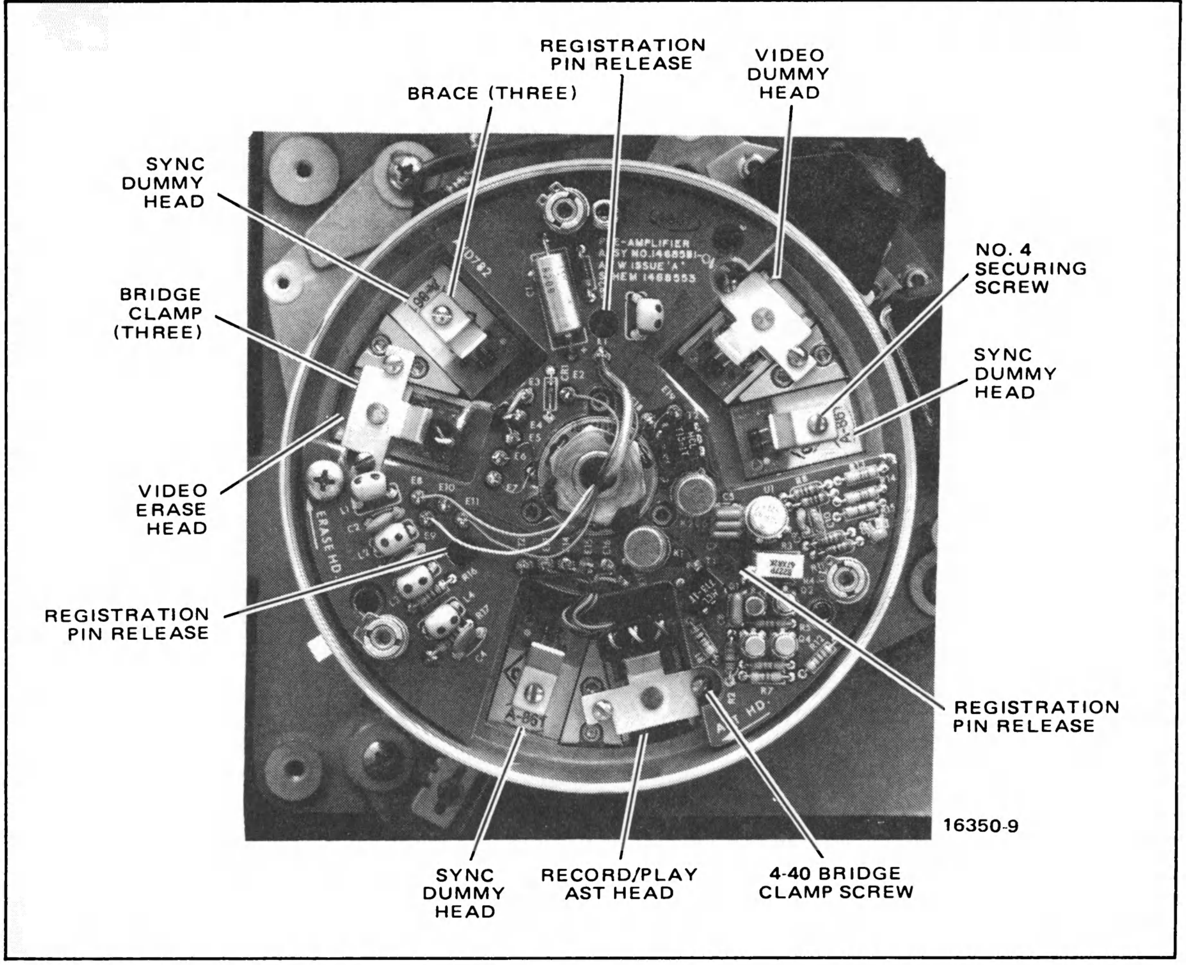


Figure 5-34. Scanner Heads and Head Securing Devices

STEP 2 Remove tape from scanner assembly.

STEP 3 Remove scanner top cover by loosening three crosshead screws.

STEP 4 To preclude the possibility of a tool striking the entrance or exit guide, rotate scanner clockwise so that head to be changed points away from entrance or exit guide.

STEP 5 Being careful not to pull on connector wires, carefully disconnect head connector by pulling connector straight up from scanner.

STEP 6 To change AST record/play head, video erase head, or video dummy head, perform the following steps. (To change a sync dummy head, proceed to step 7.)

a. Turn the two outer no. 4 slot-head screws of bridge clamp two turns counterclockwise so that bridge can be slipped out from under the two securing screws.

b. Access to the registration pin head lock release is through a hole in the Preamplifier PWA that is nearest the head to be changed (Figure 5-34). Turn the head lock screw counterclockwise from center detent until it stops (about 1/4-turn) to retract the registration pin from the head.

c. Carefully slide head back toward center of scanner casting, and raise rear end of head assembly while removing head from scanner.

d. Check that there is no dirt or lint on scanner (use clean compressed air if available). Carefully slide new head in place into scanner while taking care not to hit the head tip. Slide head all the way forward toward outer edge of scanner.

e. Lock head against the registration pin by turning registration pin head lock screw clockwise to center detent.

f. Slide bridge clamp under the two bridge securing screws and then tighten the two screws.

g. Align head connector with head connector pins and gently insert head connector (if applicable).

STEP 7 To change a dummy sync head, perform the following steps.

a. Unscrew the single no. 4 slot-head screw that secures the head and connector brace to scanner casting. Remove brace and screw.

b. Access to registration pin head lock is through a hole in the Preamplifier PWA that is nearest to the head being changed (Figure 5-34). Turn head lock screw clockwise from center detent until it stops (about 1/4-turn) to retract registration pin from the head.

c. Carefully slide head back toward center of casting and raise rear end of head assembly while removing head from scanner.

d. Check that there is no dirt or lint on scanner (use clean compressed air if available). Carefully slide new head in place into scanner while taking care not to hit the tip. Slide head all the way forward toward outer edge of scanner.

e. Lock head against registration pin by turning registration pin head-lock screw counterclockwise to center detent.

f. Reinstall the no. 4 slot-head screw and connector brace removed in step 7a. Tighten screw just enough to hold head in place (do not overtighten screw).

CAUTION

DO NOT APPLY HEAD DATA GUMMED LABEL FROM HEAD BOX TO ROTATING SCANNER AS THIS WILL CAUSE SCANNER TO BE OUT OF BALANCE.

STEP 8 Reinstall scanner top cover removed in step 3 so that identifying engraving on head cover is aligned with the respective head assembly. Do not over-tighten the three screws that secure cover.

5-111 Slip-Ring Brushes

The twelve graphite scanner slip-ring brushes (Ampex Part No. 1461442) have a long life expectancy and should not require frequent replacement. However, if they become broken, damaged, or contaminated, they can be changed as follows:

STEP 1 Remove scanner assembly from transport as described in paragraph 5-106. Install scanner onto service leg set assembly (see Table 4-1, Part I).

STEP 2 With rear of scanner facing upward, remove the two screws securing motor cover to scanner assembly. See Figure 5-35.

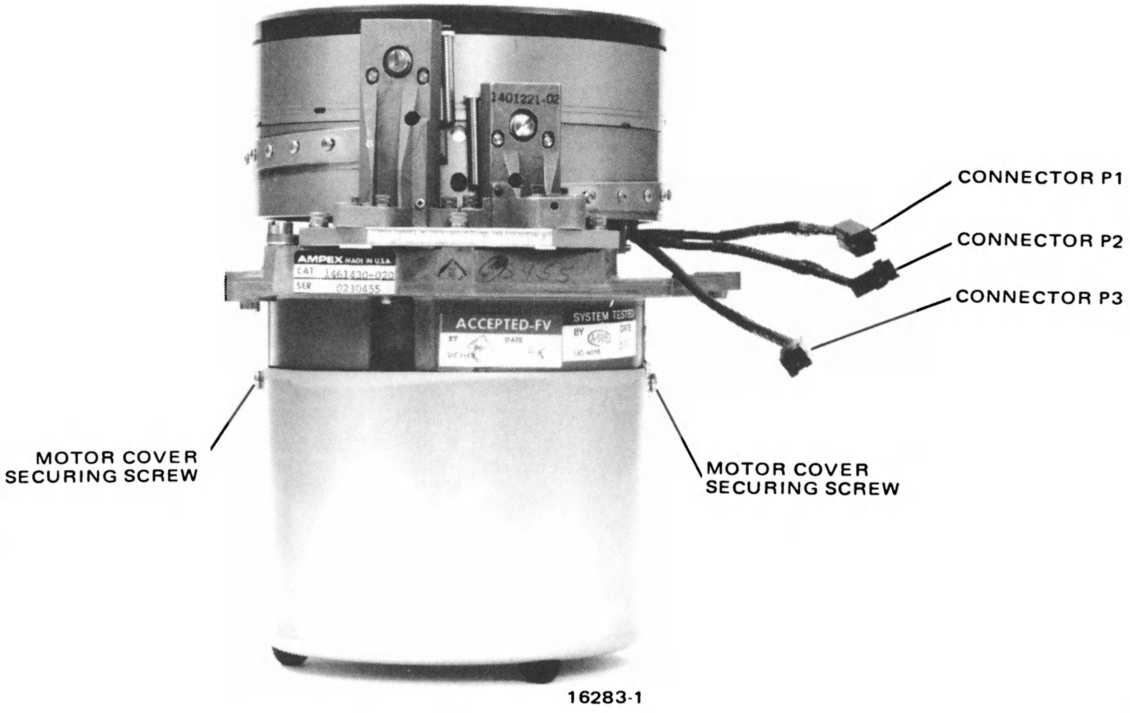


Figure 5-35. Scanner Motor Cover

STEP 3 Remove the three 6-32 screws that secure the brush support bracket to motor spacer. See Figure 5-36.

STEP 4 Slide brush housing in direction shown in Figure 5-36, allowing brushes to snap together so that brush housing can be lifted free of slip-ring assembly.

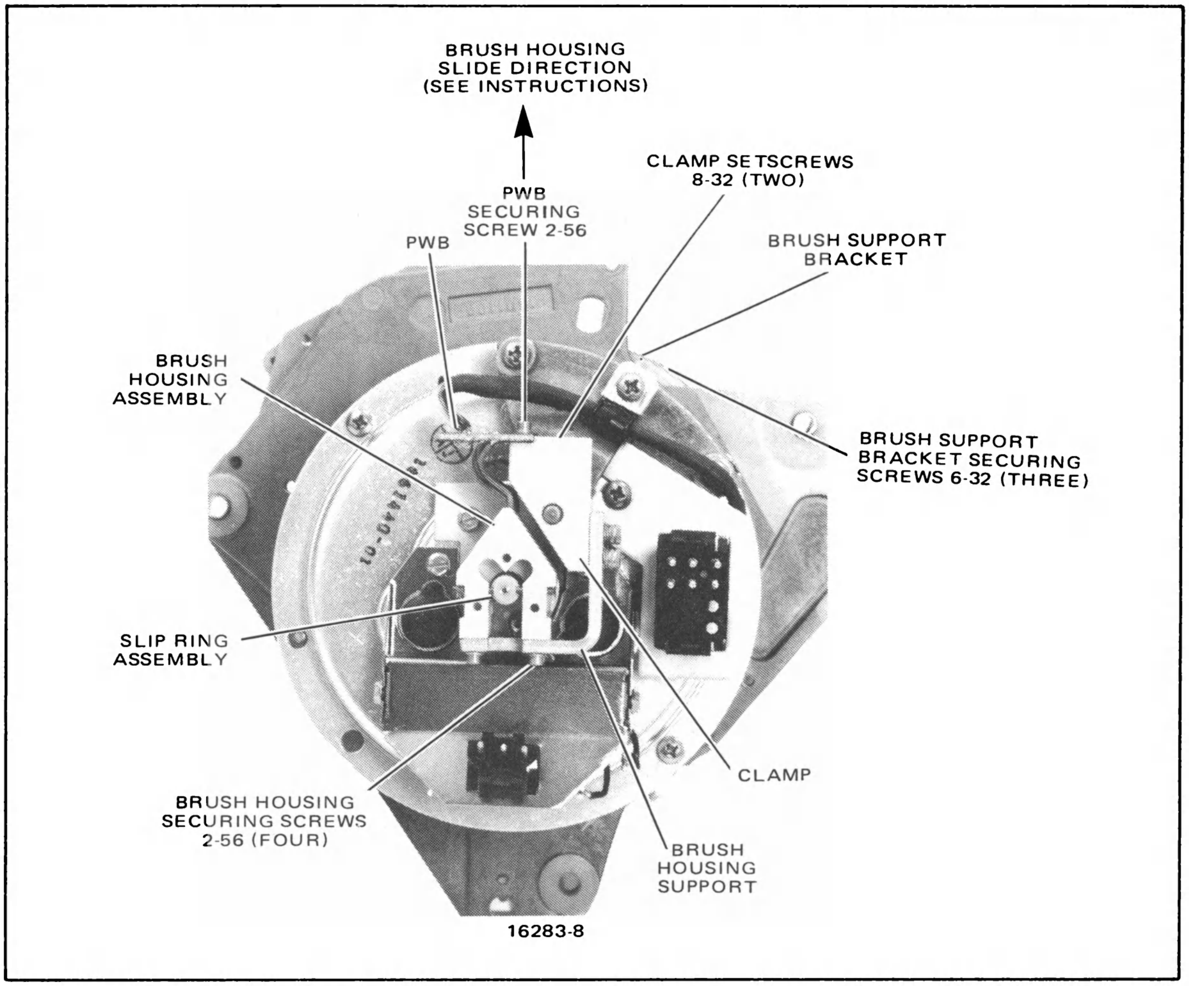

BRUSH HOUSING SLIDE DIRECTION (SEE INSTRUCTIONS)
CLAMP SETSCREWS 8-32 (TWO)
PWB SECURING SCREW 2-56
PWB
BRUSH SUPPORT BRACKET
BRUSH HOUSING ASSEMBLY
BRUSH SUPPORT BRACKET SECURING SCREWS 6-32 (THREE)
SLIP RING ASSEMBLY
CLAMP
BRUSH HOUSING SECURING SCREWS 2-56 (FOUR)
BRUSH HOUSING SUPPORT
16283-8

Figure 5-36. Scanner Slip-Ring Brush Replacement

STEP 5 Move the 12 brush retaining springs aside, one at a time, and withdraw old brushes.

STEP 6 Insert brush installation tool (Ampex Part No. 1463203) into brush housing as shown in Figure 5-37. The tool holds brushes in a spread position until brush housing is mounted in place around the slip-ring assembly.

STEP 7 Install new carbon brushes with V-groove end out. Place brush retaining springs back into place over brush ends, and examine each brush to verify that spring wire is resting in the V-groove in end of brush.

CAUTION

USE EXTREME CARE NOT TO HIT, SCRAPE, OR OTHERWISE DAMAGE PRECISION SURFACE OF THE SILVER SLIP RINGS. EVEN A MINOR NICK CAN CAUSE ARCING WHICH CAN AFFECT PICTURE QUALITY.

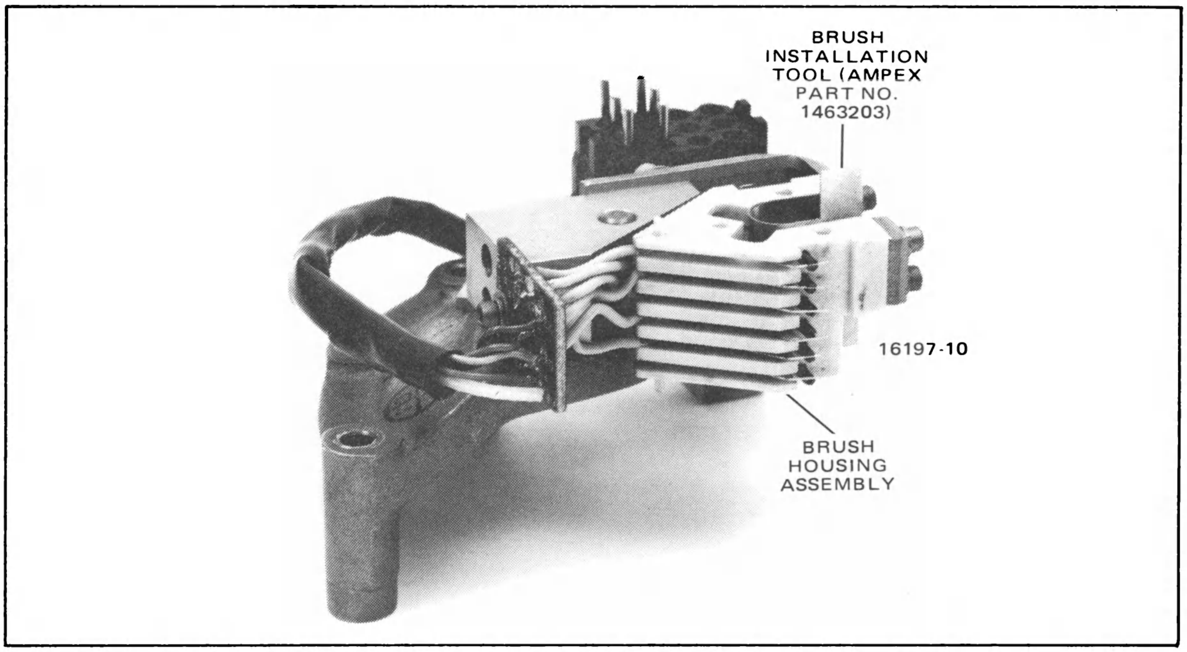


Figure 5-37. Brush Installation Tool Mounted on Brush Housing Assembly

STEP 8 Inspect slip rings closely to ensure there are no scratches, nicks, grooves, or contamination on the rings. The presence of any of these factors can cause arcing and result in picture degradation. If cleaning is needed, clean the slip rings with freon. See paragraph 5-122.

STEP 9 Put brush housing assembly, with brush installation tool still installed, in position around slip-ring assembly. Secure brush support bracket to motor spacer using three 6-32 screws removed in step 3.

STEP 10 Carefully remove brush installation tool allowing brushes to contact slip-ring assembly.

STEP 11 If necessary for brush/slip-ring alignment purposes, loosen two 8-32 clamp setscrews (Figure 5-36) and four brush housing 2-56 securing screws. Orient brush housing to ensure that it is centered over slip-ring assembly and that all brushes contact slip ring at the center of slip-ring area. Tighten screws.

STEP 12 Reinstall scanner motor cover (two screws) and remove scanner service leg assembly.

STEP 13 Reinstall scanner into transport as described in paragraph 5-106.

5-112 Motor Brushes

Scanner motor brushes are located within the scanner brush plate assembly (rear cover of motor). Replace brushes using Brush Replacement Ampex Part No.

1461442-AA (black wire with white tracer) and Brush Replacement Ampex Part No. 1461442-AB (red wire with white tracer). These parts consist of an electrographite brush with attaching wire, and spiked spade. Proceed as follows:

STEP 1 Remove scanner assembly from transport as described in paragraph 5-106 and install scanner on service leg assembly.

STEP 2 With rear of scanner facing upward, remove two 6-32 screws securing motor cover to drum adapter plate and remove cover.

STEP 3 Remove the three 6-32 screws that secure brush support bracket to motor spacer. Refer to Figure 5-36.

STEP 4 Slide brush housing in direction shown in Figure 5-36, allowing brushes to snap together so that brush housing can be lifted free of slip-ring assembly.

STEP 5 Remove two no. 4 screws that secure printed circuit motor plate shield to the brush plate assembly. See Figure 5-38.

STEP 6 Remove two 6-32 screws that mount brush plate assembly to motor spacer (one side) and motor front plate (other side).

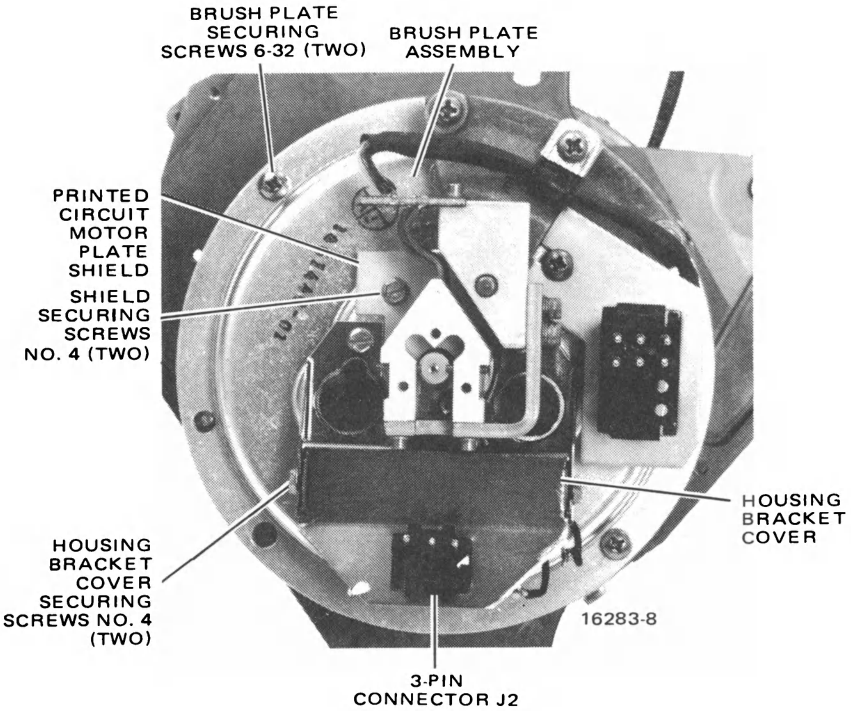

BRUSH PLATE SECURING SCREWS 6-32 (TWO)
BRUSH PLATE ASSEMBLY
PRINTED CIRCUIT MOTOR PLATE SHIELD
SHIELD SECURING SCREWS NO. 4 (TWO)
HOUSING BRACKET COVER
HOUSING BRACKET COVER SECURING SCREWS NO. 4 (TWO)
16283-8
3-PIN CONNECTOR J2

Figure 5-38. Scanner Motor Brush Replacement

CAUTION

DURING NEXT STEP, DO NOT SLIDE SCREWDRIVER IN TOO FAR AS ROTOR DAMAGE CAN OCCUR. PULL MOTOR BRUSH PLATE STRAIGHT UP FROM MOTOR HOUSING. DO NOT SLIDE LATERALLY OR ROTOR DAMAGE CAN OCCUR. DO NOT SCRATCH OR TOUCH PRINTED MOTOR ROTOR SURFACE, ESPECIALLY IN COMMUTATOR AREA.

STEP 7 The permanent magnet within the brush plate assembly tends to hold the plate to the motor front plate. Use a flat-bladed screwdriver placed in slot provided in the front plate to carefully pry plate up from motor front plate. Then remove brush plate assembly.

CAUTION

DO NOT ALLOW METALLIC PARTICLES TO GATHER ON PERMANENT MAGNET.

STEP 8 Remove two no. 4 screws that secure housing bracket cover to housing bracket and remove cover.

STEP 9 Unsolder the two brush connector wires connected to feed-through capacitors. See Figure 5-39.

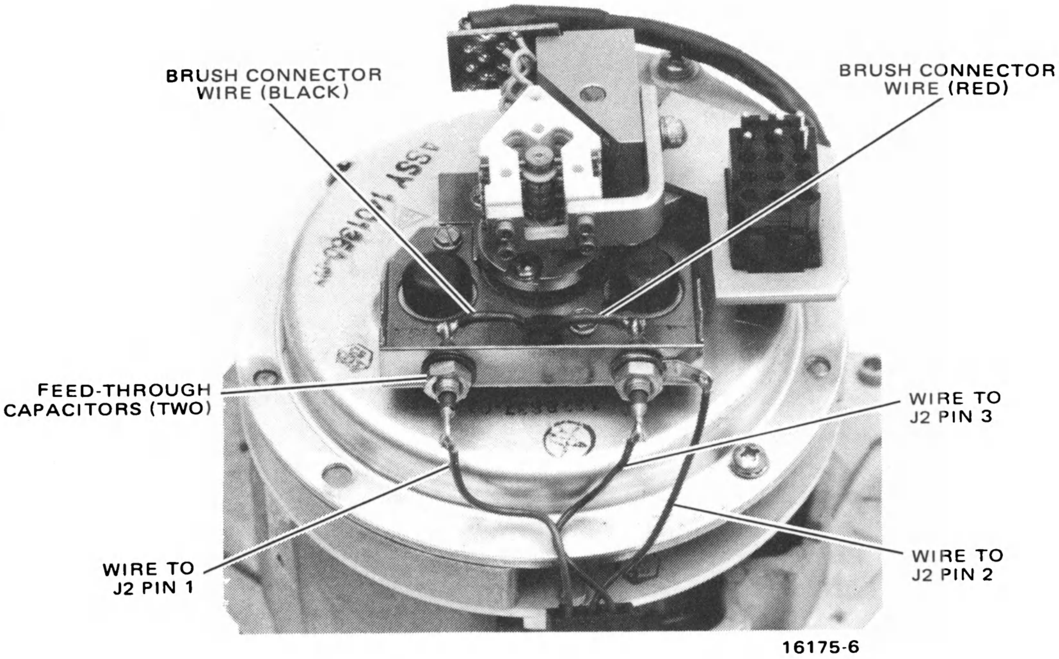

BRUSH CONNECTOR WIRE (BLACK)
BRUSH CONNECTOR WIRE (RED)
FEED-THROUGH CAPACITORS (TWO)
WIRE TO J2 PIN 3
WIRE TO J2 PIN 1
WIRE TO J2 PIN 2
16175-6

Figure 5-39. Scanner Motor Brush Wiring

STEP 10 Use needle-nose pliers to pull crimp straight up to remove each spiked spade and brush from the two rubber grommet/brush holders. See Figure 5-40. Pull out connecting wires that were unsoldered in step 9. Save the two springs.

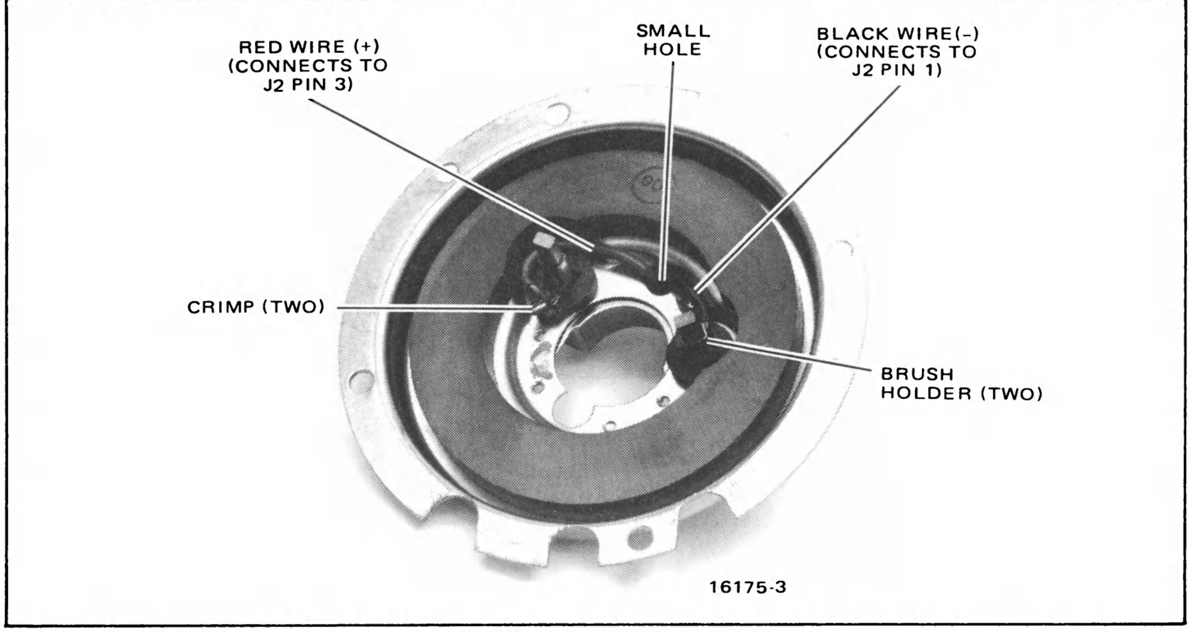


Figure 5-40. Scanner Brush Plate Assembly Rear View

STEP 11 Note that outside of brush plate assembly is identified (+) and (–). Insert springs saved in step 10 into brush holders and install black/white wire replacement brush into the (-) terminal. Install red/white wire replacement brush into the (+) terminal. Feed wires through small hole. Insert brush into holder and insert spiked spade into rubber grommet to secure. Brush should move freely in and out under spring pressure.

STEP 12 Cut brush red/white and black/white wires to appropriate length allowing for stripping of insulation from end. Solder positive (+) red brush lead to feed-through capacitor that is wired to connector J2 pin 3. Solder negative (-) black brush lead to feed-through capacitor that is wired to connector J2 pin 1.

STEP 13 Reinstall cover removed in step 8.

STEP 14 Clean all contamination from magnet and brushes with isopropyl alcohol. Remove all residue and allow brushes to dry.

STEP 15 Clean rotor surface with isopropyl alcohol. Remove all residue.

STEP 16 Carefully reinstall brush plate assembly onto front plate and position over the front plate centering indentations. Secure with screws removed in step 6.

STEP 17 Reinstall printed motor plate shield onto brush plate assembly and secure with screws removed in step 5.

STEP 18 Reinstall (and adjust as necessary) brush housing assembly by following instructions given in paragraph 5-111, steps 5 through 12.

STEP 19 Reinstall scanner into transport as described in paragraph 5-106.

Note

It may require approximately 30 hours of running time before brushes are properly contoured to the rotor surface.

5-113 Slip-Ring Assembly

The slip-ring assembly has a long life expectancy and should normally not require replacement. However, minor nicks, grooves, or other damage to the silver rings can cause arcing which can affect picture quality. In such cases, the slip-ring assembly should be replaced.

The slip-ring assembly is mounted on top of the collar adapter as shown in Figure 5-41. Three sets of shielded connecting wires feed from it through the center of the scanner assembly and connect to terminals on the Preamplifier PWA. This PWA is located on the upper (rotating) drum of the scanner assembly.

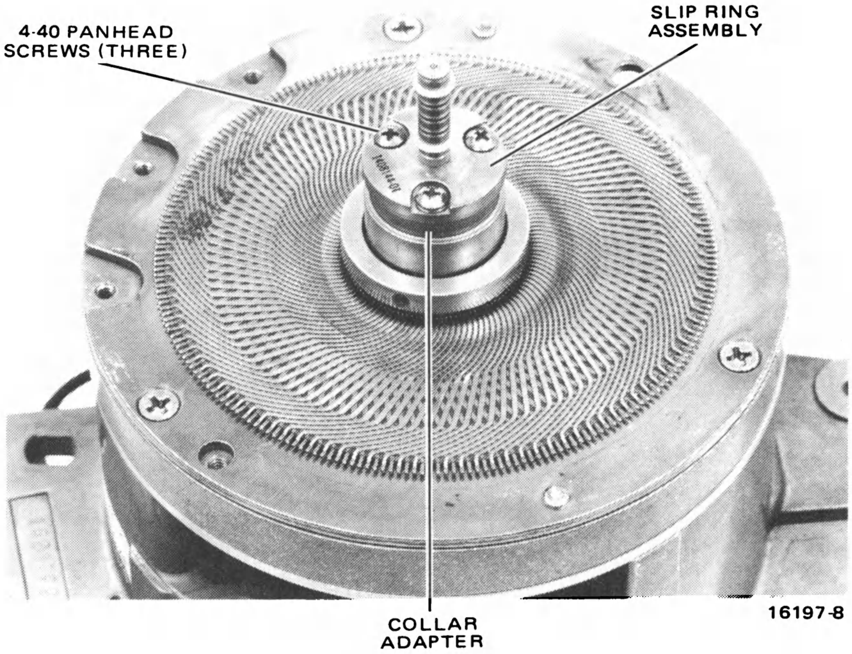


Figure 5-41. Scanner Slip-Ring Assembly

Replace the slip-ring assembly using the procedure below. Note that a dial indicator tool is required for setting runout.

STEP 1 Remove scanner assembly from transport as described in paragraph 5-106. Install scanner on service leg assembly.

STEP 2 Remove brush housing assembly as described in paragraph 5-111, steps 2 through 4.

STEP 3 Remove the three 4-40 panhead screws (Figure 5-41) securing slip-ring assembly to collar adapter. Temporarily put motor cover back on scanner.

STEP 4 Invert scanner so that rotating drum is facing upward and remove drum cover (three screws).

STEP 5 Unsolder six slip-ring wires from Preamplifier PWA terminals E1, E2, and E8-E11. See Figure 5-42.

STEP 6 Tilt scanner sideways and remove motor cover. Carefully remove slip-ring assembly with connecting wires from scanner.

STEP 7 Compare wire length between new slip-ring assembly and the old. If necessary, trim leads of new assembly to match those of old (lead length must be duplicated to ensure critical scanner balance is retained).

STEP 8 Thread six wires of new slip-ring assembly through scanner core to Preamplifier PWA. Continue threading until slip-ring assembly base mates with its mounting surface on scanner. (It may be helpful to temporarily place wires inside a piece of tubing to facilitate threading them through the scanner. Remove tubing before soldering leads in place.)

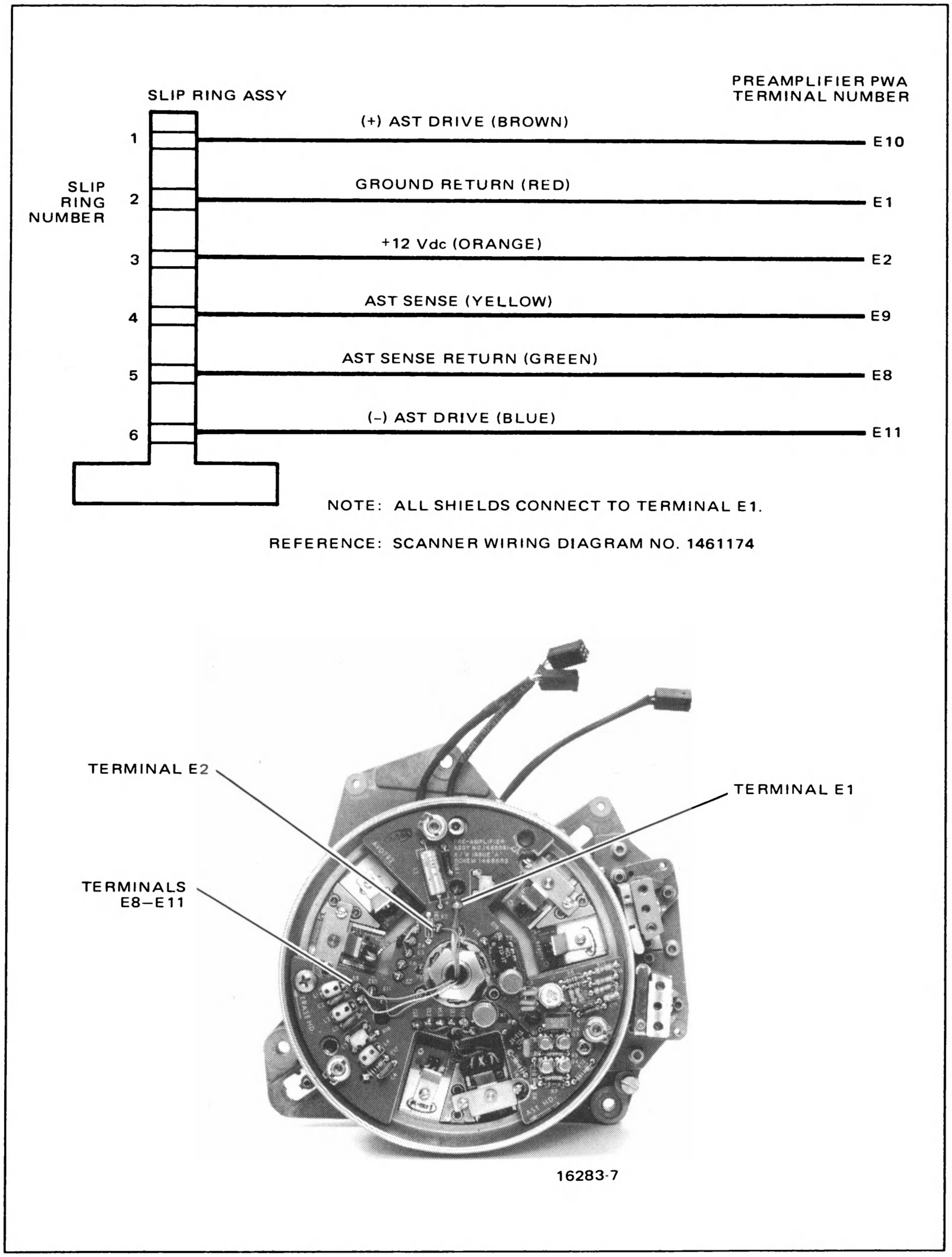
STEP 9 Solder slip-ring assembly leads to Preamplifier PWA terminals using a minimum of solder. Refer to Figure 5-42 for lead color/terminal assignment.

STEP 10 Reinstall scanner top cover in its proper orientation.

STEP 11 Invert scanner and insert three 4-40 screws that secure slip-ring assembly. Thread screws loosely.

STEP 12 Loosen the two 8-32 clamp setscrews (Figure 5-36) and remove clamp from brush support bracket stub.

STEP 13 Install brush support bracket on motor spacer using three 6-32 screws and then mount Starrett 711-HS dial indicator and indicator support on brush support bracket stub as shown in Figure 5-43.



NOTE: ALL SHIELDS CONNECT TO TERMINAL E1.

REFERENCE: SCANNER WIRING DIAGRAM NO. 1461174

Figure 5-42. Slip-Ring Wire Connections to Preamplifier PWA

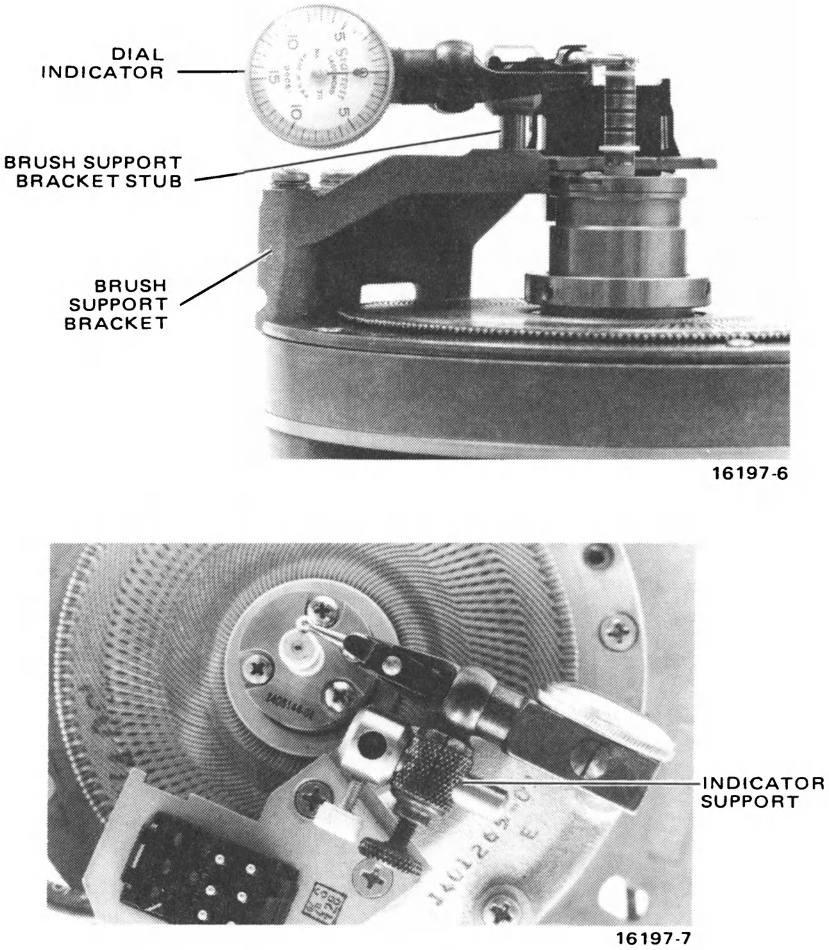


Figure 5-43. Measuring Slip-Ring Runout

STEP 14 Locate indicator tip at center of the number 1 ring (top ring) and adjust indicator for half-scale reading.

STEP 16 Tighten three slip-ring mounting screws and recheck for concentricity. If it is more than 0.001 in. (0.0254 mm) runout, loosen mounting screws and repeat steps 14 and 15.

STEP 17 Remove dial indicator and support from brush support bracket stub. Clean slip ring with freon before proceeding.

STEP 18 Install new brushes and reinstall and adjust brush housing assembly by following instructions given in paragraph 5-111, steps 5 through 12.

STEP 19 Reinstall scanner assembly into transport as described in paragraph 5-106.

5-114 Motor Rotor

CAUTION

DYNAMIC SCANNER BALANCE, AS ACHIEVED AT THE FACTORY, IS CRITICAL. REMOVING AND REPLACING THE MOTOR ROTOR DEGRADES THIS BALANCE. SCANNER IMBALANCE CAN CAUSE VIDEO DETERIORATION OR POSSIBLY DAMAGE TO THE SCANNER. THE FOLLOWING INSTRUCTIONS FOR ROTOR REPLACEMENT SHOULD BE FOLLOWED ONLY IN AN EMERGENCY, AND ONLY WHEN AMPEX SERVICE IS NOT AVAILABLE.

Replace scanner motor rotor as follows:

STEP 1 Remove scanner assembly from transport as outlined in paragraph 5-106, steps 1 through 6. Install scanner on service leg assembly.

STEP 2 With rear of scanner facing upward, remove two 6-32 screws securing motor cover to drum adapter plate and remove cover.

STEP 3 Remove the three 6-32 screws that secure brush support bracket to motor spacer. Refer to Figure 5-36.

STEP 4 Slide brush housing in direction shown in Figure 5-36, allowing brushes to snap together so that brush housing can be lifted free of slip-ring assembly.

STEP 5 Remove two no. 4 screws that secure printed circuit motor plate shield to brush plate assembly. See Figure 5-38.

STEP 6 Remove two 6-32 screws that mount brush plate assembly to motor spacer (one side) and motor front plate (other side).

CAUTION

DURING NEXT STEP, DO NOT SLIDE SCREWDRIVER IN TOO FAR AS ROTOR DAMAGE CAN OCCUR. PULL MOTOR BRUSH PLATE STRAIGHT UP FROM MOTOR HOUSING. DO NOT SLIDE LATERALLY OR ROTOR DAMAGE CAN OCCUR. DO NOT SCRATCH OR TOUCH PRINTED MOTOR ROTOR SURFACE, ESPECIALLY IN COMMUTATOR AREA.

STEP 7 The permanent magnet within brush plate assembly tends to hold plate to motor front plate. Use a flat-bladed screwdriver placed in the slot provided in the front plate to carefully pry plate up from motor front plate. Then remove brush plate assembly.

CAUTION

DO NOT ALLOW METALLIC PARTICLES TO GATHER ON PERMANENT MAGNET.

STEP 8 Loosen three no. 4 hex recessed setscrews (Figure 5-44) and remove motor clamp.

STEP 9 Remove old rotor and install new rotor.

STEP 10 Reinstall rotor motor clamp against rotor. Observe clearance between circumference of motor shaft and rotor motor clamp. Tighten three no. 4 setscrews alternately so that when screws are equally tight there is equal clearance all around shaft and clamp.

STEP 11 Clean new rotor assembly with isopropyl alcohol used sparingly. Remove all residue.

STEP 12 Clean brushes and interior of brush plate assembly with isopropyl alcohol or compressed air. Remove all residue and dry with compressed air.

STEP 13 Carefully reinstall brush plate assembly onto front plate in position over front plate centering indentations. Secure with two 6-32 screws.

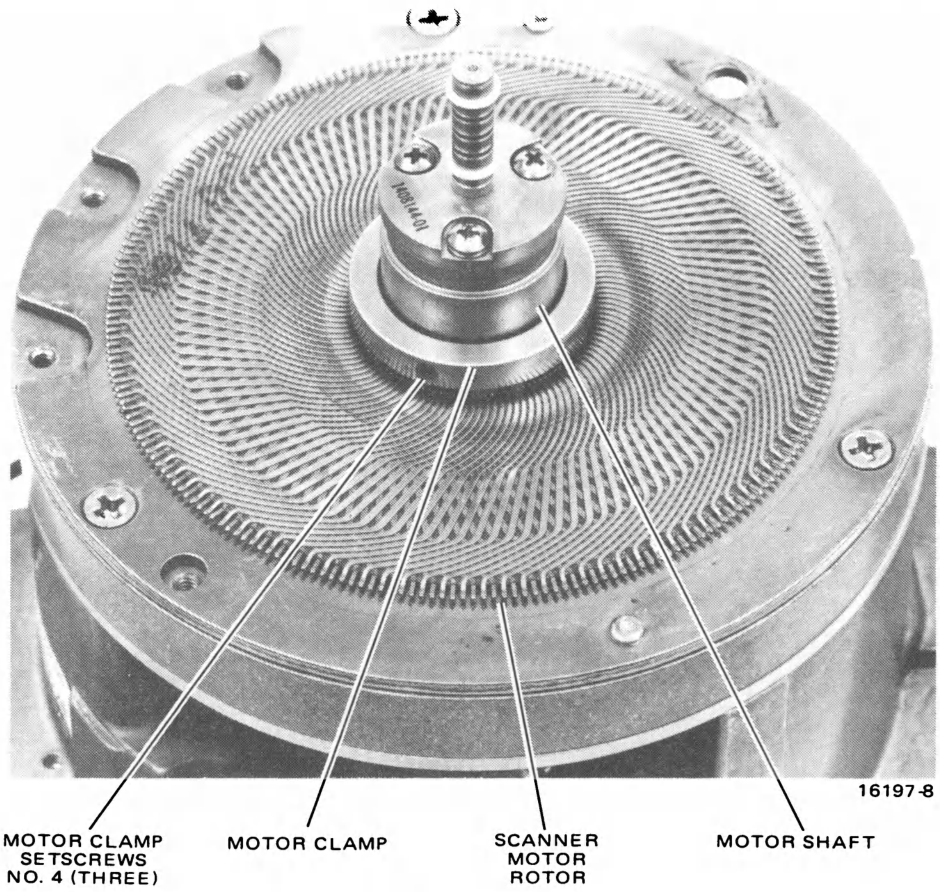


Figure 5-44. Replacing Scanner Motor Rotor

STEP 14 Reinstall printed motor plate shield onto brush plate assembly and secure with two no. 4 screws.

STEP 15 Insert brush installation tool (Ampex Part No. 1463203) into brush housing as shown in Figure 5-37. Tool holds brushes in a spread position until brush housing is mounted in place around slip-ring assembly.

STEP 16 Examine each brush to verify that spring wire is resting in the V-groove in end of brush.

CAUTION

USE EXTREME CARE NOT TO HIT, SCRAPE, OR OTHERWISE DAMAGE PRECISION SURFACE OF THE SILVER SLIP RINGS. EVEN A MINOR NICK CAN CAUSE ARCING WHICH CAN AFFECT PICTURE QUALITY.

STEP 17 Inspect slip rings closely to ensure there are no scratches, nicks, grooves, or contamination on the rings. The presence of any of these factors can cause arcing and result in picture degradation. If cleaning is needed, clean slip rings with freon. See paragraph 5-122.

STEP 18 Put brush housing assembly, with brush installation tool still installed, in position around slip-ring assembly. Secure brush support bracket to motor spacer using three 6-32 screws removed in step 3.

STEP 19 Carefully remove brush installation tool allowing brushes to contact slip-ring assembly.

STEP 20 If necessary for brush/slip-ring alignment purposes, loosen two 8-32 clamp setscrews (Figure 5-36) and four brush housing 2-56 securing screws. Orient brush housing to ensure it is centered over slip-ring assembly and that all brushes contact slip ring at the center of slip-ring area. Tighten screws.

STEP 21 Reinstall scanner motor cover (two screws) and remove scanner service leg assembly.

STEP 22 Reinstall scanner assembly into transport as described in paragraph 5-106.

5-115 Preamplifier PWA Parts

In an emergency, individual parts on the PWA can be changed in the field without appreciably changing drum balance if certain precautions are taken. These include using replacement parts of the same value, size, and weight and using only an adequate amount of solder. In addition, the Preamplifier PWA position on the drum should be marked in relation to the drum before loosening the mounting screws so that the PWA can be reinstalled in the same position as before removal. To remove the Preamplifier PWA from the scanner, proceed as follows:

STEP 1 Turn VPR-80 power off.

STEP 2 Loosen three screws securing cover to rotating scanner and remove cover. See Figure 5-45.

STEP 3 Unplug video head and erase head connectors.

STEP 4 Use a pencil to mark position of Preamplifier PWA with respect to drum. (Place pencil mark on drum opposite a mark on Preamplifier PWA in two places 90° apart.)

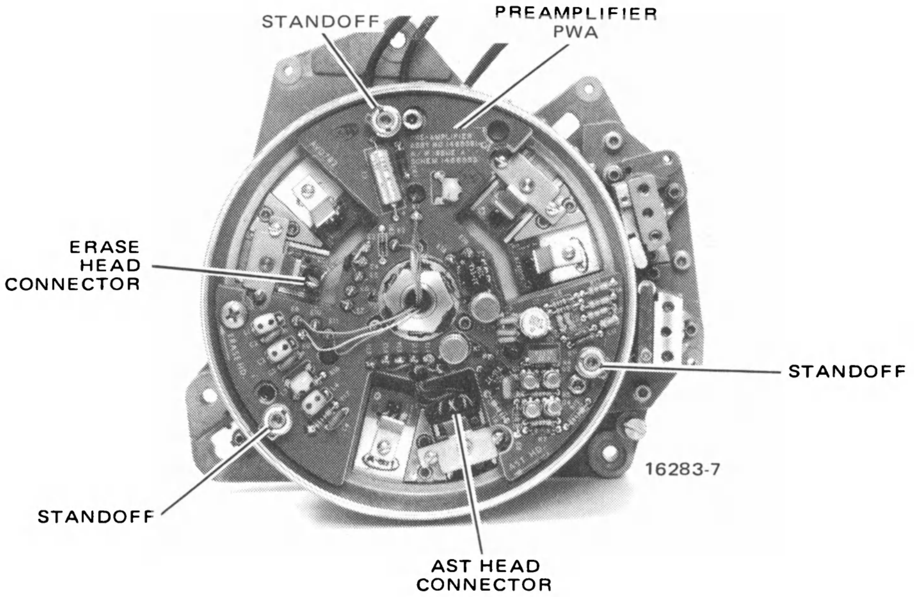


Figure 5-45. Removing Preamplifier PWA

STEP 5 Note color of leads supplied from slip-ring assembly and the four leads from rotary transformer. Table 5-5 provides information for identifying leads. Carefully unsolder leads from PWA terminals listed in table.

STEP 6 Remove three cover-mounting standoffs that also secure Preamplifier PWA to drum, then remove PWA. Remove a standoff as follows:

a. Remove retaining ring.

b. Remove compression ring.

c. Remove inner post (insert).

d. Unscrew outer post (standoff).

Table 5-5. Preamplifier PWA Terminal Assignment

Preamplifier PWA Terminal	Preamplifier PWA Terminal Wire/Color	Remarks
E1	Red, shield	Ground return
E2	Orange	+ 12 Vdc
E6	Bare, solid	Rotary transformer (erase)
E7	Bare, solid	Rotary transformer (erase)
E8	Green	AST sense return
E9	Yellow	AST sense
E10	Brown	(+) AST drive
E11	Blue	(–) AST drive
E18	Bare, solid	Rotary transformer (video)
E19	Bare, solid	Rotary transformer (video)

Note

Rotary transformer lead phasing is not critical.

Reference: Scanner Wiring Diagram No. 1461174

CAUTION

REPLACING PARTS ON THE PREAMPLIFIER PWA CAN SERIOUSLY DEGRADE SCANNER BALANCE. USE PARTS OF TYPE, WEIGHT, AND LEAD LENGTH IDENTICAL TO THE ORIGINAL. USE A LIKE AMOUNT OF SOLDER AND POSITION PARTS AS THEY WERE ORIGINALLY POSITIONED.

STEP 7 After parts are replaced on PWA, reinstall PWA on scanner drum in exact location marked in step 4. Secure PWA with standoffs removed in step 6.

STEP 8 Resolder leads and shield wires disconnected in step 5. Route leads as shown in Figure 5-45. When soldering leads use minimal solder to preserve dynamic balance.

STEP 9 Connect video and erase head connectors.

STEP 10 Reinstall scanner head cover. The cover is labeled and care should be used in positioning cover on scanner before securing with three screws.

5-116 Capstan Assembly

The following paragraphs cover replacement of parts within the capstan assembly. Instructions are given for replacement of the tach sensor, motor brushes, motor rotor, and capstan shaft.

5-117 Tach Sensor

The Capstan Tach PWA and tach sensor housing assembly are removed as a unit from the capstan assembly. Once removed, individual parts can be replaced in the field, with the exception of the glass tach sensor grating assembly located on the housing assembly. To remove tach sensor and housing from the capstan motor assembly, proceed as follows:

STEP 1 Remove capstan assembly from transport as described in paragraph 5-107, steps 1 through 10.

STEP 2 Remove two 6-32 crosshead screws that secure tach housing assembly to motor bell housing and remove tach housing assembly. See Figure 5-46.

STEP 3 Reinstall tach housing onto motor bell housing using screws removed in step 2. Do not tighten screws too firmly as tach phase must be set after capstan assembly is reinstalled.

STEP 4 Reinstall capstan assembly on transport casting and secure with three screws shown in Figure 5-33.

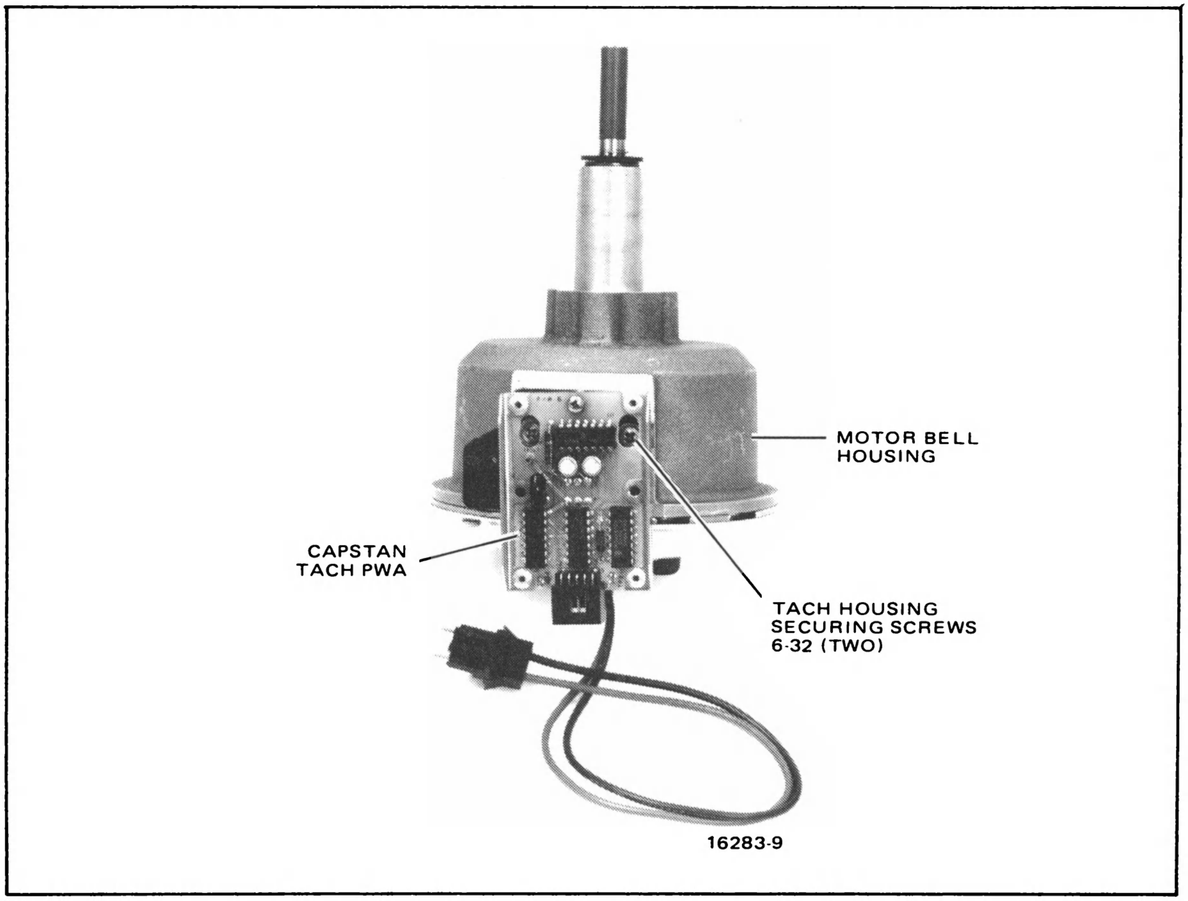


Figure 5-46. Capstan Tach PWA

STEP 5 Reconnect three capstan assembly connectors. Refer to Figure 5-32.

STEP 6 Adjust tach phase as described in paragraph 5-138.

STEP 7 Reinstall Audio PWA assembly (includes mounting plate and shield). Secure cables with tie wraps.

STEP 8 Raise card cage assembly to its normal operating position, and close rear door assembly.

STEP 9 Reinstall head cover and transport trim.

5-118 Motor Brushes

Capstan motor brushes are located inside motor brush plate assembly (rear cover), which is part of the capstan assembly. Brush replacement requires that the capstan assembly be removed from the transport. Brushes are replaced using Brush Replacement Kit (Ampex Part No. 1463500) which consists of two electrographite brushes with attaching 12-in. wire (one red and one black), spiked spade, connector pin, and a strain relief cable clamp. Proceed as follows:

STEP 1 Remove capstan assembly from transport as described in paragraph 5-107, steps 1 through 10.

STEP 2 Remove two screws and washers securing capstan motor brush plate to motor housing.

CAUTION

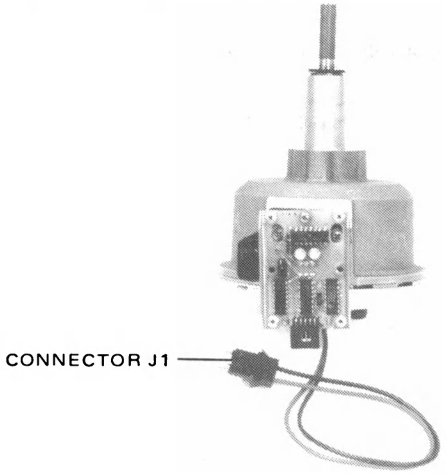
DURING NEXT STEP, DO NOT SLIDE SCREWDRIVER IN TOO FAR AS ROTOR DAMAGE CAN OCCUR. PULL MOTOR BRUSH PLATE STRAIGHT UP FROM MOTOR HOUSING—DO NOT SLIDE LATERALLY. DO NOT SCRATCH OR TOUCH PRINTED MOTOR ROTOR SURFACE, ESPECIALLY IN COMMUTATOR AREA.

STEP 3 The permanent magnet within the brush plate assembly tends to hold the plate to the motor front plate. Use a flat-bladed screwdriver placed in the slot in the front plate, located between the brush plate (rear cover) and the motor housing, to carefully pry plate up from the motor front plate. Then remove brush plate assembly. Temporarily remove capstan shaft thrust bearing and spring inserted in brush plate assembly. See Figure 5-47.

CAUTION

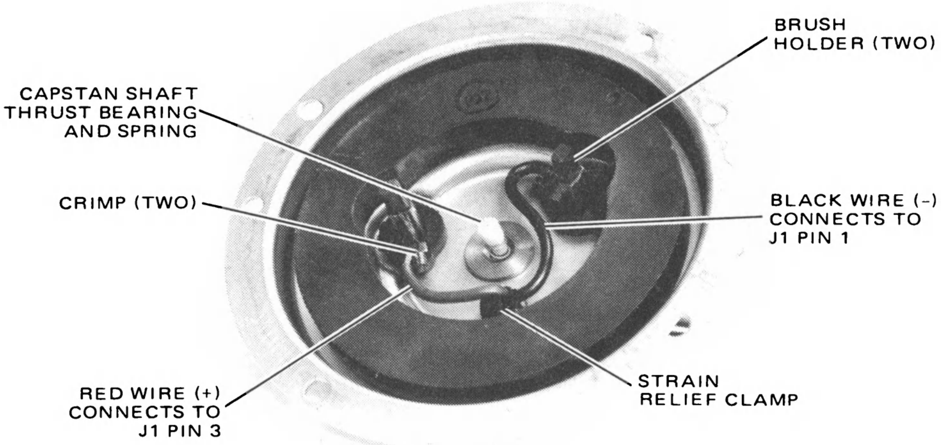
DO NOT ALLOW METALLIC PARTICLES TO GATHER ON PERMANENT MAGNET.

STEP 4 Use needle-nose pliers to pull crimp straight up to remove each spiked spade and brush from the two rubber grommets. Save the two brush



16283-9

CAPSTAN MOTOR ASSEMBLY



16283-12

BRUSH PLATE ASSEMBLY

Figure 5-47. Capstan Motor and Brush Plate Assemblies

holder springs. Cut and discard wires, but remove pins from connector J1 body and save body. Remove and discard strain relief clamp. See Figure 5-47.

STEP 5 Note that the outside of the brush plate assembly is identified (+) and (−). Insert springs saved in step 2 into brush holders. Install black wire replacement brush into (-) terminal and install red wire replacement brush into (+) terminal. Insert spiked spade into rubber grommet to secure. Brush should move freely in and out under spring pressure.

STEP 6 See Figure 5-47 for lead length and dress within brush plate assembly. Feed wires with attached male contact pins through hole and encircle wires with new strain relief clamp. Before inserting strain relief clamp into hole (from outside of brush housing), ensure there is minimum lead length within brush plate assembly.

STEP 7 Insert pins into connector body. The black wire is J1 pin 1, and the red wire is J1 pin 3.

STEP 8 Clean all contamination from magnet, brushes, and rotor using compressed air and then isopropyl alcohol. Remove all residue and allow surfaces to dry before proceeding.

STEP 9 Reinstall thrust bearing into spring on brush plate assembly and then reinstall motor brush plate on capstan motor housing securing with two screws and washers removed in step 2.

STEP 10 Reinstall capstan motor assembly and reinstall trim as described in paragraph 5-107, steps 11 through 15.

5-119 Motor Rotor

Replacing the capstan motor rotor requires disassembly of the capstan motor assembly. Proceed as follows:

CAUTION

USE EXTREME CARE NOT TO DAMAGE OR CONTAMINATE GLASS TACHOMETER DISKS OR URETHANE COATING ON CAPSTAN SHAFT.

STEP 1 To protect capstan shaft urethane coating, temporarily cover shaft with a snug piece of tubing 0.375 in. (9.525 mm) inside diameter.

STEP 2 Remove capstan assembly from transport as described in paragraph 5-107, steps 1 through 10.

STEP 3 Refer to Figure 5-46. Remove two 6-32 crosshead screws and washers that secure tach housing assembly to motor bell housing and remove tach housing assembly.

STEP 4 Remove two 6-32 screws securing capstan motor brush plate to motor bell housing. See Figure 5-48.

CAUTION

DURING NEXT STEP, DO NOT SLIDE SCREWDRIVER IN TOO FAR AS ROTOR DAMAGE CAN OCCUR. PULL MOTOR BRUSH PLATE STRAIGHT UP FROM MOTOR HOUSING—DO NOT SLIDE LATERALLY. USE CARE NOT TO SCRATCH OR TOUCH PRINTED MOTOR ROTOR SURFACE ESPECIALLY IN COMMUTATOR AREA.

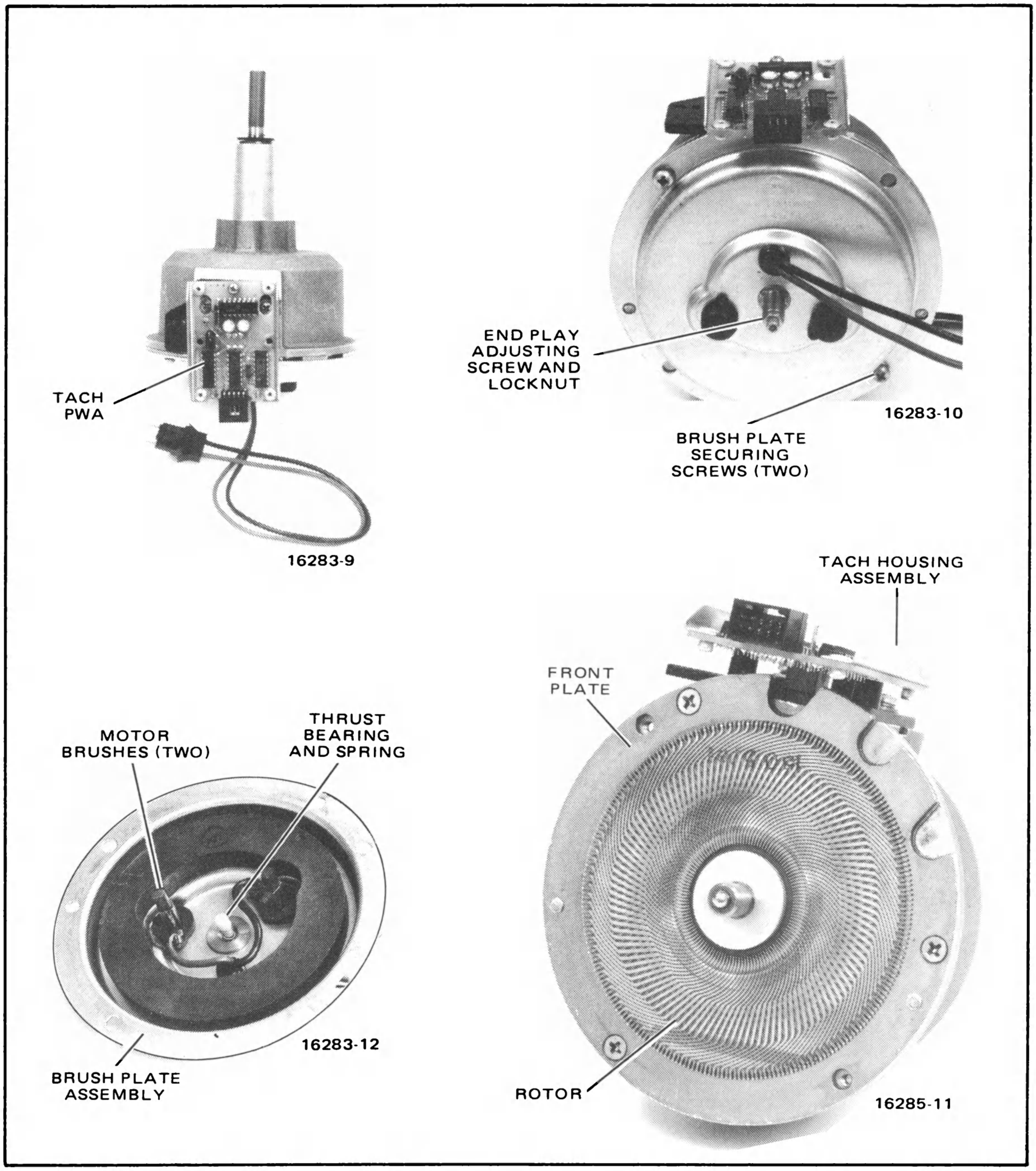


Figure 5-48. Capstan Assembly Components

STEP 5 The permanent magnet within the brush plate assembly tends to hold the plate to the motor front plate. Use a flat-bladed screwdriver placed in the slot in the front plate (slot located between the brush plate and the motor bell housing) to carefully pry plate up from motor front plate. Then remove brush plate assembly. Do not lose the thrust bearing or spring, shown in Figure 5-48, inserted in brush plate assembly.

CAUTION

DO NOT ALLOW METALLIC PARTICLES TO GATHER ON PERMANENT MAGNET.

STEP 6 See Figure 5-49. Remove rotor from capstan shaft by using a 9/64-in. setscrew wrench to remove the 8-32 cap screw and hardware that secure rotor to capstan shaft. Access to screw is through rectangular opening made visible by removal of tach housing assembly (step 3).

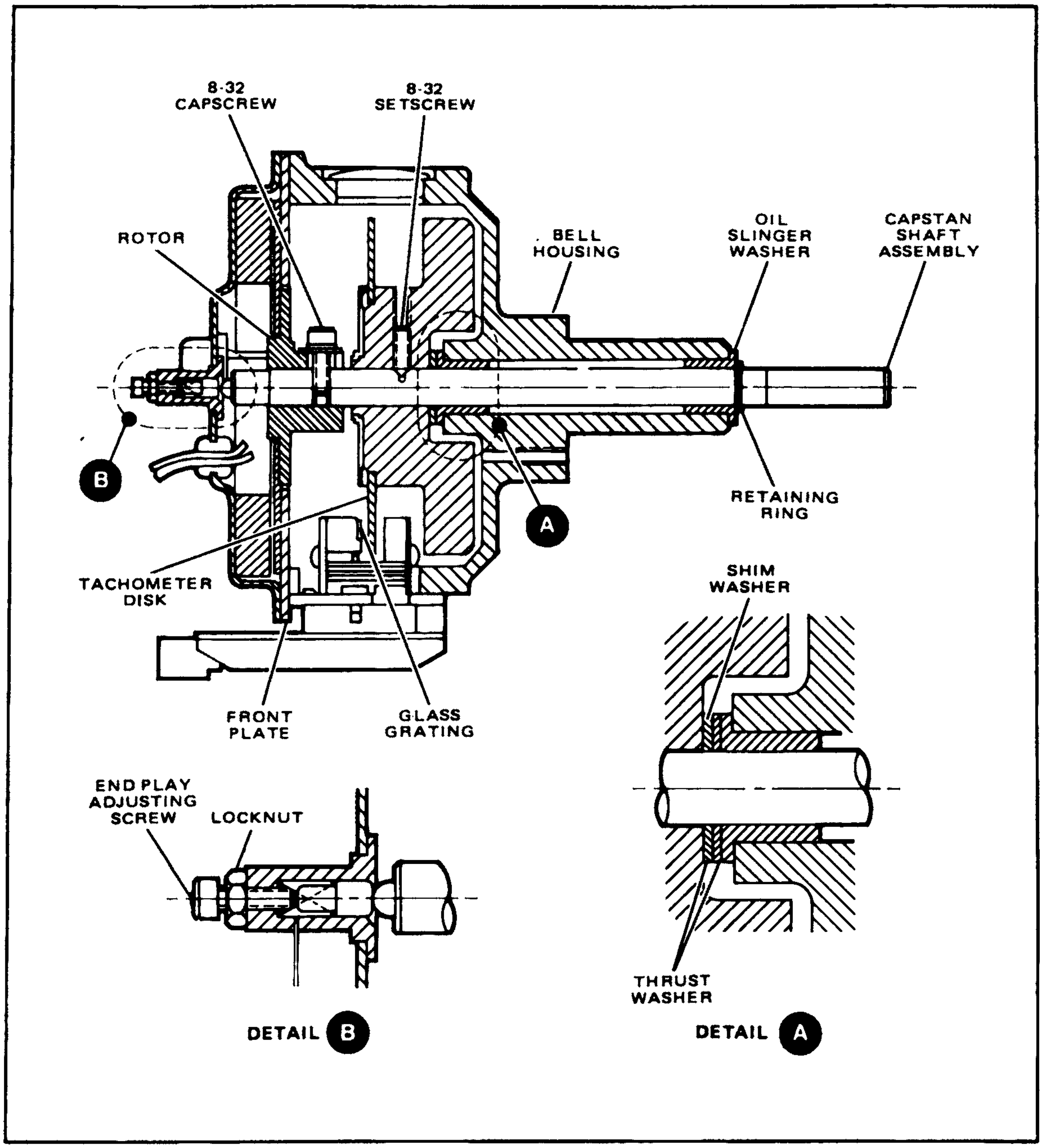


Figure 5-49. Capstan Assembly Cutaway Views

STEP 7 Rotor is installed on capstan shaft with a 0.015-in. (0.381-mm) clearance between rotor and front plate. Orient capstan shaft so that flywheel setscrew is visible through bell housing rectangular opening. Carefully place rotor onto shaft. Place a plastic 0.015-in. (0.381-mm) shim between rotor and front plate. With motor held vertically (rotor end up) so that flywheel is pressed against thrust washers (or single plastic washer), install cap screw and hardware removed in step 6 to secure rotor to capstan shaft. Use a torque wrench to torque screw to 16 in.-lb (1.81 Newton-meters). Remove plastic shim.

STEP 8 Use compressed air to remove all contamination from brushes, permanent magnet, and rotor. Use isopropyl alcohol to clean rotor surface.

STEP 9 Install spring and thrust bearing in place on brush plate assembly and reinstall motor brush plate on capstan motor housing using screws and washers removed in step 4.

STEP 10 Refer to Figures 5-48 and 5-49 and set capstan shaft end play as follows: Loosen no. 4 locknut. Turn end-play adjust screw counterclockwise and then turn clockwise until screw is tight. Then back off screw 1/8-turn and tighten locknut.

CAUTION

IN NEXT STEP, CLEAN GRATING GENTLY USING ISOPROPYL ALCOHOL SPARINGLY SO AS NOT TO DISSOLVE GRATING ADHESIVE.

STEP 11 Clean tach housing glass grating with a soft tissue moistened sparingly with isopropyl alcohol. Reinstall tach housing onto motor bell housing using screws removed in step 3.

STEP 12 Reinstall capstan assembly on transport casting and secure with three screws shown in Figure 5-33.

STEP 13 Reconnect the three capstan assembly connectors. Refer to Figure 5-32.

STEP 14 Remove protective tubing from capstan shaft and clean urethane coating with a soft tissue moistened with isopropyl alcohol.

STEP 15 Adjust capstan tach phase as described in paragraph 5-138.

STEP 16 Reinstall Audio PWA assembly (includes mounting plate and shield). Secure cables with tie wraps.

STEP 17 Raise card cage assembly to its normal operating position, and close rear door assembly.

STEP 18 Reinstall head cover and transport trim.

5-120 Capstan Shaft

Replacing the capstan shaft requires disassembly of the capstan assembly. Proceed as follows:

CAUTION

USE EXTREME CARE NOT TO DAMAGE OR CONTAMINATE URETHANE COATING ON CAPSTAN SHAFT OR DAMAGE GLASS TACHOMETER DISKS.

STEP 1 To protect urethane coating on new capstan shaft, slide a piece of electrical tubing, 0.375 in. (9.525 mm) inside diameter, over coated portion of shaft.

STEP 2 Remove capstan assembly from transport as described in paragraph 5-107, steps 1 through 10.

STEP 3 Refer to Figure 5-46. Remove two 6-32 crosshead screws and washers that secure tach housing assembly to motor bell housing and remove tach housing assembly.

STEP 4 Refer to Figure 5-48. Remove two 6-32 screws securing capstan motor brush assembly plate to motor bell housing.

CAUTION

DURING NEXT STEP, DO NOT SLIDE SCREWDRIVER IN TOO FAR AS ROTOR DAMAGE CAN OCCUR. PULL MOTOR BRUSH PLATE STRAIGHT UP FROM MOTOR HOUSING—DO NOT SLIDE LATERALLY. USE CARE NOT TO SCRATCH OR TOUCH PRINTED MOTOR ROTOR SURFACE ESPECIALLY IN COMMUTATOR AREA.

STEP 5 The permanent magnet within the brush plate assembly tends to hold plate to motor front plate. Use a flat-bladed screwdriver placed in slot in front plate, located between brush plate (rear cover) and motor bell housing, to carefully pry plate up from motor front plate. Then remove brush plate assembly. Do not lose thrust bearing and spring, shown in Figure 5-48, inserted in brush plate assembly.

CAUTION

DO NOT ALLOW METALLIC PARTICLES TO GATHER ON PERMANENT MAGNET.

STEP 6 Refer to Figure 5-49. Remove rotor from capstan shaft by using a 9/64-in. setscrew wrench to remove 8-32 cap screw and hardware that secures rotor to capstan shaft. Access to screw is through rectangular opening made visible by removal of the tach housing assembly (step 3).

STEP 7 Remove three 6-32 flathead screws and detach front plate from motor bell housing.

STEP 8 Using a 5/64-in. setscrew wrench, loosen the 8-32 setscrew that secures flywheel to capstan shaft and remove flywheel. Use care not to lose shim washer sandwiched by two thrust washers in recess of flywheel. (Refer to Figure 5-49, detail A).

Note

Some capstan motors have a single plastic washer instead of three washers.

STEP 9 Slide old capstan shaft out from top side of motor bell housing.

STEP 10 Note orientation of oil slinger washer and crescent retaining ring on capstan shaft. In transferring these parts to new capstan shaft do not slide parts over urethane coated portion of capstan shaft. The crescent ring can be removed by using a small screwdriver to push ring sideways off old shaft.

STEP 11 Ensure new shaft is clean, and lightly oil shaft with lubricant (Ampex Part No. 087-579) in area just below oil slinger washer.

STEP 12 Using care to protect coated portion of shaft (step 1), insert bottom end of shaft into top of motor bell housing until oil slinger washer contacts top of bell housing.

STEP 13 Ensure that shim washer and two thrust washers (noted in step 8) are clean. Lubricate both sides of shim washer with three drops of lubricant (Ampex Part No. 087-579). Then sandwich shim between two thrust washers and install onto capstan shaft.

STEP 14 Clean both sides of flywheel tachometer disk of all contamination (fingerprints, etc.) using a soft tissue moistened sparingly with isopropyl alcohol.

STEP 15 Position capstan shaft so that hole for flywheel setscrew is visible through bell housing rectangular opening. Then install flywheel and secure with setscrew loosened in step 6. Use a torque wrench to torque setscrew to 16 in.-lb (1.81 Newton-meters).

Note

Torque setting affects flutter.

STEP 16 Refer to Figure 5-48. Note orientation of front plate half-circle cutouts with respect to tach housing assembly. Reinstall front plate on motor bell housing using three flathead 6-32 crosshead screws removed in step 6.

STEP 17 Rotor is installed on capstan shaft with a 0.015-in. (0.381-mm) clearance between rotor and front plate. Orient capstan shaft so that flywheel setscrew is visible through bell housing rectangular opening. Carefully place rotor onto shaft. Place a plastic 0.015-in. (0.381-mm) shim between rotor and front plate. With motor held vertically (rotor end up) so that flywheel is pressed against thrust washers (or single plastic washer), install cap screw and hardware removed in step 6 to secure rotor to capstan shaft. Use a torque wrench to torque screw to 16 in.-lb (1.81 Newton-meters). Remove plastic shim.

STEP 18 Use compressed air to remove all contamination from brushes, permanent magnet, and rotor. Use isopropyl alcohol to clean rotor surface.

STEP 19 Ensure that thrust bearing and spring are in place on brush assembly and reinstall motor brush plate on capstan motor housing using screws and washers removed in step 4.

STEP 20 Refer to Figures 5-48 and 5-49 and set capstan shaft end play as follows:

a. Loosen no. 4 locknut.

b. Turn end-play adjust screw counterclockwise, and then turn clockwise until screw is tight.

c. Back off screw 1/8-turn and tighten locknut.

STEP 21 Clean tach housing glass grating with a soft tissue moistened sparingly with isopropyl alcohol. Reinstall tach housing onto motor bell housing using screws removed in step 3.

STEP 22 Reinstall capstan assembly on transport casting and secure with three screws shown in Figure 5-33.

STEP 23 Reconnect three capstan assembly connectors. Refer to Figure 5-32.

STEP 24 Remove protective tubing from capstan shaft and clean urethane coating with a soft tissue moistened with isopropyl alcohol.

STEP 25 Adjust capstan tach phase as described in paragraph 5-136.

STEP 26 Reinstall Audio PWA assembly (includes mounting plate and shield). Secure cables with tie wraps.

STEP 27 Raise card cage assembly to its normal operating position, and close rear door assembly.

STEP 28 Reinstall head cover and transport trim.

5-121 CLEANING

Cleaning instructions for slip rings, brushes, and rotor within the scanner, and for capstan motor brushes and rotor are given in the following paragraphs.

5-122 Scanner Slip Rings and Brushes

To ensure reliable performance, scanner slip rings and slip-ring brushes may require periodic cleaning. Recommended interval is 1000 hours of operation. Clean slip rings and slip-ring brushes with compressed air, or, if necessary, with freon. To clean slip rings and brushes, proceed as follows:

CAUTION

WHEN HANDLING SCANNER ASSEMBLY, BE CAREFUL NOT TO TOUCH PROTRUDING HEAD TIPS.

STEP 1 Remove scanner from transport as described in paragraph 5-106.

STEP 2 Install scanner service leg set assembly (Table 4-1, Part I,) on scanner and rest inverted scanner on work bench.

STEP 3 With rear of scanner facing upward, remove two screws securing motor cover to scanner assembly and remove cover. Refer to Figure 5-35.

STEP 4 Use compressed air to clean slip rings and brushes. If necessary, lightly spray freon on slip rings. See Figure 5-50. Turn drum slowly so that brushes wipe the slip rings. A cotton-tipped swab can be used to wipe slip rings if care is used to ensure that cotton filaments are not left behind to foul brushes. Permit slip rings and brushes to dry thoroughly before reinstalling motor cover.

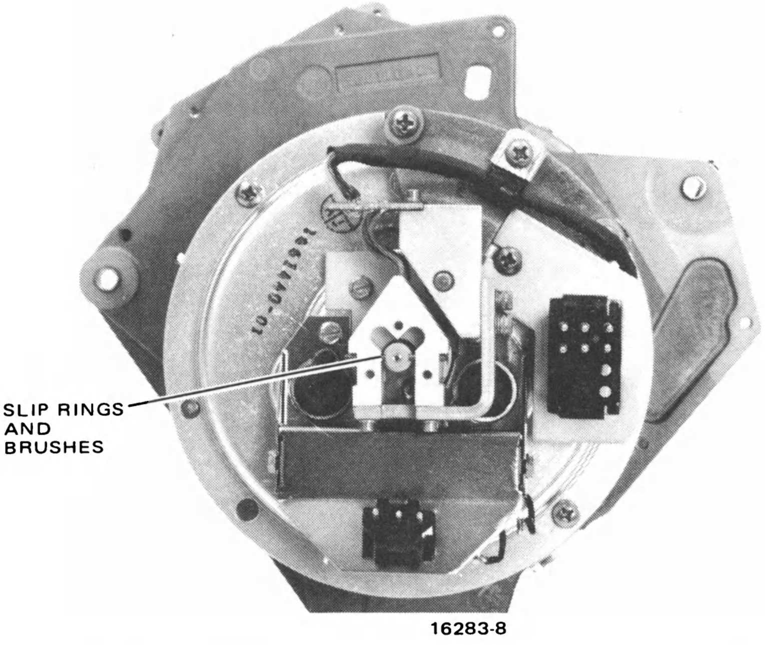


Figure 5-50. Scanner Slip Rings and Brushes

STEP 5 Reinstall motor cover removed in step 3.

STEP 6 Separate leg set from scanner, and reinstall scanner assembly on transport.

5-123 Scanner Motor Brushes and Rotor

For maximum scanner rotor life, scanner motor brushes and rotor should be cleaned after each 1000 hours of use. The cleaning procedure requires that scanner be removed from the transport. Proceed as follows:

STEP 1 Remove scanner assembly from transport as outlined in paragraph 5-106.

STEP 2 Install scanner on service leg assembly.

STEP 3 With rear of scanner facing upward, remove two 6-32 screws securing motor cover to drum adapter plate and remove cover.

STEP 4 Remove three 6-32 screws that secure brush support bracket to motor spacer. Refer to Figure 5-36.

STEP 5 Slide brush housing in direction shown in Figure 5-36, allowing brushes to snap together so that brush housing can be lifted free of slip-ring assembly.

STEP 6 Remove two no. 4 screws that secure printed circuit motor plate shield to brush plate assembly. Refer to Figure 5-38.

STEP 7 Remove two 6-32 screws that mount brush plate assembly to motor spacer (one side) and motor front plate (other side).

CAUTION

DURING NEXT STEP, DO NOT SLIDE SCREWDRIVER IN TOO FAR AS ROTOR DAMAGE CAN OCCUR. PULL MOTOR BRUSH PLATE STRAIGHT UP FROM MOTOR HOUSING. DO NOT SLIDE LATERALLY OR ROTOR DAMAGE CAN OCCUR. DO NOT SCRATCH OR TOUCH PRINTED MOTOR ROTOR SURFACE, ESPECIALLY IN COMMUTATOR AREA.

STEP 8 The permanent magnet within brush plate assembly tends to hold the plate to motor front plate. Use a flat-bladed screwdriver placed in slot provided in front plate to carefully pry plate up from motor front plate. Then remove brush plate assembly.

CAUTION

DO NOT ALLOW METALLIC PARTICLES TO GATHER ON PERMANENT MAGNET.

STEP 9 Use compressed air to clean rotor and brushes. If necessary, clean rotor surface with isopropyl alcohol and remove all residue. Clean motor brushes and interior of brush plate assembly with isopropyl alcohol. Remove all residue and allow brushes to dry.

STEP 10 Reinstall printed motor plate shield onto brush plate assembly and secure with screws removed in step 6.

STEP 11 Reinstall (and adjust as necessary) brush housing assembly by following instructions given in paragraph 5-14, steps 5 through 12.

STEP 12 Reinstall scanner into transport as described in paragraph 5-106.

5-124 Capstan Motor Brushes and Rotor

For maximum capstan rotor life, capstan motor brushes and rotor should be cleaned after each 1000 hours of operation. The procedure requires that the capstan motor be removed from the transport. Proceed as follows:

STEP 1 Remove capstan assembly from transport as described in paragraph 5-107, steps 1 through 10.

STEP 2 Remove two screws and washers securing motor brush plate to motor housing.

CAUTION

DURING NEXT STEP, DO NOT SLIDE SCREWDRIVER IN TOO FAR AS ROTOR DAMAGE CAN OCCUR. PULL MOTOR BRUSH PLATE STRAIGHT UP FROM MOTOR HOUSING—DO NOT SLIDE LATERALLY. DO NOT SCRATCH OR TOUCH PRINTED MOTOR ROTOR SURFACE, ESPECIALLY IN COMMUTATOR AREA.

STEP 3 The permanent magnet within the brush plate assembly tends to hold plate to motor front plate. Use a flat-bladed screwdriver placed in slot in front plate, located between brush plate (rear cover) and motor housing, to carefully pry plate up from motor front plate. Then remove brush plate assembly. Do not lose thrust bearing or spring, shown in Figure 5-48, inserted in brush plate assembly.

CAUTION

DO NOT ALLOW METALLIC PARTICLES TO GATHER ON PERMANENT MAGNET.

STEP 4 Use compressed air to remove all contamination from brushes, permanent magnet, and rotor. If necessary, use isopropyl alcohol to clean surfaces. Remove all residue and allow brushes to dry.

STEP 5 Ensure that thrust bearing and spring are in place on brush plate assembly, then reinstall motor brush plate on capstan motor housing.

STEP 6 Reinstall capstan motor assembly on transport casting as described in paragraph 5-107, steps 11 through 15.

5-125 SERVO SIGNAL SYSTEM ALIGNMENT

5-126 Reference Lock

The following adjustment optimizes the ability of the servo system to lock to externally supplied station reference and video inputs. Adjust reference lock as follows:

STEP 1 Mount AST Servo PWA on an extender.

STEP 2 Put Control PWA edge-mounted REF SELECT switch (6S5) in AUTO position.

STEP 3 Remove video and station reference video inputs, if any, at VIDEO IN and REF VIDEO IN connectors on I/O connector panel.

STEP 4 Turn VPR-80 power on and press EE. EE indicator should be lighted.

STEP 5 SYSTEM indicator should be lighted. Press SYSTEM and verify that system indication 03 is displayed.

STEP 6 Connect scope channel 1 probe to test point 4TP7 (REF FRAME) on AST Servo PWA. See Figure 5-66.

STEP 7 Connect external video signal input to scope channel 2. Trigger scope internally on channel 1.

STEP 8 Observing scope channel 2, adjust 4L2 on AST Servo PWA to minimize video drift. See Figure 5-66.

STEP 9 Remove scope probe. Reconnect video and station reference video inputs at I/O connector panel.

STEP 10 Return REF SELECT switch 6S5 on Control PWA to desired operational position.

STEP 11 Remove extender and reinstall AST Servo PWA in card cage.

5-127 AST System

The following adjustments should be made whenever a new video record/play AST head is installed. Make adjustments in the following sequence.

- Null frequency: see paragraph 5-129
- Damp phase and gain: see paragraph 5-130
- Jump track gain: see paragraph 5-131
- Jump track timing: see paragraph 5-132

5-128 AST Drive Centering

AST drive centering must be checked and adjusted whenever fault code **101-02** (**AST high voltage** fault) is displayed.

Adjustment of AST drive centering can affect VPR-80 interchangeability. After adjustment of AST drive voltages, refer to Section 4, Part I, and make the scanner tach measurement/adjustment outlined in paragraph 4-29.

WARNING

THE AST DRIVER PWA EMPLOYS HIGH VOLTAGES. USE EXTREME CARE WHEN MEASURING OR ADJUSTING VOLTAGES ON THIS PWA.

Note

Voltage measurements on the AST Driver PWA must be made with a high impedance digital voltmeter (10M or greater).

Check and adjust AST drive centering as follows:

STEP 1 With power off, open hinged transport cover and release catches so cover hangs below control panel.

STEP 2 Remove two screws (one from each side of control panel) and pivot control panel forward so that AST Driver PWA is accessible.

STEP 3 The plastic safety cover in front of the PWA is mounted on four standoffs. Disengage cover from each of four standoffs by placing two fingers beneath cover and pressing thumb on standoff.

STEP 4 Turn VPR-80 power on, and carefully measure dc voltage between AST Driver PWA test points TP7 and TPG1 or TPG3. Voltage should be +250 Vdc ±30 Vdc. See Figure 5-67. If voltage is not within tolerance, refer to Schematic Drawing No. 1450268 and check ac input rectification and filtering circuits. Otherwise, proceed to step 5.

STEP 5 Carefully measure dc voltage between AST Driver PWA test points TP6 and TPG2. Voltage should be -250 Vdc ±30 Vdc. See Figure 5-67. If voltage is not within tolerance, refer to Schematic Drawing No. 1450268 and check ac input rectification and filtering circuits. Otherwise, proceed to step 6.

STEP 6 Turn VPR-80 power off. Set section 8 of DIP switch 4S1 (TRACK JUMP TIMING) to closed position. This will turn on AST drive control and zero the error.

Note

Absolute value of voltages measured at test points TP5 and TP4 must be within 0.2 Vdc of each other.

STEP 7 Connect (+) voltmeter probe to test point TP5 (+ DRIVE) and (-) probe to a ground test point. Turn on VPR-80 power. Voltage should be +125 Vdc ½2 Vdc. Adjust R60 as necessary. See Figure 5-67. Turn off VPR-80 power.

STEP 8 Connect (-) voltmeter probe to test point TP4 (- DRIVE) and (+) probe to a ground test point. Turn on VPR-80 power. Voltage should be -125 Vdc ½2 Vdc. Adjust R53 as necessary. See Figure 5-67.

STEP 9 Ensure that absolute values of voltages at test points TP4 and TP5 are within 0.2 Vdc of each other. If not, repeat steps 7 and 8, as necessary.

STEP 10 Turn VPR-80 power off, and return section 8 of DIP switch 4S1 to open position.

STEP 11 Reinstall safety cover removed in step 3.

STEP 12 Refer back to Section 4, Part I of this manual and make scanner tach measurement/adjustment outlined in paragraph 4-29.

5-129 Null Frequency

Adjust null frequency as follows:

STEP 1 Thread a prerecorded work tape on transport. Ensure that tape is not in contact with video record/play AST head. Ensure that PWA edge-mounted AST ON/OFF switch on AST Servo PWA is ON.

STEP 2 Turn VPR-80 power on and leave in standby condition. (Do not press READY switch.)

STEP 3 Set scope vertical gain to 50 mV/cm, and connect scope probe to test point 4TP11 (AST ERROR). Set sweep to 2 ms/cm, and trigger scope on test point 4TP7 (REF FRAME).

STEP 4 Set section 8 of DIP switch 4S1 (TRACK JUMP TIMING) to closed position.

STEP 5 Press switch 4S2 (NULL TEST), and adjust 4R114 (NULL FREQ) for minimum amplitude of the 750-Hz waveform. See Figures 5-51 and 5-52.

STEP 6 Return section 8 of DIP switch 4S1 (TRACK JUMP TIMING) to open position.

5-130 Damping Phase and Gain

Adjust damping phase and gain as follows:

STEP 1 With a prerecorded work tape threaded on transport and VPR-80 power on, press READY. Ensure that EE indicator is not lighted and that scanner motor is up to lock speed.

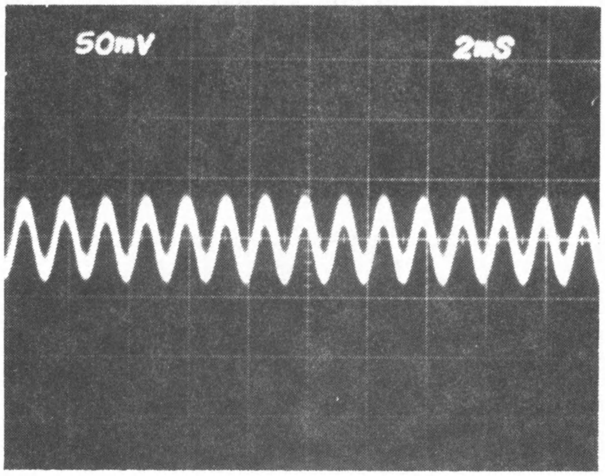


Figure 5-51. Null Frequency Amplitude Misadjusted

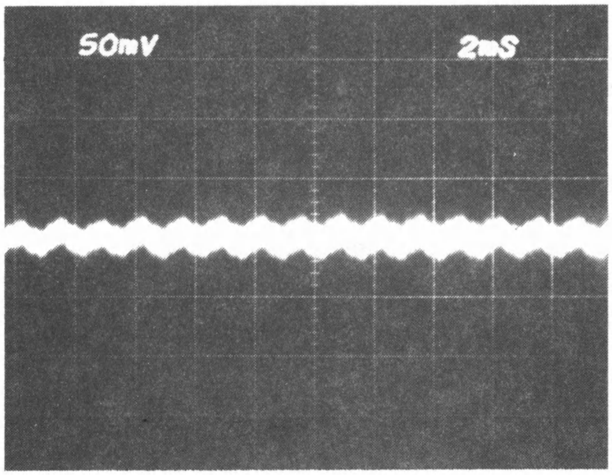


Figure 5-52. Null Frequency Amplitude Correctly Adjusted

STEP 2 Set section 7 of DIP switch 4S1 (TRACK JUMP TIMING) to closed position.

STEP 3 Set scope vertical gain to 500 mV/cm, and connect scope probe to test point 4TP10 (SENSE ERROR). Set sweep speed to 2 ms/cm, and trigger scope on test point 4TP7 (REF FRAME). Scope should display a reasonably stable sawtooth waveform.

STEP 4 Adjust 4R84 (DAMP PHASE) and 4R85 (DAMP GAIN) for no oscillation and minimum ringing as shown in Figure 5-53. These adjustments are interactive. Avoid underdamping (Figure 5-54) and overdamping (Figure 5-55).

STEP 5 Return section 7 of DIP switch 4S1 to open position.

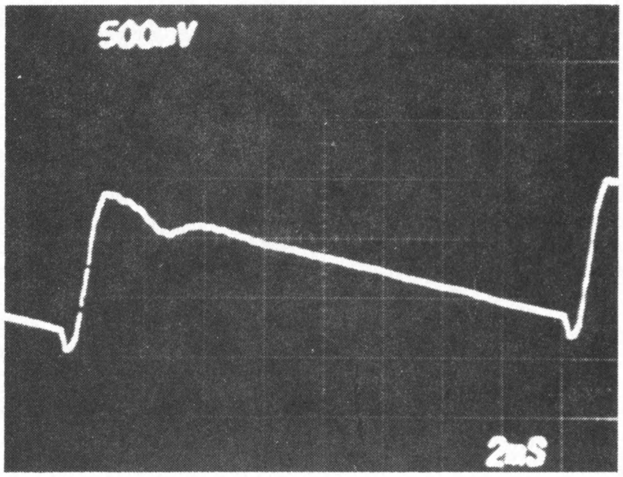


Figure 5-53. Damp Phase and Damp Gain Correctly Adjusted

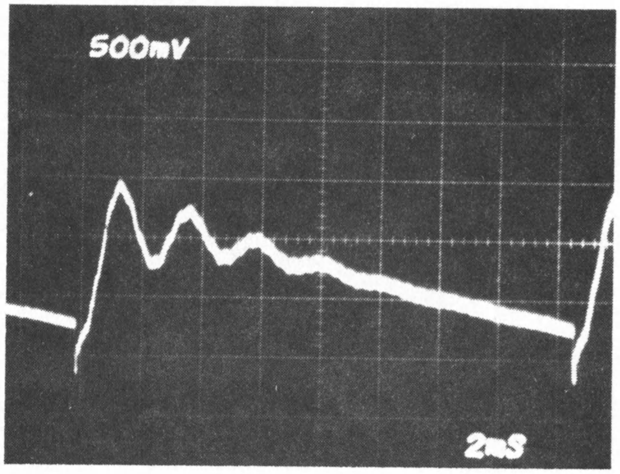


Figure 5-54. Damp Phase and Damp Gain Misadjusted (Underdamped)

5-131 Jump Track Gain

With the VPR-80 in stop mode/ready condition, and a prerecorded work tape threaded on the transport, adjust jump track gain. This is done in two stages: first a coarse adjustment, and then a fine adjustment as follows:

STEP 1 Set scope vertical gain to 50 mV/cm, and connect scope probe to playback rf seen at test point 1TP17 (INPUT RF) on Mod/Demod PWA. Set sweep speed to 5 ms/cm, and trigger scope on test point 4TP7 (REF FRAME).

STEP 2 For coarse adjustment, press VAR PLAY switch, and turn tape speed control full counterclockwise to variable play STOP position. Rf

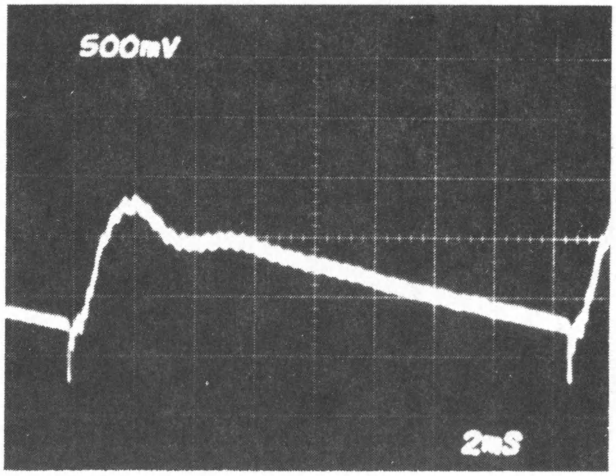


Figure 5-55. Damp Phase and Damp Gain Misadjusted (Overdamped)

envelope should be stable and nearly flat. If necessary, adjust 4R115 (JUMP LEVEL) to achieve this. See Figures 5-56 and 5-57.

STEP 3 Adjust tape speed control knob clockwise for a tape speed of 5-10 frames per second, and adjust 4R115 (JUMP LEVEL) for minimum rf envelope flicker.

STEP 4 Turn tape speed control knob full clockwise to 1.5 PLAY position. If necessary, adjust 4R115 again. Rf envelope should be flat and stable at all tape speeds. See Figures 5-58 and 5-59. Return tape speed control knob to STOP position.

5-132 Jump Track Timing

With the VPR-80 in variable-play mode/still-frame operation, a prerecorded work tape threaded on the transport, and scope probe, trigger, and vertical gain as set in paragraph 5-131, adjust jump track timing as follows:

STEP 1 Set scope sweep speed to 0.5 V/cm.

STEP 2 Adjust tape speed control knob for a tape speed of 5—10 frames per second, and observe rf envelope in vicinity of dropout interval. There will be some flicker as tracks jump, but both dropout edges should be clearly defined.

STEP 3 Edges of the rf envelope on each side of dropout interval should be symmetrical. Set switches 4S1-1 through 4S1-5 to achieve this. Figure 5-60 shows late track jump, and Figure 5-61 shows correctly timed track jump.

Note

Sections 1 through 5 of DIP switch 4S1 (TRACK JUMP TIMING) are binary weighted. Section 4S1-1 is binary 1; section 4S1-5 is binary 16.

Start timing adjustment by setting switch 4S1-5 (bit 16) to closed position and switches 4S1-1 through 4S1-4 to open position. This sets timing in the middle of adjustment range.

AST head alignment is complete when rf envelope appears as shown in Figure 5-62.

5-133 AFC Error

PWA-edge test point 4TP9 (AFC ERROR) should be at ground potential ±50 mV during normal play mode. Check and adjust AFC error as follows:

STEP 1 With VPR-80 power off, thread a prerecorded work tape onto the transport.

STEP 2 Connect a scope probe to test point 4TP9 (AFC ERROR) on AST Servo PWA. See Figure 5-66.

STEP 3 Turn on VPR-80 power and enter normal play mode. The average level should be ground potential ±50 mV. If not, continue with step 4 and subsequent steps.

STEP 4 With VPR-80 power off, install AST Servo PWA on an extender, and reconnect scope probe to test point 4TP9 (AFC ERROR).

Note

AFC error will be different when AST Servo PWA is mounted on extender.

STEP 5 Turn on VPR-80 power and observe waveform at test point 4TP9. If average level is too high when PWA is in place in card cage, adjust 4L1 (see Figure 5-66) to reduce indication. If average level is too low when PWA is in place in card cage, adjust 4L1 to increase indication.

STEP 6 Turn off VPR-80 power, disconnect scope probe, and remove extender.

STEP 7 Reinstall AST Servo PWA in card cage, and reconnect scope probe to test point 4TP9.

STEP 8 Turn on VPR-80 power and enter normal play mode. Average level should be ground potential ±50 mV. If not, repeat steps 4 through 8 until AFC error is within tolerance.

5-134 A/D Gain Trim

Adjust A/D gain trim as follows:

STEP 1 With VPR-80 power off, mount Servo PWA on an extender.

STEP 2 Connect (+) probe of digital voltmeter to pin 3 of A/D converter 5U8.

STEP 3 Connect (-) probe of digital voltmeter to ground test point 5TPG1.

STEP 4 Turn on VPR-80 power, and adjust 5R55 for indication of +5.7 Vdc at 5U8, pin 3.

STEP 5 Turn off VPR-80 power and disconnect DVM probes.

5-135 A/D Zero Offset

Adjust A/D zero offset as follows:

STEP 1 With VPR-80 power off, mount Servo PWA on an extender.

STEP 2 Put SCANNER PHASE switch 5S1, section 8 in closed position. See Figure 5-68.

STEP 3 Turn on VPR-80 power and observe that indicator 5DS1 (green LED) is off. Adjust 5R1 until indicator 5DS1 turns on and is lighted steadily. Adjust 5R1 to the center of its range which lights 5DS1.

STEP 4 Return section 8 of DIP switch 5S1 to open position.

STEP 5 Turn off VPR-80 power. Remove extender and reinstall Servo PWA.

5-136 Capstan Tach

Alignment of the capstan tach involves verification of maximum height and symmetry of the two tach output waveforms, and then verification of the 90° phase relationship between them.

5-137 Waveform Height and Symmetry

Adjust capstan tach waveform height and symmetry as follows:

STEP 1 Remove longitudinal head cover and transport trim as outlined in Part I, paragraph 4-12.

STEP 2 Loosen two captive screws at rear of cabinet, and lower card cage assembly.

STEP 3 Disengage four captive screws securing Audio PWA assembly (includes shield). Refer to Figure 5-31.

STEP 4 Cut two cable tie wraps on left-hand side of cabinet which secure cables to Audio PWA. Refer to Figure 5-31.

STEP 5 Detach Audio PWA assembly and lay it back to gain access to rear of capstan assembly.

STEP 6 Block tape-in-path sensor on Tape Timer Tach/TIP PWA.

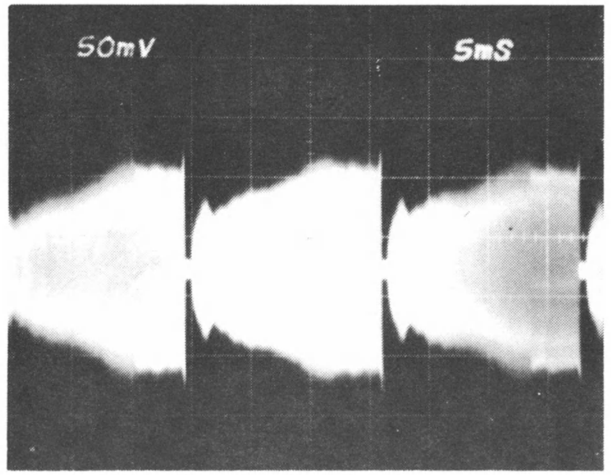


Figure 5-56. Jump Track Gain Misadjusted (Coarse Alignment)

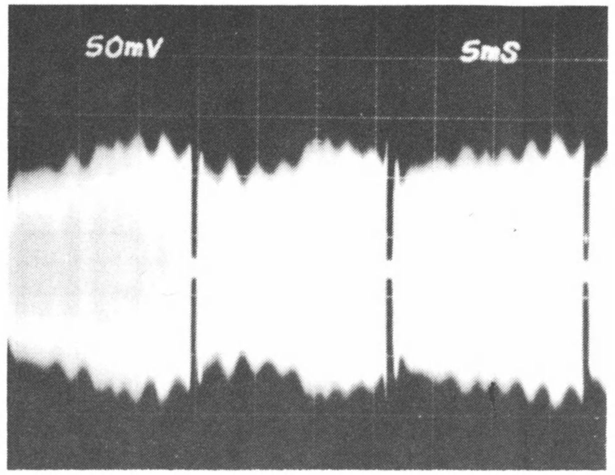


Figure 5-58. Jump Track Gain Misadjusted (Fine Alignment)

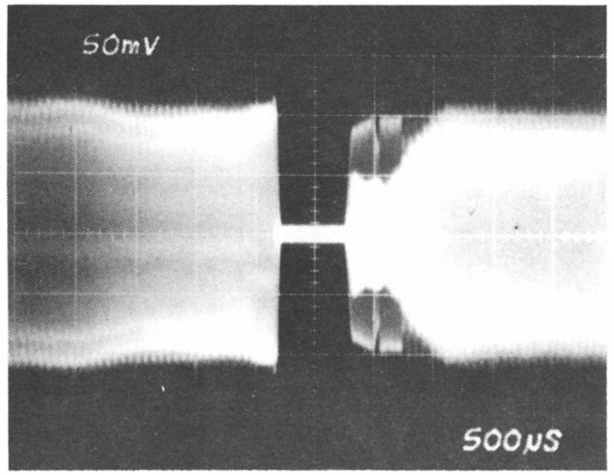


Figure 5-60. Jump Track Timing Misadjusted (Late)

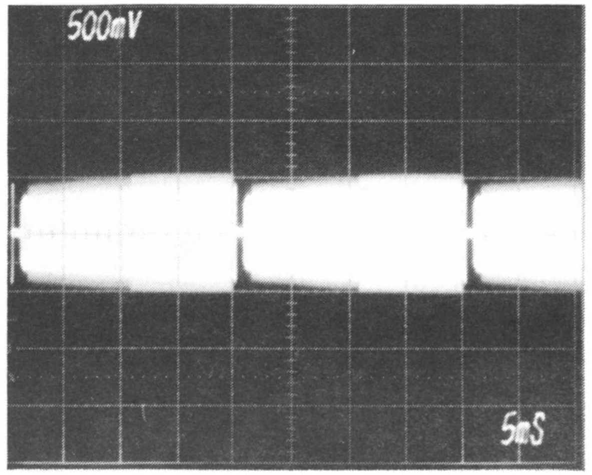


Figure 5-62. Correctly Aligned RF Envelope

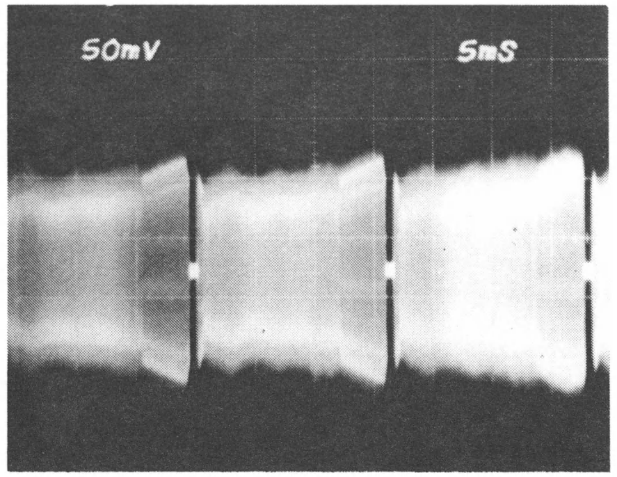


Figure 5-57. Jump Track Gain Correctly Adjusted (Coarse Alignment)

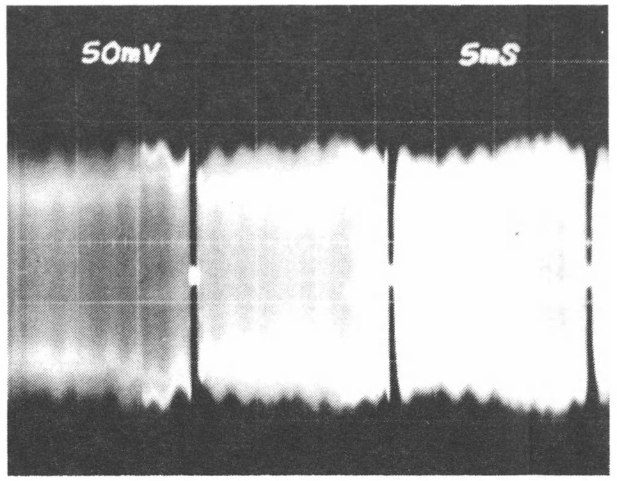


Figure 5-59. Jump Track Gain Correctly Adjusted (Fine Alignment)

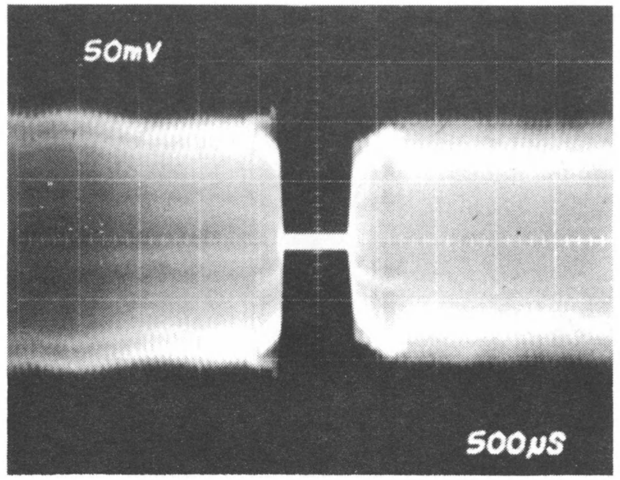


Figure 5-61. Jump Track Timing Correctly Adjusted

STEP 7 Turn VPR-80 power on and press PLAY.

STEP 8 Set scope vertical scale to 0.1 V/cm, and set horizontal scale to 1 ms/cm. With scope ac coupled, connect x10 probe to test point TP4 on Capstan Tach PWA. See Figure 5-69.

STEP 9 Adjust R3 for maximum peak-to-peak sine wave. Disregard any clipping that may occur as R3 is adjusted.

STEP 10 Set scope horizontal scale to 0.1 ms/cm, and move scope probe to test point TP1. Verify a TTL logic level square wave.

STEP 11 Readjust R3 for symmetrical square wave (50% duty cycle).

STEP 12 Set scope horizontal scale to 1 ms/cm, and move scope probe to test point TP3.

STEP 13 Adjust R2 for maximum peak-to-peak sine wave. Disregard any clipping that may occur as R2 is adjusted.

STEP 14 Set scope horizontal scale to 0.1 ms/cm, and move scope probe to test point TP2. Verify a TTL logic level square wave.

STEP 15 Readjust R2 for symmetrical square wave (50% duty cycle).

STEP 16 Press VPR-80 STOP and remove scope probes.

5-138 Tach Pulse Phasing

Assuming that VPR-80 is in the same configuration as at the end of the procedure in the preceding paragraph, continue by adjusting phase relationship of tach pulses as follows:

STEP 1 Set scope to chop mode, and set vertical scale for channels 1 and 2 to 0.2 V/cm. Set horizontal scale for channels 1 and 2 to 0.1 ms/cm. Trigger from channel 1.

STEP 2 Connect scope channel 1 probe to test point TP1; connect scope channel 2 probe to test point TP2.

STEP 3 Press VPR-80 PLAY and observe phase relationship of two tach pulse waveforms.

STEP 4 Waveform on channel 2 should lead waveform on channel 1 by 90°. If not, loosen two cross-recessed screws which are accessible through holes in Capstan Tach PWA. See Figure 5-63.

STEP 5 Observing scope, grasp black plastic slide adjustment and move it toward or away from the PWA, as required, to achieve a 90° phase relationship between the two tach pulses.

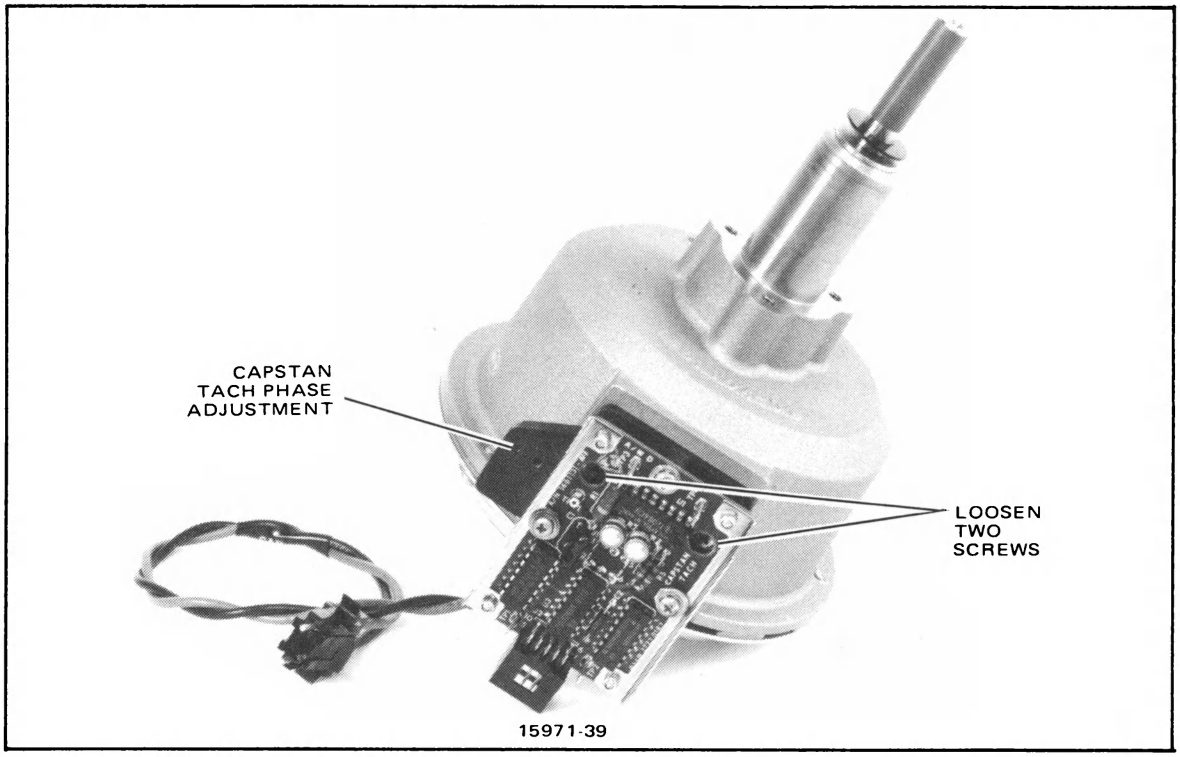


Figure 5-63. Capstan Tach Phasing Adjustment

STEP 6 Tighten two screws which were loosened in step 4 to preserve adjustment.

5-139 Capstan Tach Filter

The capstan tach notch filter eliminates carrier at play speed. Adjust capstan tach filter as follows:

STEP 1 With VPR-80 power off, mount Servo PWA on an extender.

STEP 2 Connect scope probe to test point 5TP17 (CAPSTAN ERROR), ac coupled. See Figure 5-68.

STEP 3 Thread a work tape on transport, and turn on VPR-80 power.

STEP 4 Enter record mode and adjust scope as required to see high-frequency component in analog signal.

STEP 5 Observing scope, adjust 5R137 for minimum amplitude of high-frequency component in analog signal. See Figures 5-64 and 5-65.

5-140 Scanner Tach

The procedure for alignment of the scanner tach is included in the interchange procedures. Refer to Section 4, Part I.

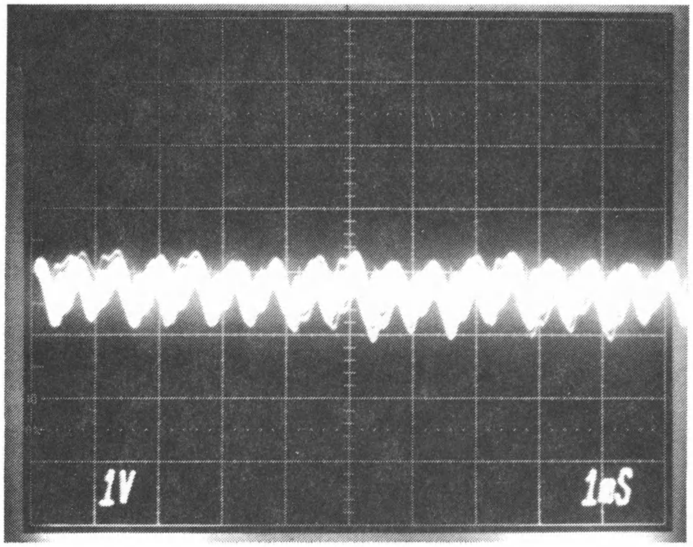


Figure 5-64. Capstan Tach Filter Misadjusted

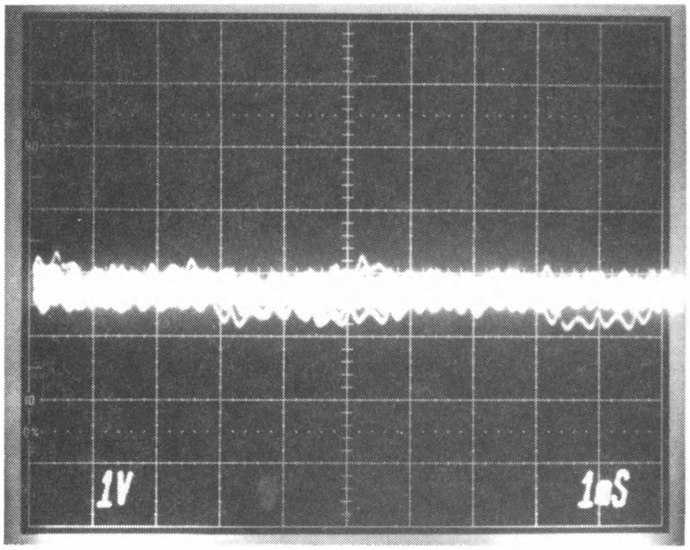


Figure 5-65. Capstan Tach Filter Correctly Adjusted

5-141 Tension Arm Assembly

Adjust tension arm position signal as follows:

STEP 1 With VPR-80 power off, mount Servo PWA on an extender.

STEP 2 Turn on VPR-80 power. Using digital voltmeter in bipolar mode, measure voltage at pin contact 82 on PWA edge connector (XA5-82). (This is TENSION ARM POSITION input to analog multiplexer 5U2.)

STEP 3 Move tension arm to right-hand stop. Verify that voltage at XA5-82 is +6.00 Vdc +0.05, -0.00 Vdc when tension arm is against right-hand stop.

STEP 4 Slowly move tension arm to the left. Voltage should decrease to 0V, and it should be -6.00 Vdc +0.00, -0.05 Vdc when tension arm is at left-hand stop.

If tension arm position voltage is not as specified in steps 3 and 4, continue as follows:

STEP 5 Remove longitudinal head cover and transport trim as outlined in Part I, paragraph 4-12.

STEP 6 With power off, loosen two captive screws at rear of cabinet, and lower rear door assembly as shown in Figure 4-3, Part I.

STEP 7 Disengage four captive screws securing Audio PWA assembly (includes shield). Refer to Figure 5-31.

STEP 8 Detach Audio PWA assembly and lay it back to gain access to rear of tension arm assembly.

STEP 9 Turn on VPR-80 power. Measure voltage at XA5-82. It should be 0.00 Vdc when tension arm is in center position. If not, adjust R1 on Photo Potentiometer PWA (part of tension arm assembly—see REFERENCE 5-5) for 0.00-Vdc indication at XA5-82.

STEP 10 While monitoring voltage at XA5-82, adjust R5 on Photo Potentiometer PWA for indication of +6.00 Vdc +0.05, -0.00 Vdc when tension arm is against right-hand stop, and for indication of -6.00 Vdc +0.00, -0.05 Vdc when tension arm is against left-hand stop.

Note

Adjustments with R1 and R5 are interactive. Repeat steps 9 and 10 as necessary.

5-142 Tension Setup

The following is the tension setup procedure. Tension measurements are made with the Tentelometer Gauge (Table 4-4).

Step 1 Remove longitudinal head cover and transport trim as outlined in Section 4, Part 1 (paragraph 4-12).

Step 2 With power off, loosen two captive screws at rear of cabinet and lower rear door assembly as shown in Section 4, Part I (Figure 4-3).

Step 3 Disengage four captive screws securing Audio PWA Assembly (includes shield). Refer to Figure 5-31.

Step 4 Cut two cable tie wraps on left-hand side of cabinet which secures cables to Audio PWA. Refer to Figure 5-31.

Step 5 Detach Audio PWA assembly and lay it back to gain access to LED and Photo Potentiometer PWAs.

Step 6 Attach scope probe to E1 on LED PWA.

Step 7 With tension arm adjust R1 on Photo Potentiometer PWA for 0V.

Step 8 Move tension arm lever from one stop to its other stop and adjust R5 on Photo Potentiometer PWA for +6V and -6V.

Step 9 On transport, adjust serrated lever on longest spring connected to tension arm for 4 1/2 oz ±0.25 (127g ±7g) of tape tension at scanner entrance guide.

Step 10 In slow forward shuttle, adjust serrated lever on smallest spring for 2 oz ±0.25 oz (57g ±6g) of tape tension at supply reel.

Step 11 In fast rewind, adjust serrated lever on intermediate size spring for 14 oz ±0.50 oz (395g ±15g) of tape tension at supply reel.

Step 12 Verify in play or record mode that tape tension at the take-up real is 16 oz ±1 oz (454g ±28g).

Step 13 Verify in still mode that tape tension at the take-up real is 5 oz ±0.25 oz (142g ±7g).

Step 14 If tape tension verification in steps 12 and 13 are not accurate, repeat steps 9, 10, and 11.

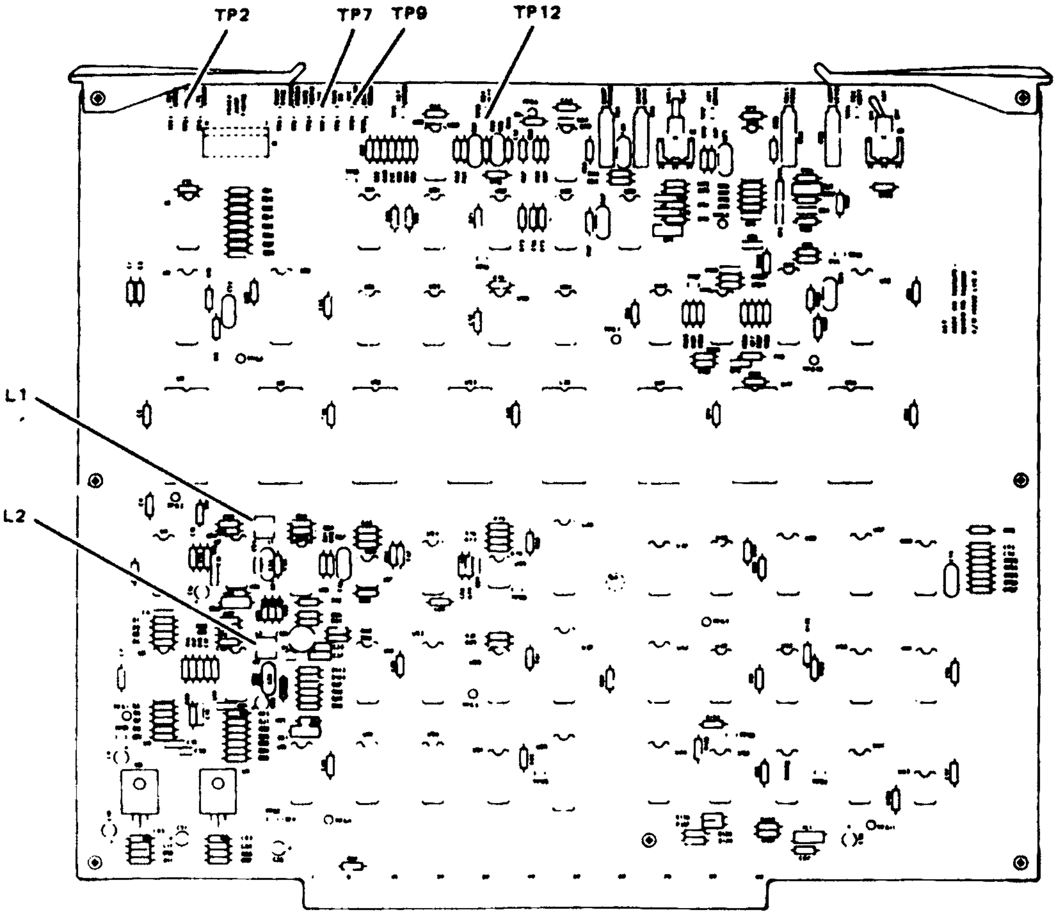


Figure 5-66. AST Servo PWA Test Points and Adjustments

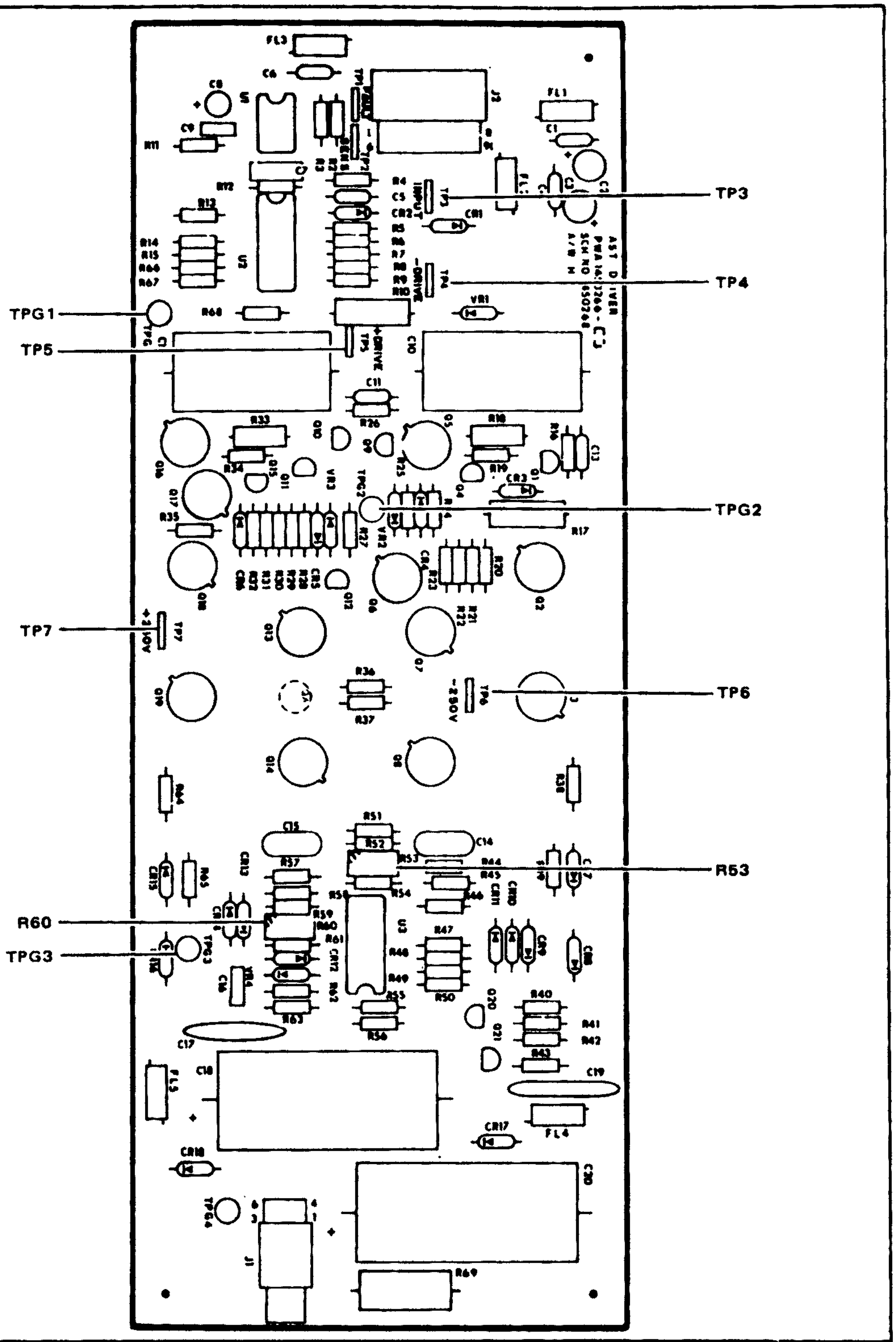


Figure 5-67. AST Driver PWA Test Points and Adjustments

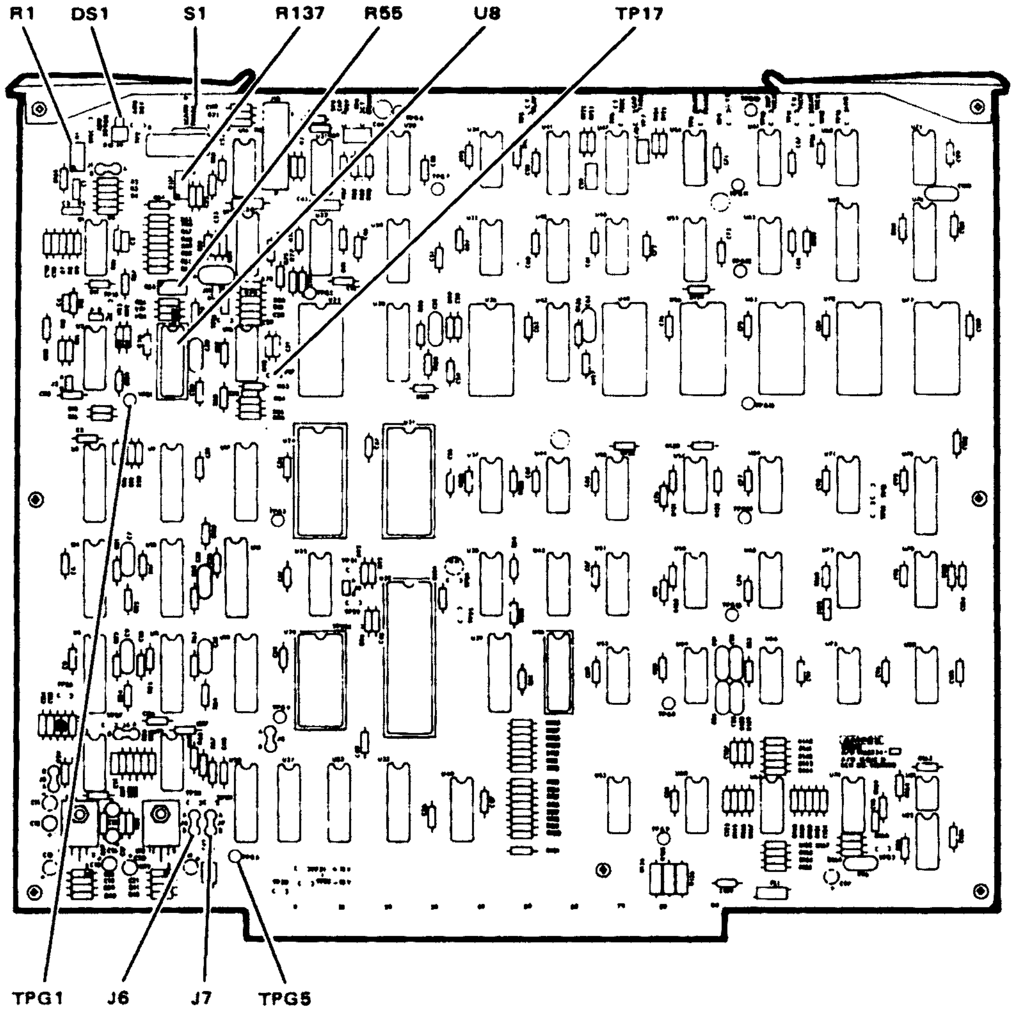


Figure 5-68. Servo PWA Test Points, Jumpers, and Adjustments

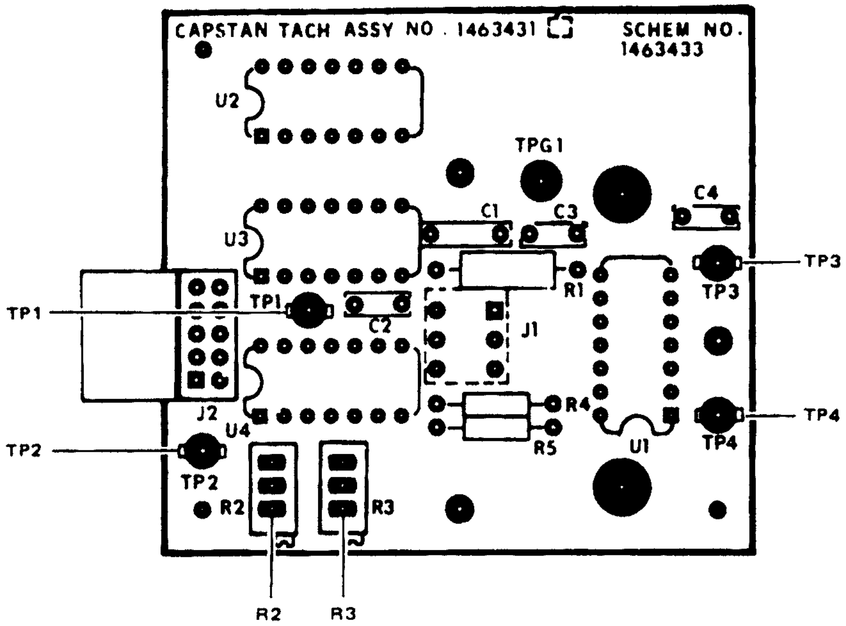


Figure 5-69. Capstan Tach PWA Test Points and Adjustments

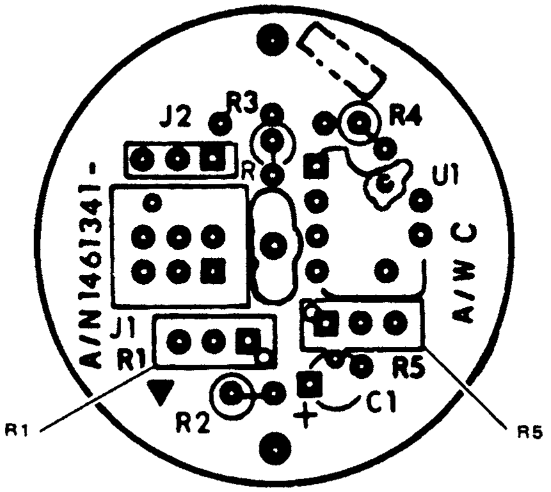


Figure 5-70. Photo Potentiometer PWA Adjustments

PART II
SECTION 6
CONTROL SYSTEM

6-1 GENERAL

This section provides theory of operation information for the control system. Instructions are given for removing and reinstalling the control panel assembly and the timer idler assembly. Procedures replacing parts within these assemblies are also given. Alignment of the tape timer tach is explained, and complete control system performance verification procedures are spelled out.

The following drawings, which are included in the *VPR-80 Parts Lists and Schematics* manual, are referenced in this section.

Drawing	Drawing No.
Control PWA	1465505
Control PWA Schematic	1465507
Primary Control Panel PWA	1450660
Primary Control Panel PWA Schematic	1450662
Secondary Control Panel PWA	1450640
Secondary Control Panel PWA Schematic	1450642
Timer Idler Assembly (525/60)	1461160
Timer Idler Assembly (625/50)	1461161
Tape Timer Tach/TIP PWA	1468560
Tape Timer Tach/TIP PWA Schematic	1468562
System Interconnect Wiring Diagram	1465497

In addition, the following are included at the end of this section.

Table 6-6. Control PWA Jumpers and Test Points
Figure 6-21. Tape Timer Tach/TIP PWA Adjustment Controls

6-2 THEORY OF OPERATION

6-3 Control System Concept

The VPR-80 can be commanded to exit any current mode and enter any other mode. Primary tasks of the control system are:

- To interpret a mode change command (whether manually entered at the control panel or received from a remote source).
- To poll the Reference PWA configuration and the status of the transport and servo systems for readiness to execute the command.
- To ensure that the command has been executed.

Recognition and interpretation of a mode change command are done by the control system microprocessor (CPU) and its firmware. Mode modification, coarse edit timing, and mode control qualification are also handled by the CPU and firmware.

6-4 Mode Change Commands

Figure 6-1 is a block diagram of the VPR-80 control system concept. Mode change commands are shown entering on the left-hand side. All control inputs, whether from switches on the local control panel or remote commands, are placed in latches and read by the CPU via the data bus during every vertical interval, or as determined by the firmware. Therefore, once the operator has manually entered a command by switch closure, execution of the command is almost entirely in the firmware domain.

The first CPU function is switch debounce logic. All control inputs are sampled during vertical intervals. Inputs must be present for one more vertical interval before they are passed along to mode request logic.

6-5 Mode Modification

If control input is shuttle, play, or cue mode command, mode request logic first holds the request to see if it is modified. Closure of SHUTTLE, PLAY, VAR PLAY, and CUE switches, if made twice in succession (or if repeated after the command is asserted), modify the mode change request. These switches do not then command the primary modes indicated, but instead command unthread, auto edit review, pause, and cue without preroll, respectively, which are modifications of the primary modes. After determining whether mode modification is necessary, the command is returned to the mode control logic.

6-6 Edit Timing

If the control input indicates record mode, mode control logic looks at auto edit status. If auto edit condition is asserted, timing and control of the edit record sequence will be done by comparing current tape time with preset values in the entrance and exit registers. Thus, record mode command is modified to auto edit record command. The CPU ensures that the tape has been cued. If tape has not been cued, the CPU causes the SYSTEM indicator to light (system code 13) and prevents issuance of record mode command to the hardware.

The CPU provides coarse edit timing by enabling timers 1 (6U27) and 2 (6U32) after determining hardware readiness. Timer outputs provide fine edit timing by initiating edit interrupts (INT 4—INT 7) synchronized with current tape time. Thus auto edit timing is shared by hardware and firmware. Timers govern switching of all video timing, audio erase, audio record exit, and audio record entrance (in that order).

6-7 Mode Control Qualification

Mode control logic (firmware) cannot issue commands to the audio, video, servo, or transport systems without regard for the current status of each of the other systems. The mode change request is processed by the CPU, and all necessary control system outputs are issued under qualifying statements (flags) from

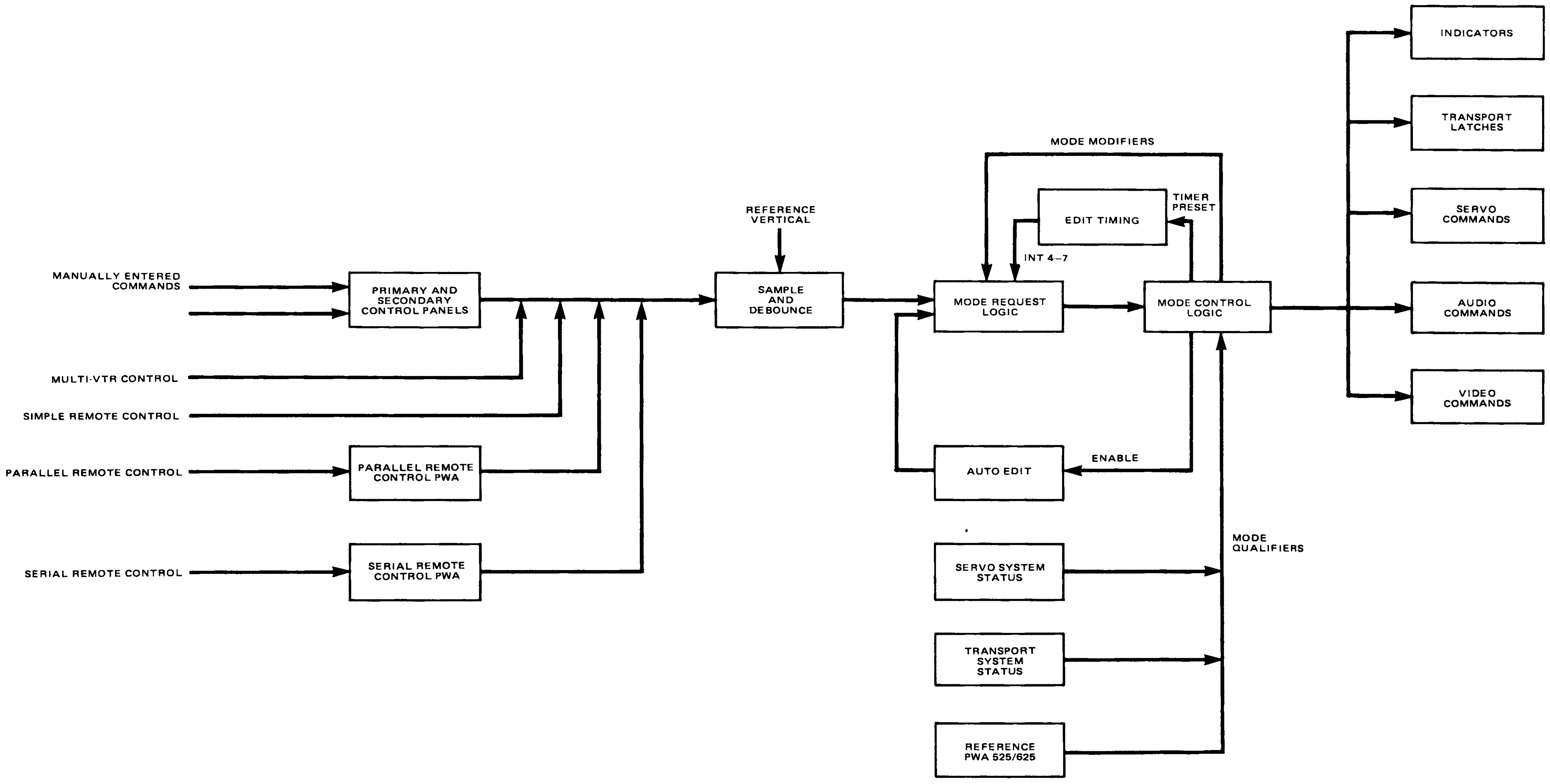


Figure 6-1.
Control System Concept

transport and servo systems. Configuration of the Reference PWA (525-line or 625-line standard) also qualifies control system outputs.

Assume that an entrance edit point (cue) is in reverse tape direction and CUE is pressed while the transport is in full speed forward shuttle mode. The only hardware changes that are affected immediately are those of turning off the SHUTTLE indicator, turning on the CUE indicator, and removing effectiveness of the tape speed (shuttle) control knob. Cue mode obviously cannot be entered immediately. The cue mode command must be qualified until shuttle mode can be exited. Firmware logic looks at tape time and direction (tape timer tach) and the relative position of the cue. Forward tape motion must be decelerated to a stop and then started in reverse direction in search of the cue. The shuttle command is not actually terminated and the cue command is not actually initiated by mode control logic until tape comes to a stop. Thus, the cue command is qualified before its execution can be effected.

A qualifying statement from the servo system can be as simple as the prevention of tape motion until the scanner motor reaches lock speed. Similarly, the transport system can abort all commands involving tape motion if the TIP sensor detects that tape has not been threaded. In all cases, configuration of the Reference PWA qualifies all commands which produce different results between 525-line and 625-line systems (i.e., frame count per second, 5- or 7-second preroll).

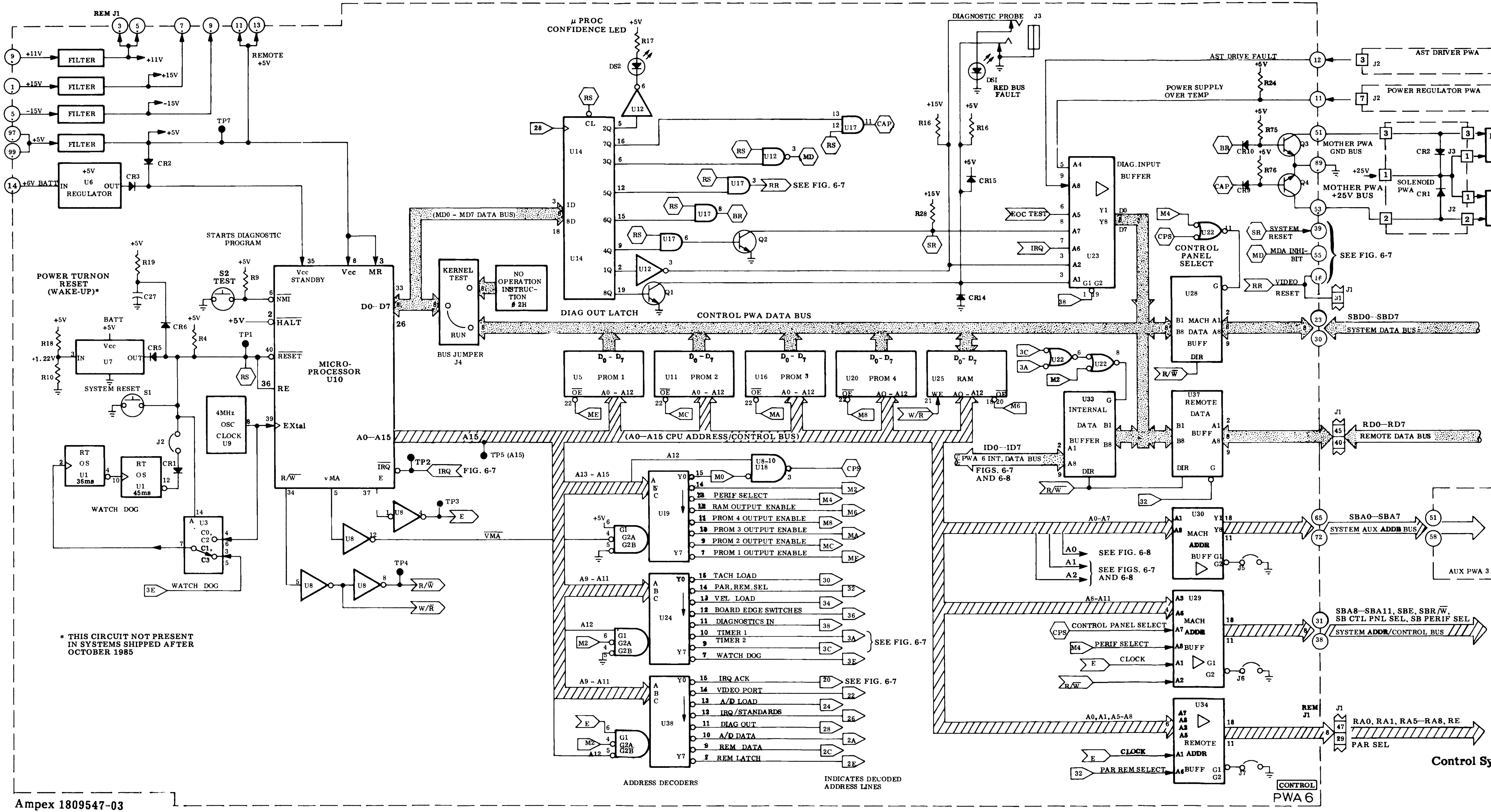
6-8 Control System Kernel

The control system kernel is shown in Figure 6-2. It is composed of an 8-bit microprocessor (CPU) and chips which are connected to the CPU when jumper J4 is in TEST (A-B) position. Thus, the kernel includes 32K bytes of erasable programmable read-only memory (EPROM), 1024 bytes of random access memory (RAM), 4-MHz crystal oscillator, primary address decoders, diagnostic input buffer, and diagnostic output latch.

6-9 Microprocessor

Microprocessor (CPU) chip U10 is an 8-bit, NMOS processor (Motorola Type MC6802A) with internal clock countdown circuit and 128 bytes of internal RAM storage. A total of 32 bytes of the internal RAM storage is protected by battery backup. The address bus output presents 16 address bits in parallel and is thus capable of accessing 64K of memory. Characteristics of each of the CPU I/O signals are described in detail on the CPU data sheet which is included in Appendix A of the *VPR-80 Parts Lists and Schematics* manual. The CPU is Ampex Part No. 589-759. The BA (bus available), xtal (1-MHz crystal), and halt input connections are not used in this application.

6-10 Power, Clock, Reset, and NMI Inputs. The regulated and filtered +5V supply is applied at U10 Vcc input pin 8. It is also applied to MR (memory ready) input pin 3. The MR input must be held high to insure the 1-MHz frequency of the E (enable) output at pin 37. Regulated +5V from the voltage regulator circuit (U6) is applied to the Vcc standby input pin 35.



* THIS CIRCUIT NOT PRESENT IN SYSTEMS SHIPPED AFTER OCTOBER 1985

Figure 6-2. Control System Kernel Block Diagram

Crystal oscillator U9 supplies a 4-MHz clock to U10 EXtal input pin 39. The CPU internal divide-by-four circuit provides the 1-MHz clock for the CPU and the 1-MHz E (enable) output which strobes address decoder U38 and clocks the two edit timers, U27 and U32. The E output becomes the system clock (SBE) on the system bus which is external to the Control PWA.

Reset and RE (RAM enable) input pins 40 and 36 are held high during normal CPU operation. reset is active low, and RE, which enables the internal 128 x 8 RAM, is active high. A reset can be applied to the CPU in four ways: power-up reset, watchdog timeout, manual reset, and decay of the +5V supply.

Power-up reset is automatically applied to the CPU when power is initially turned on or when it resumes after an outage. When power comes up initially, the CPU is held in reset during the R4/C27 time constant. The power-up reset also establishes a starting address for the CPU program counter. When C27 is fully charged, the reset is removed, and the CPU begins the initialization routine.

The watchdog timer is composed of one-shots U1-4 and U1-12 and selector circuit U3. The watchdog prevents the CPU from entering a repetitive loop of subroutine activity which can only be exited by power-down/power-up reset. The watchdog timer looks at address 3EXX (hex) which occurs with regularity throughout CPU operation. The repeated assertion of watchdog address 3EXX (address decoder U24-7) keeps the output of one-shot U1-12 high. If address 3EXX does not recur within timeout of the retriggerable one-shots (81 ms), the output at U1-12 resets the CPU. When reset, the CPU stores current tape time and cues in RAM 1, the battery-supported RAM storage within CPU U10.

In normal operation, select input to U3-14 is high, and address 3EXX is routed from address decoder U24-7 to one-shot U1-2 through C1 and C3 inputs of selector U3. During reset or power down, the selector switches to the C0 and C2 inputs, to which 4-MHz clock pulses are applied. On power-up, the clock inputs to the watchdog timer trigger U1-4 (and U1-12), thus removing the low reset output of the watchdog. Without this start-up circuit, a watchdog reset would be asserted if address 3EXX did not occur within 81 ms after other reset inputs were removed.

On VPR-80s manufactured prior to October 1985, voltage comparator U7 monitors the +5V supply. If the +5V decays to +4.7V, U7 causes reset to be asserted and the CPU to store tape time and cues in its internal RAM storage.

A manual reset can be asserted at any time by closure of the momentary contact SYSTEM RESET switch S1. When closed, the switch puts a logic low on CPU reset input pin 40. When the switch is released, reset is removed, and the CPU program counter resumes operation from the starting address, beginning the initialization routine.

Nonmaskable interrupt (NMI) input pin 6 is also held high during normal CPU operation. A low-going edge on this input causes an NMI sequence to be generated within the CPU. NMI is caused by closure of the momentary contact TEST switch S2. As with the interrupt request (IRQ) signal, the CPU will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask bit in the condition code register has no effect on NMI. NMI inputs to CPU U10 are used to initiate diagnostic routines.

6-11 E, VMA, and R/W Outputs. The E (enable) output at pin 37, which is a 1-MHz, TTL-compatible clock signal, is placed on the address/control bus. It is derived from the 4-MHz external clock input to the CPU. The 0.5-µs period during which E is high gates the outputs of address decoder U38. E is also used to gate read and write outputs of the CPU and to clock edit timers U27 and U32.

The VMA (valid memory address) output at CPU pin 5 is the validating strobe to address decoder U19 which indicates a valid address on the address bus. U19 examines address bits A13—A15, and provides enabling outputs to the four EPROMs, the RAM, and the control panel assembly. When the CPU accesses other components of the Control PWA (and other systems in the VPR-80), decoder U19 asserts the peripheral select signal, M4. The M4 output of decoder U19 is applied to decoders U24 and U38 as the validating strobe.

The R/W (read/write) output at CPU pin 34 is placed on the address/control bus in both normal (high = read/low = write) and inverted form (low = read/high = write). These outputs tell the peripheral and memory chips whether the CPU is in a read or write state. R/W is also used to control the bidirectional data buffers.

6-12 Data Bus

Pins 26 through 33 of the CPU are the 8-bit (D0—D7) data bus port. The data bus is bidirectional. It transfers data and commands from the CPU to the rest of the control system (and other systems in the VPR-80) on a write cycle. It transfers status and instructions to the CPU on a read cycle. Data bus pins on the CPU are inputs and outputs of bidirectional tristate buffers. Details of data bus structure in the VPR-80 are given in paragraph 6-19.

6-13 Address Bus

Pins 9 through 20 and 22 through 25 of the CPU are the 16-bit (A0—A15) address bus port. Unidirectional address bus outputs are routed to address decoders, EPROM and RAM chips, machine address buffers (U29, U30), and the remote address buffer (U34). Details of the address bus structure in the VPR-80 are given in paragraph 6-25.

6-14 Memory

The control system kernel contains four EPROM chips and one RAM chip. The EPROMs each have the capacity to contain 8K words of 8-bit information, thus providing a total storage capacity of 32K x 8. Low active PRGM (program enable) inputs at pin 27 are pulled up to +5V, and are thereby disabled. Low active CE (chip enable) inputs at pin 20 are tied to ground, and are thus not the controlling input. Contents of EPROMs 1 (U5), 2 (U11), 3 (U16), and 4 (U20) are selectively accessed by the ME, MC, MA, and M8 outputs of address decoder U19, which are applied to the low active OE (output enable) inputs at pin 22.

The 128 bytes of RAM storage within CPU U10 are referred to here and in diagnostics documentation as RAM 1. RAM chip U25 is referred to as RAM 2.

RAM 2 (U25) provides temporary storage for 1024 words of 8-bit information, such as machine status, servo status, and servo commands. RAM 2 (U25) is accessed by the M6 output of address decoder U19 and the R/W (high = read/low = write) output of CPU U10. Contents of RAM 2 are protected by an internal battery in VPR-80s manufactured after October 1985.

6-15 Address Decoding

Addressing contents of the EPROMs, RAM 2 (U25), and the various I/O buffers and latches in the VPR-80 is accomplished at two levels. High-order address bits are decoded to derive a chip select, output enable, or clock (load enable) output to the addressed chip. Low-order address bits define the specific address within that chip.

For example, when accessing a memory chip, high-order address bits enable the chip output, and low-order address bits access the specific address. If the addressed chip is an input buffer, where all bits present at buffer inputs are to be gated as one word, low-order address bits are irrelevent.

6-16 Memory Map

The control system memory map is shown in simplified form in Figure 6-3. The design of the memory map is straightforward. Decoder U19 takes the three highest-order address bits (A13—A15) and divides the entire address range into eight equal parts (M0—ME). Five of these outputs (M6—ME) are used directly with no further decoding to enable the four EPROMs and RAM U25. M4 (peripheral select) is placed on the system bus and enables secondary decoders on Servo, Reference, Audio, Serial Remote, and Time-Code System PWAs. M4 enables bidirectional machine data buffer, U33. M2 enables the internal data buffer and is further decoded into 16 internal enable lines for internal I/O ports and the Parallel Remote PWA. M0 is qualified by A12 (U18) and enables control panel PWAs for addresses 1000—1FFF (hex).

Generally, all addresses are expressed in hexadecimal (hex) notation. (Figure 6-3 shows both hex and decimal notation.) Where less than four hex digits are used (as in Table 6-1 and on the schematics), lower-order digits (on the right) are irrelevent, or in "don't care" states, designated by X.

As seen in Figure 6-3, addresses 0000—007F are dedicated to RAM 1 (the CPU internal RAM, or scratchpad memory). The next higher block of 3967 addresses, 0080—0FFF, is unused. Addresses 1000—1FFF are used for addressing components on Primary and Secondary Control Panel PWAs. Addresses 2000—3FFF access other components on the Control PWA and on the Parallel Remote PWA.

CPU U10 treats Audio, Reference, and Servo PWAs as peripherals, and all hex addresses in the range 4XXX (peripheral select) access components on these PWAs. The accessory Serial Remote PWA and Time-Code System PWA are also accessed within this block of the I/O map.

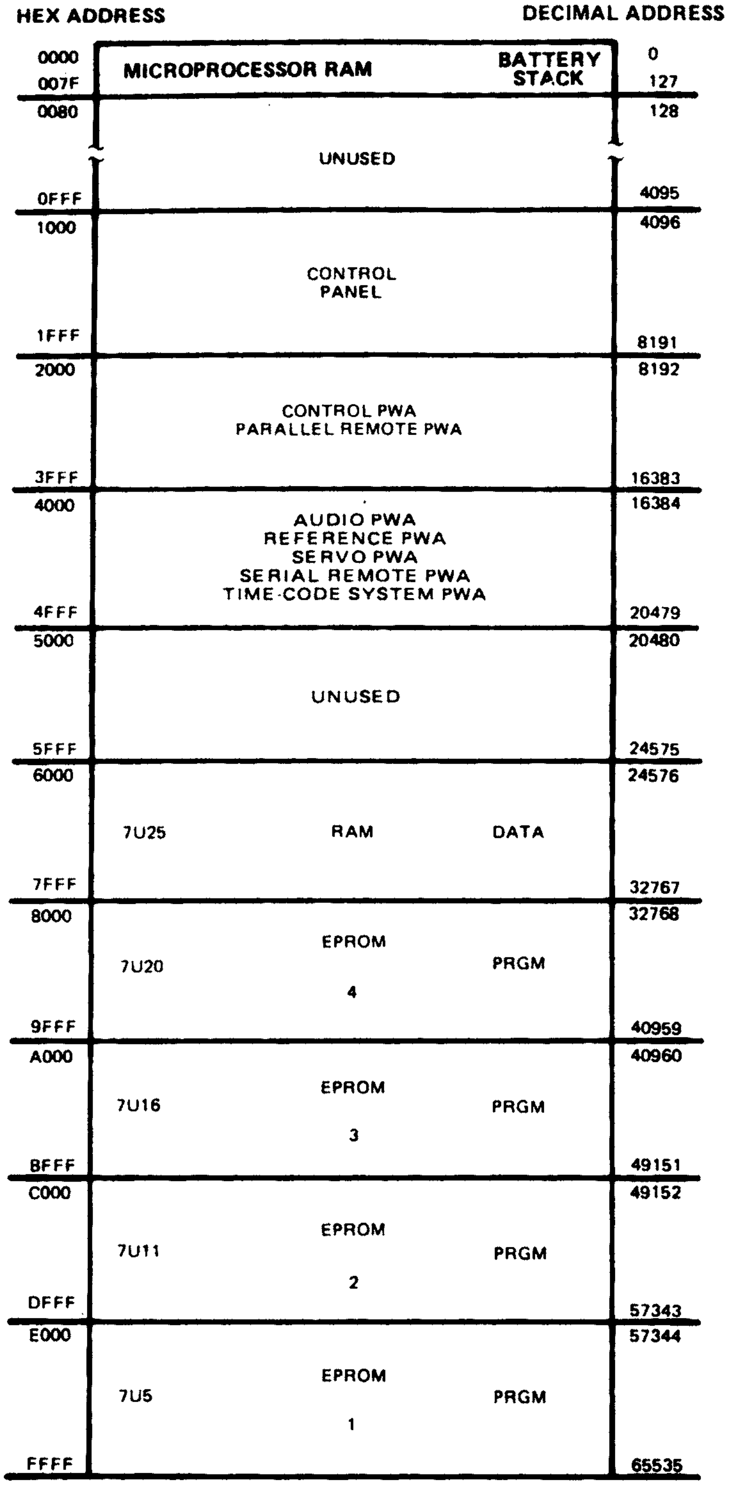


Figure 6-3. Simplified Control System Memory Map

The 4095 addresses between 5000 and 5FFF are unused. The next five blocks of higher addresses are allocated for access to data and instructions in RAM and EPROM chips.

Table 6-1 lists I/O addresses in ascending order. The table also shows address mnemonics used on the schematic diagrams, and lists point of origin for each decoded address. The Remarks column of Table 6-1 lists the outputs of the accessed devices. Reference designations in the Source and Remarks columns are preceded by PWA number, where a number has been assigned (i.e., 6U33 = U33 on PWA 6). Input = input to the CPU. Output = output from the CPU. In addition, the following abbreviations are used in the Remarks column to conserve space:

AD	Address Decoder	MAB	Machine Address Buffer
ADC	Analog-to-Digital Converter	MDB	Machine Data Buffer
APWA	Audio PWA	OD	Output Decoder
CPS	Control Panel Select	ODB	Output Data Buffer
CPU	Central Processor Unit	PCP	Primary Control Panel PWA
DB	Data Buffer	PR	Parallel Remote PWA
DIB	Diagnostic Input Buffer	RAB	Remote Address Buffer
DOL	Diagnostic Out Latch	RDB	Remote Data Buffer
DL	Data Latch	RF	Register File
FIFO	First-in/First-out Register	ROL	Remote Output Latch
ID	Input Decoder	SCP	Secondary Control Panel PWA
IDB	Internal Data Buffer	SR	Serial Remote PWA
IPE	Interrupt Priority Encoder	TCS	Time-Code System PWA
ITB	Interrupt Request Test Buffer	TVC	Tape Velocity Counter
LD	Lamp Driver	WD	Watchdog

Table 6-1. Control System Memory Map

Address	Mnemonic	Source	Remarks
1XXX	CPS	NAND 6U18-3	CTL PNL SELECT. Enables MDB 6U28, PCP DB U1, OD U2, and ID U3. Also applied to MAB 6U29–output as SB CTL PNL SEL.
1XXX	M0	AD 6U19-15	Enables CPS (above).
10XX	E0	PCP OD U2-15	Clocks PCP latch U21/LD U22–STOP, SHUTTLE, CUE, VAR PLAY, PLAY, and RECORD indicators.
11XX	E1	PCP OD U2-14	Clocks PCP latch U5/LD U6–READY, INSERT, ASSEM, VIDEO, and AUDIO 1-3 (record lockout) indicators.

(Continued next page)

Table 6-1. Control System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
12XX	E2	PCP OD U2-13	Clocks PCP latch U8/LD U9–REM 1, EE, MASTER (record lockout), REM 2, ENTR, EXIT, and AUTO indicators.
13XX	E3	PCP OD U2-12	Clocks PCP latch U10/LD U11–8-digit tape time display.
14XX	E4	PCP OD U2-11	Clocks SCP latch U3/LD U1–SET UP, CHROMA/EQUAL, CLR FMR, AUDIO 1-3 MONITOR indicators and HOURS meter drive.
15XX	E5	PCP OD U2-10	Clocks SCP latch U4/LD U2–FAULT, SYSTEM, and SERVO indicators.
16XX	E6	(Not used)	
17XX	E7	(Not used)	
18XX	E8	PCP ID U3-15	Enables PCP DB U20–STOP, SHUTTLE, CUE, VAR PLAY, PLAY, RECORD, TRIM +, and ZERO switches.
19XX	E9	PCP ID U3-14	Enables PCP DB U4–READY (9), INSERT (2), ASSEM (0), VIDEO (7), AUDIO 1 (4), AUDIO 2 (1), AUDIO 3 (ENTER), and AUTO (5) keypad switches.
1AXX	EA	PCP ID U3-13	Enables PCP DB U7–REM 1 (3), EE (6), MASTER (8), REM 2 (backspace) keypad switches, and ENTR, EXIT, and TRIM (-) switches.
1BXX	EB	PCP ID U3-12	Enables SCP DB U5–SET UP, MANUAL (equalizer), INVERT (color framer), and AUDIO 1-3 (monitor) switches.

(Continued next page)

Table 6-1. Control System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
1CXX	EC	PCP ID U3-11	Enables SCP DB U6–FAULT, SYSTEM, TSO RETARD, TSO ADVANCE, and EDIT OPTIMIZE switches.
2XXX	M2	AD 6U19-14	Enables ADs 6U24/6U38 and IDB 6U33.
20XX	20	AD 6U38-15	IRQ ACK. Clocks IRQ ACK latch 6U45.
22XX	22	AD 6U38-14	VID PRT. Clocks video port 6U36. Data bus commands to system: video edit erase, video record relay control, video record to Record Amplifier and Edit Erase PWA, multi-VTR cue and send, A/D end-of-conversion (EOC) latch 6U43 reset, I-phase, remote control track select.
24X*	24	AD 6U38-13	Address latch enable and start conversion command to ADC 6U47. *Three LSB of CPU address bus are decoded to select the following input voltages for conversion: 0 Tape speed control 1 TRACKING control 2 Battery 3 Remote tape speed control 4 Remote TSO 5 Low line/high line 6 +15-Vdc regulated supply 7 +11-Vdc unregulated supply

(Continued next page)

Table 6-1. Control System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
26XX	26	AD 6U38-12	IRQ TST. Enables ITB 6U46–tape-in-path (TIP) sense, tape direction, reference frame, television standards. IPE 6U44 priority word (A0-A2) placed on IDB (ID0-ID2): 0 Vertical 1 Tach frame 2 Tape direction change 3 Control track 4 Video edit 5 Audio edit erase 6 Audio exit edit 7 Audio entrance edit
28XX	28	AD 6U38-11	DIAG OUT. Clocks DOL 6U14. Outputs are pinch roller solenoid and reel brake commands, MDA inhibit, diagnostic probe voltage, green LED indicator 6DS2, and system resets.
2AXX	2A	AD 6U38-10	A/D DATA. Output enable to ADC 6U47.
2CXX	2C	AD 6U38-9	REM DATA. Enables RIB 6U50. Simple remote inputs to CPU U10: STOP, FAST FORWARD, PLAY, REWIND, and RECORD switches. MVC inputs to CPU U10: MVC cue and receive.
2EXX	2E	AD 6U38-7	REM LATCH. Clocks ROL 6U40/LD 6U39–STOP, PLAY, RECORD, FAST FORWARD, and REWIND remote indicators.
30XX	30	AD 6U24-15	TACH LOAD. Clock CK0 to tape timer divider 6U27.
32XX	32	AD 6U24-14	PAR REM SEL. Enables RDB 6U37.

(Continued next page)

Table 6-1. Control System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
320X	90	PR AD U13-15	WRITE input to PR RF U18/U21. Write display data 1-2-4-8 from CPU.
322X		PR AD U13-14	Clocks PR latch U2. Outputs: USER/TC, TAPE TIMER, and TCR/TCG remote indicators.
324X		PR AD U13-13	Clocks PR latch U5. Outputs: remote active, READY, REMOTE LOCKOUT, SERVO LOCK, FAULT (SYSTEM) indicators, edit interval.
326X		PR AD U13-12	Clocks PR latch U9. Outputs: STOP SHUTTLE, CUE, VAR PLAY, PLAY, RECORD, and DROP FRAME indicators.
328X		PR AD U13-11	Enables PR DB U4. Inputs: CLR FMR ON/OFF, CLR FMR normal/INVERT, normal/ACE/-VPR-2, and TSO switches.
32AX		PR AD U13-10	Enables PR DB U1. Inputs: TAPE/EE, FRAME/FIELD, REHEARSE, EXIT, and FREEZE switches.
32CX		PR AD U13-9	Enables PR DB U8. Inputs: READY, INSERT, ASSEMBLE, VIDEO, A1–A3 RECORD ENABLE, and AUTO EDIT switches.
32EX		PR AD U13-7	Enables PR DB U12. Inputs: STOP, SHUTTLE, CUE (search), VAR PLAY, PLAY, and RECORD switches.
34XX	34	AD 6U24-13	VEL LOAD. Clock CK1 to TVC 6U27.

(Continued next page)

Table 6-1. Control System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
36XX	36	AD 6U24-12	BOARD EDGE. Enables DB 6U41. Inputs: PREROLL SEL, DROP FRAME, CLR FRAME, and REF SELECT PWA6 edge-mounted switches.
38XX	38	AD 6U24-11	DIAG IN. Enables DIB 6U23. Inputs: AST drive fault, power supply over-temperature, system reset, IRQ, diagnostic probe, and ADC end-of-conversion.
3AXX	3A	AD 6U24-10	TIMER 1. Enables timer no. 1 6U27 and IDB 6U33. Inputs: tape timer divider, tape velocity counter, and video edit timing.
3CXX	3C	AD 6U24-9	TIMER 2. Enables timer no. 2 6U32 and IDB 6U33. Inputs: audio erase, audio exit edit, and audio entrance edit timing.
3EXX	3E	AD 6U24-7	WATCHDOG. Triggers WD 6U1/6U3.
4XXX	M4	AD 6U19-13	PERIF SELECT. Enables MDB 6U28 (transfer of data between system data bus and Control PWA data bus). Also applied to MAB 6U29–output as SB PERIF SEL.
40XX		APWA AD U56-15	Clocks APWA latch U72. Outputs: audio 50/60 bus, A1–A3 EE bus, video erase, and A1–A3 erase.
41XX		APWA AD U56-14	Clocks APWA latch U65. Outputs: A1–A3 record, 2X play (fast wind), A1–A3 monitor enable.
42XX		APWA AD U56-13	Clocks APWA latch U90. Outputs: internal time code (ITC) and control track EE.

(Continued next page)

Table 6-1. Control System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
46XX		AD 2U34-9	Enables IDB 2U28. Inputs: color/mono input reference, standard Sc/H phase, P/B RF present, reference video present, and input video present.
47XX		AD 2U34-7	Enables ODB 2U23. Outputs: tape/EE, meter inhibit, VIDEO/RF meter select, manual/auto chroma, and shuttle/play.
48XX	E0	AD 5U40-15	Clocks latch 5U20. Outputs SBD0–SBD7 from system data bus to servo CPU data bus.
49XX	E1	AD 5U40-14	Clocks latch 5U27. Outputs SBD0–SBD7 from system data bus to servo CPU data bus.
4AXX	E2	AD 5U40-13	Enables output of latch 5U33. Inputs SBD0–SBD7 from servo CPU data bus to system data bus.
4BXX	E3	AD 5U40-12	Enables output of latch 5U83. Inputs SBD0–SBD7 from servo CPU data bus to system data bus.
4CXX		SR AD U17-11	Enables SR AD U16
4C00		SR AD U16-12	4C00 READ. Enables SR IDB U9. Inputs SBD0–SBD7 from SR data bus to system data bus.
4C02		SR AD U16-10	4C02 WRITE. Shifts SBD0–SBD7 from system data bus into SR FIFO U11, U12, U13, U14.
4C03		SR AD U16-9	4C03 RESET. Resets SR FIFO U11, U12, U13, U14.

(Continued next page)

Table 6-1. Control System Memory Map (Continued)

Address	Mnemonic	Source	Remarks
4D00		TCS AD U57-12	Clocks TCS IDB U40. Inputs SBD0–SBD7 from TCS data bus to system data bus.
4D02		TCS AD U57-10	Shifts FIFO U37. Outputs SBD0–SBD7 from system data bus to TCS FIFO.
4D03		TCS AD U57-9	Resets TCS FIFO U35.

6-17 Address Decoders

Primary address decoders are U19, U24, and U38. An output from one (or more) of these decoders is involved in every CPU instruction or data transfer.

Address bits A13—A15 and VMA are presented to address decoder U19. Outputs of U19 enable access to the EPROM and RAM storage in the control system kernel (M6, M8, MA, MC, and ME). The CPS (M0) output of U19, gated with address bit A12, accesses control panel PWAs and enables bidirectional machine data buffer, U28.

The M4 output of U19 is PERIF SELECT. It also enables machine data buffer U28, enabling transfer of information between system data bus (SBD0—SBD7) and Control PWA data bus (D0—D7). In addition, M4 is also presented, through machine address buffer U29, to secondary address decoders in other VPR-80 systems.

The M2 output of U19 enables internal data buffer U33, thereby enabling transfer of information between the Control PWA data bus (D0—D7) and eight other chips on the Control PWA via the internal data bus (ID0—ID7). Decoded M2 output is also presented to one of the enabling inputs of address decoders U24 and U38.

Decoders U24 and U38 sort out address bits A9—A12 and enable transfer of information between the CPU and other logic on the Control PWA. Since decoder U19 interprets address bits A13—A15, and will have no output unless the address bus is validated by VMA, any output of either U24 or U38 is based on decoding of address bits A9—A15 and the presence of VMA. Parallel remote select (PAR REM SEL) output of U24 enables the secondary address decoder on the Parallel Remote PWA, which decodes lower-order bits of the address word. Outputs of decoder U38 are qualified by E which ensures that data from the CPU is valid before an output enable goes low.

6-18 Data and Address Bus Structure

Figure 6-4 shows an overall picture of the data and address bus structure. It not only shows bus structure within the Control PWA, but also shows data and address paths on the card cage motherboard and paths to the Audio PWA, control panel PWAs, and accessory Parallel Remote, Serial Remote, and Time-Code System PWAs.

6-19 Data Bus Structure

Data bus structure is composed of five major segments plus data bus paths which are internal to the other (peripheral) PWAs. The five major segments of the data bus structure are:

- Microprocessor (CPU) data bus (MD0—MD7)
- Control PWA data bus (D0—D7)
- Internal data bus (ID0—ID7)
- System data bus (SBD0—SBD7)
- Remote data bus (RD0—RD7).

6-20 Microprocessor (CPU) Data Bus. The microprocessor data bus provides an 8-bit bidirectional bit (MD0—MD7) path for data transfers between CPU U10 and the Control PWA data bus (D0—D7). Diagnostic jumper J4 is the interface between the two bus paths; however, when the jumper is in its normal position (B—C), the two bus structures are simply hard-wired together. The microprocessor data bus also carries 8 bits of information to the data out latch, U14. Latched outputs are system reset, MDA inhibit, reel brake control, pinch roller solenoid control, video reset, and voltage to CPU LED DS2 and the diagnostic probe. Updates of the latched outputs are clocked into the diagnostic out latch by DIAG OUT (28) from address decoder U38. Latch outputs are not part of the data bus structure.

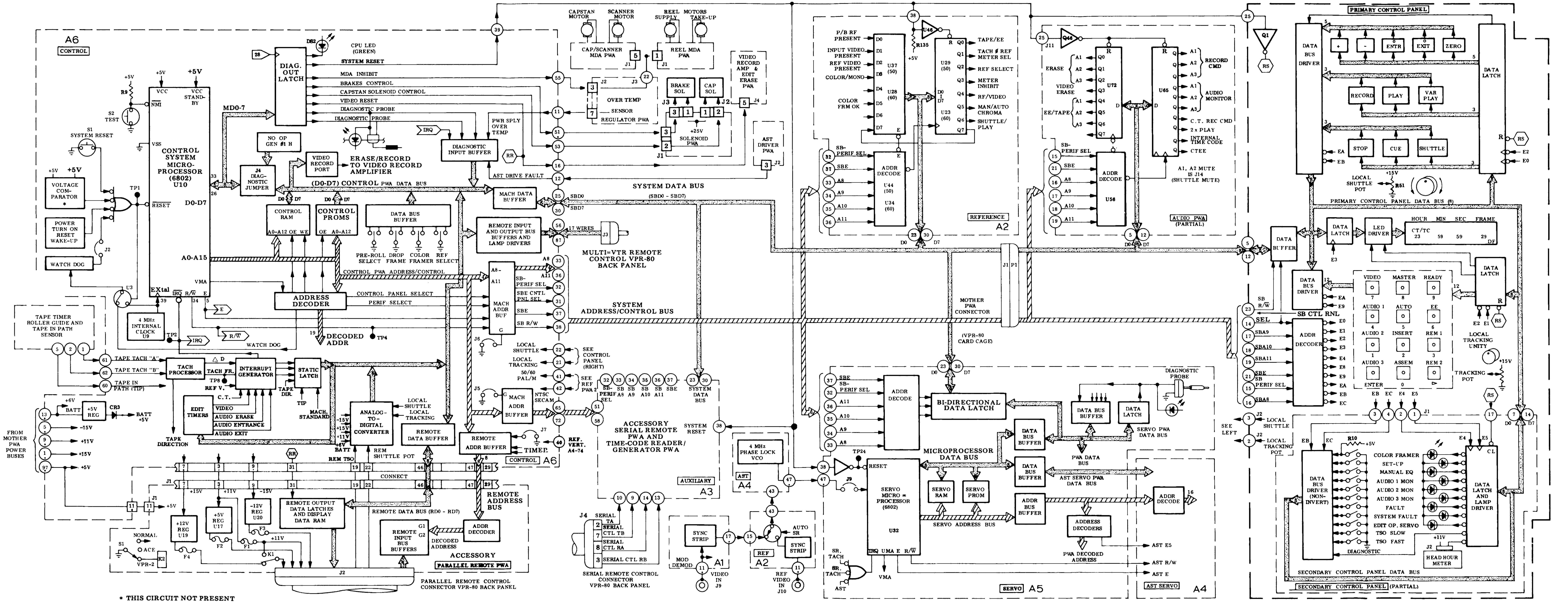
6-21 Control PWA Data Bus. The Control PWA data bus is the path for bidirectional 8-bit (D0—D7) information transfers between the CPU (diagnostic jumper interface) and machine data buffer U28, remote data buffer U37, and internal data buffer U33. Direction of information transfer is controlled by logic level of the R/W output of CPU U10.

The machine data buffer, U28, is the interface between the Control PWA data bus and the system data bus (SBD0—SBD7). The remote data buffer, U37, is the interface between the Control PWA data bus and the remote data bus (RD0—RD7).

The internal data buffer, U33, is the interface between the Control PWA data bus and the internal data bus (ID0—ID7).

6-22 Internal Data Bus. The internal data bus is the path for bidirectional 8-bit (ID0—ID7) information transfers between the Control PWA data bus (at internal data buffer U33) and nine other components on the Control PWA as follows:

U46	IRQ test buffer	U41	Switch data buffer
U45	IRQ acknowledge latch	U50	Remote input buffer
U27	Timer 1	U40	Remote output latch
U32	Timer 2	U36	Video port latch
U47	A/D converter		



* THIS CIRCUIT NOT PRESENT IN SYSTEMS SHIPPED AFTER OCTOBER 1985

Figure 6-4.
Control System Bus Structure

Communication between the CPU and the nine chips listed above is provided when internal data buffer U33 is enabled by M2 from decoder U19. Direction of information transfer is controlled by logic level of the R/W output of CPU U10. The internal data bus is shown in Figures 6-2, 6-7, and 6-8.

6-23 **System Data Bus.** The system data bus is the path for bidirectional 8-bit (SBD0—SBD7) information transfers between the Control PWA data bus (at machine data buffer U28) and addressable data registers within Servo and Reference PWAs (and accessory PWAs) in the card cage, plus the Audio PWA and control panel PWAs. The machine data buffer is enabled by either of two inputs: CPS from NAND gate U18-3, or by M4 from decoder U19. Direction of information transfer is controlled by logic level of the R/W output of CPU U10. The system data bus is shown in Figure 6-4.

6-24 **Remote Data Bus.** The remote data bus is the path for bidirectional 8-bit (RD0—RD7) information transfers between the Control PWA data bus (at remote data buffer U37) and the accessory Parallel Remote PWA. The remote data buffer is enabled by PAR REM SEL (32) from address decoder U24. Direction of information transfer is controlled by logic level of the R/W output of CPU U10.

The Parallel Remote PWA is mounted adjacent to the Control PWA. Both remote data (RD0—RD7) and remote address information are conducted by a PWA-edge-to-PWA-edge connector. The remote data bus is shown in Figure 6-4.

6-25 Address/Control Bus Structure

The address bus structure is composed of three major segments, plus address bus paths which are internal to the other (peripheral) PWAs. The three major segments of the address bus structure are: the microprocessor (CPU) address bus (A0—A15); the system address bus (SBA0—SBA11, SBE, SBR/W, SB CTL PNL SEL, and SB PERIF SEL); and the remote address bus (RA0, RA1, RA5-RA8, RE, and PAR SEL).

6-26 **CPU Address/Control Bus.** The microprocessor address bus is the 16-bit (A0—A15) path for address information from CPU U10 to EPROMs U5, U11, U16, and U20, RAM U25, address decoders U19, U24, and U38, machine address buffers U29 and U30, and remote address buffer U34.

Machine address buffer U29 is the interface between the CPU address/control bus and eight system address/control bus lines: SBA8—SBA11, SBE, SBR/W, SB CTL PNL SEL, and SB PERIF SEL. Machine address buffer U30 is the interface between the CPU address bus and system address bus lines SBA0—SBA7. Remote address buffer U34 is the interface between the CPU address bus and the eight remote address bus lines: RA0, RA1, RA5—RA8, RE, and PAR SEL.

The three least significant bits of the CPU address/control bus are also broken out separately. Address bits A1 and A2 are used to access one of the three discrete counters in each of timer numbers 1 and 2 (U27 and U32 shown in Figure 6-7). Address bits A0, A1, and A2 are applied to a decoder within A/D converter U47 (Figure 6-8). Thus, one of the eight analog inputs to the A/D converter is selected for conversion to 8-bit binary notation.

6-27 **System Address/Control Bus.** The system address bus is the path for 16-bit (SBA0—SBA11, SBE, SBR/W, SB CTL PNL SEL, and SB PERIF SEL) address information from the CPU address bus (at machine address buffers U29 and U30) to secondary address decoders and addressable data registers within each of the other PWAs in the card cage, plus Audio PWA and control panel PWAs. Refer to Figure 6-4.

Machine address buffers U29/U30 gate lower order address bits A0—A11 directly to secondary address decoders for interpretation (SBA0—SBA11). Decoded higher-order address bits, A12—A15, are gated,to secondary decoders as either SB CTL PNL SEL or SB PERIF SEL (M0 or M4 from primary decoder U19). The E and R/W outputs of CPU U10 are gated as SBE and SBR/W. Both machine address buffers are continuously enabled by connection to ground through jumpers J5 and J6.

6-28 **Remote Address/Control Bus.** The remote address bus is the path for 8-bit (RA0, RA1, RA5—RA8, RE, and PAR SEL) address information transfers from the CPU address bus (at remote address buffer U34) and the accessory Parallel Remote PWA. The remote address buffer is continuously enabled by connection to ground through jumper J7. Remote address information is conducted from the Control PWA to the Parallel Remote PWA via a PWA-edge-to-PWA-edge connector. Refer to Figure 6-4.

6-29 Jumpers

The Control PWA is equipped with jumpers as aids to testing the CPU kernel and address decoders and isolating malfunctions in the address bus structure. Although reference designations J1 through J10 are assigned, only six are jumpers in the conventional sense. Jumper J1 has no function and should be left in place. Jumpers J9 and J10 are hard-wire connectors permanently installed in the CPU address bus and should also be disregarded. The J3 designation is assigned to the accessory diagnostic probe connector. Functions of jumpers J2 and J4 through J8 are listed in Table 6-2. Jumper locations are shown in Table 6-6 at the end of this section of the manual.

Table 6-2. Control PWA Jumpers

Jumper	Position	Function
J2	A-B	Watchdog timer enabled (normal).
	B-C	Watchdog timer reset disabled for diagnostics.
J4	A-B	Normal operation.
	B-C	Forces continual NO-OP instruction for test of CPU address/control bus.
J5	A-B	Machine address buffer U30 enabled (address bits SBA0-SBA7 to Servo, Reference, Audio, and control panel PWAs-also Serial Remote PWA and Time-Code System PWA).
	Removed	Above PWAs isolated from CPU address/control bus.

(Continued next page)

Table 6-2. Control PWA Jumpers (Continued)

Jumper	Position	Function
J5 (Con't)	Removed	Above PWAs isolated from CPU address/control bus.
J6	A-B	Machine address buffer U29 enabled (address bits SBA8–SBA11, SBE, SBR/W, SB CTL PNL SEL, and SB PERIF SEL on system address/control bus).
	Removed	System address/control bus isolated from CPU address/ control bus.
J7	A-B	Remote address buffer U34 enabled (address/control bits RA0, RA1, RA5–RA8, RE, and PAR SEL to Parallel Remote PWA).
	Removed	Remote address/control bus isolated from CPU address/ control bus.
J8	A-B	Priority encoder U44 enabled.
	Removed	Priority encoder U44 disabled.

6-30 Control Panel Assembly

The control panel assembly is composed of the primary and secondary control panels. Controls and indicators used for record/playback operation and editing procedures are located on the primary control panel. Controls and indicators used less frequently, such as those used during special operating or adjustment procedures, are located on the secondary control panel directly above the primary controls.

Figure 6-5 is a simplified block diagram of the primary and secondary control panels. As shown in the diagram, PWAs for both panels share a common data buffer and secondary address decoders which are contained on the Primary Control Panel PWA. Also note that +5V and +11V supplies to the Secondary Control Panel PWA are routed through the Primary Control Panel PWA. Figure 6-5 does not show A/D conversion of tape speed or manual tracking control voltages. (Those controls are shown in Figure 6-7.)

In the following paragraphs, component reference designations are prefixed with 6, PCP, or SCP. The prefix 6 indicates the Control PWA, prefix PCP indicates the Primary Control Panel PWA, and prefix SCP indicates the Secondary Control Panel PWA.

6-31 Primary Control Panel

Most circuitry on the primary control panel and its PWA is shown on the left-hand side of Figure 6-5. Refer to Schematic Diagram No. 1450662 for wiring and components involved in the analog record and play level controls and meters.

The only function of the control panel circuits which can be diagrammed in Figure 6-5 is control of the panel indicators. Switching and routing of voltages to implement manually entered commands are done under the direction of CPU 6U10, which recognizes and interprets the manually entered inputs. Switching of voltage to the panel indicators is also done by the CPU.

Contents of display latches PCPU21, 5, and 8 are changed by updated outputs of data buffer PCPU1 when it is enabled on a CPU write cycle.

On each vertical interval, CPU 6U10 initiates E8, E9, and EA to strobe tristate input buffers PCPU20, 4, and 7 on a read cycle. For example, if PLAY switch closure is detected by a change in buffer outputs, the CPU retests the buffer output on the next vertical interval to ensure that the changed input is still there (switch PCPS20 still closed). Following this debounce logic (refer to paragraph 6-4), the CPU clocks display latches PCPU21, 5, and 8 on the vertical interval. Display latch PCPU21 thus turns on the PLAY indicator, and the transition to play mode is begun.

When VPR-80 power is turned on, the power-up reset causes the initialization routine to be performed. Initialization routine firmware commands the VPR-80 to wake up in stop mode/standby condition. Indicators reflecting information stored in the battery-protected portion of RAM 1 are lighted (see paragraph 6-33 for list). If battery protection has been lost, only STOP and EE indicators are lighted. Tape time is displayed if the Control PWA (or the battery) has not been removed since the last power-up reset. All these indications are under CPU control rather than as a result of switch closure (other than the PWR switch).

The SB CTL PNL SEL decoded address bit from machine address buffer 6U29 is applied at connector J2, pin 14. When asserted (low), it enables data buffer PCPU1. Direction of information transfer is controlled by logic level of SBR/W from 6U29. On a write cycle this level is low, and updated outputs of buffer PCPU1 are presented at inputs of all display latches in parallel. The SB CTL PNL SEL ouput of machine address buffer 6U29 also enables secondary address decoders PCPU2 and PCPU3 to decode address bits SBA8—SBA11. When display latches PCPU21, 5, and 8 are clocked by the next assertion of E0, E1, and E2, indicators are controlled by lamp drivers PCPU22, 6, and 9.

Outputs of data buffer PCPU1 are also applied to inputs of display latch PCPU10. When clocked by the next eight assertions of E3 by decoder PCPU2, tape time display is updated.

System reset (SR) is applied at connector J2, pin 25, clearing display latches PCPU22, 6, and 9 in parallel. All indicators except tape time display are turned off.

6-32 Secondary Control Panel

Secondary control panel switches and associated buffers, display latches, LED drivers, and LED indicators are shown on the right-hand side of Figure 6-5. The head HOURS meter and the manual TRACKING control, SCPR3, are also shown.

The data bus, the decoded address (control) bus, and the system reset line, which are internal to the Primary Control Panel PWA, are simply extended to the Secondary Control Panel PWA.

As with the primary control panel, circuitry diagrammed in Figure 6-5 shows how secondary control panel indicators are controlled. Implementation of manually entered commands is entirely in the firmware domain. The FAULT, SYSTEM, and SERVO indicators are turned on under direction of CPU 6U10.

Updating of the secondary control panel data bus comes from Primary Control Panel PWA data buffer (PCPU1). The secondary address decoding of EB, EC, E4, and E5 is also provided by the Primary Control Panel PWA (PCPU2 and PCPU3).

6-33 Initialization Routine

CPU U10 performs the initialization routine as a result of an active (low) reset input at pin 40. As explained in paragraph 6-10, reset can be applied from any one of four sources: power-up reset, watchdog timeout, manual reset, or power-down reset (decay of +5V supply). The sequence of system reset and initialization is charted in Figure 6-6.

When the reset line to CPU U10 goes active (low), so do two other lines: SR, the system reset line, and RR, the remote reset line. SR is asserted throughout the control system. This places all control system logic in a reset condition. SR is also applied to all control interface circuits (address and data latches) in the other VPR-80 systems via the system address/control bus. RR is applied to the accessory Parallel Remote PWA via the PWA-edge-to-PWA-edge connector, J1. Thus, all control interface circuits throughout the VPR-80 are cleared. The active system reset line also resets the CPU on the Servo PWA. With both CPUs in reset condition, audio and video recording is inhibited, motor drive amplifiers (MDAs) are inhibited, reel brakes are applied, and the capstan pinch roller is disengaged.

CPU U10 first tests RAM 2 (U25) and RAM 1 (internal to U10). These tests ensure that the RAMs are responsive to communication and that they are functioning. Testing the RAMs also provides a partial checkout of address decoder U19. If a fault is detected, fault code **102-25*** (RAM 2) or **102-10*** (RAM 1) will be brought up for display.

The CPU then tests for the presence of information in the 32 bytes of RAM storage (RAM 1). If information in RAM 1 is present, the CPU removes the reset condition, retrieves the RAM-stored information, and initializes the audio, video, and servo systems. If RAM-stored information has been lost due to decay of battery voltage or removal of the Control PWA since the last initialization, the CPU will initialize audio, video, and servo systems without that information, and nonstandard condition (SYSTEM) indication **19** will be displayed.

The CPU ensures that reset has been released by looking at pin 8 of U23, the diagnostic input buffer. If reset has not been released, fault code **102-23** is displayed.

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* See Table 9-1, Part II for fault code definitions.

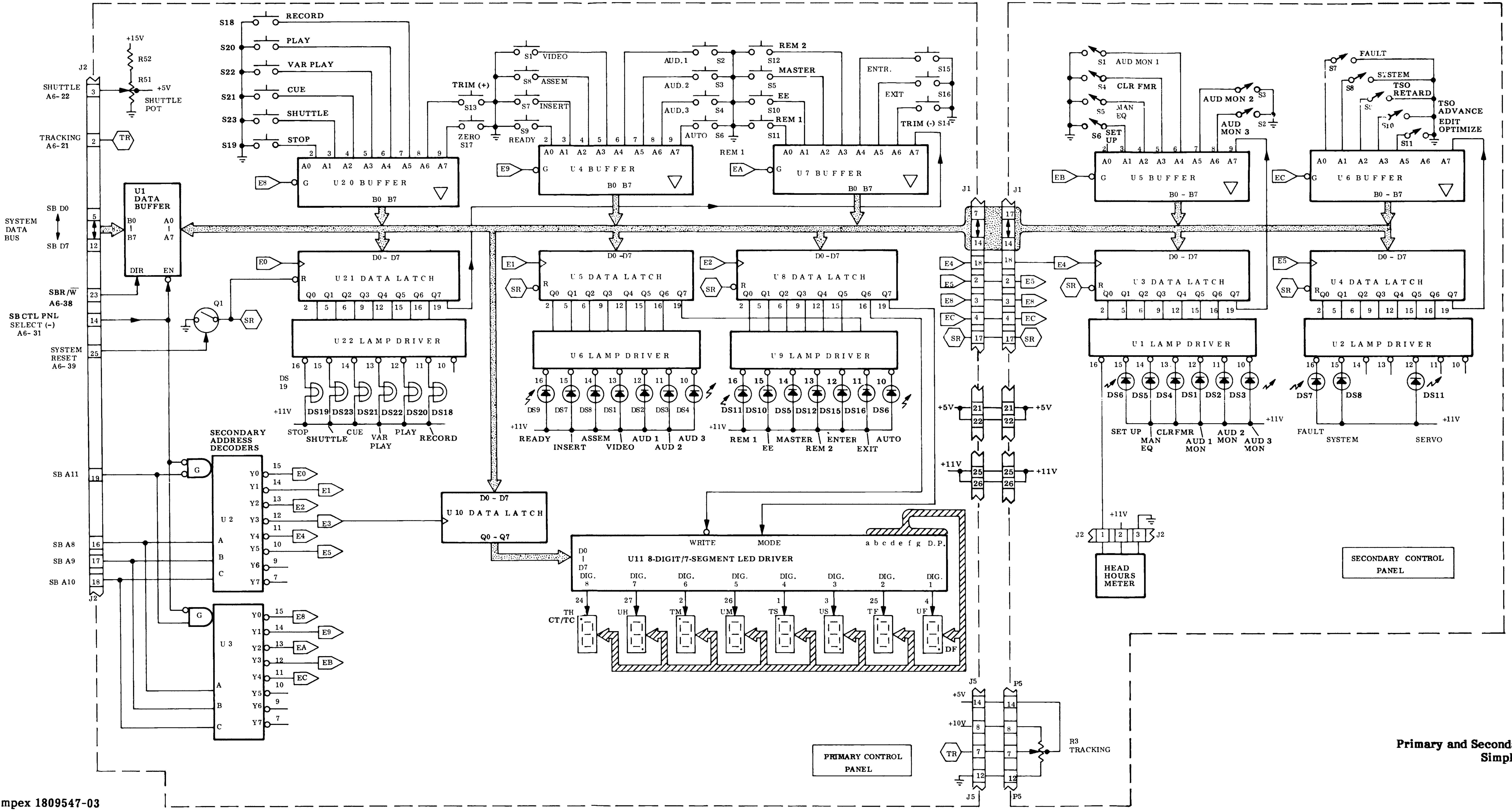

Figure 6-5.
Primary and Secondary Control Panels—
Simplified Block Diagram

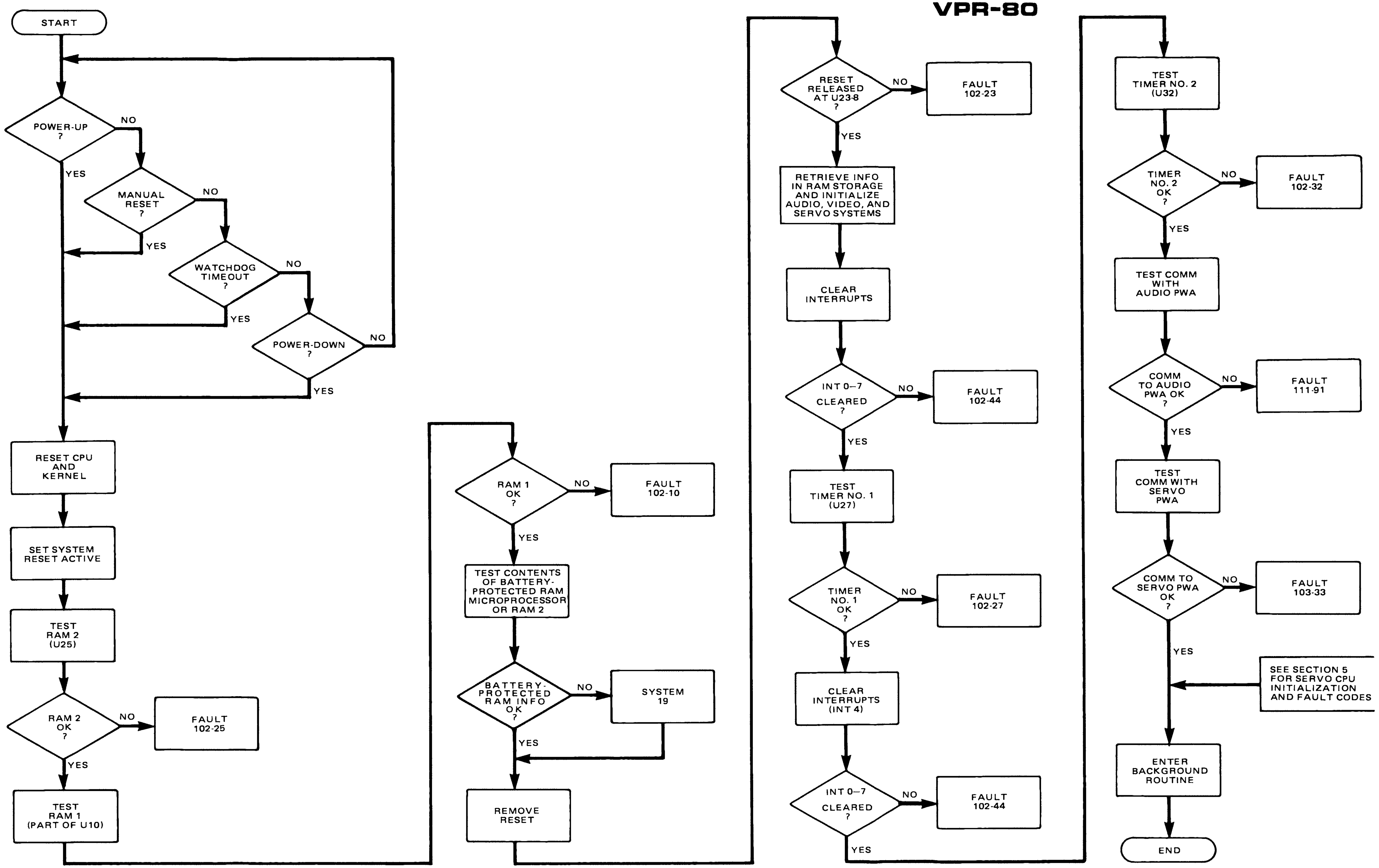

Figure 6-6.
Control System Initialization Routine

Next, the CPU clears all interrupt request lines. When interrupts are cleared, interrupt generator flip-flops U48, 49, 52, and 53 are all in preset condition, and INT 0—7 are all at logic high (inactive) state. The CPU tests these lines and if any are low (active), fault code **102-44** is brought up for display.

The CPU then checks operation of timer no. 1, U27 and timer no. 2, U32. At the same time, it checks out operation of interrupt generator flip-flops, U48, U49, U52, and U53, the IRQ priority encoder, U44, the IRQ test buffer, U46, and diagnostic input buffer, U23. The CPU does this by loading a preset count into the video edit timing counter in U27. E clock pulses then count the preset value down to zero. At the count of zero, the OUT 2 output of timer U27 clocks flip-flop U48-9. The flip-flop output, INT 4, is prioritized by priority encoder U44, and IRQ is asserted at pin 4 of CPU U10. If IRQ is not asserted, fault code **102-27** is brought up for display. The CPU then clears interrupt lines and retests to ensure that they are all inactive.

The CPU proceeds to check out the three timers in chip U32 in the same fashion. Thus, timer no. 2 (U32), IRQ acknowledge latch U45, and the interrupt generator flip-flops associated with INT 5, INT 6, and INT 7 are also checked out. Testing of timer chips U27 and U32 also provides a partial checkout of address decoders U24 and U38. If a fault in U32 is detected, fault code **102-32** is brought up for display.

Until initialization is complete, the condition code register mask in CPU U10 prevents the CPU from branching into interrupt service (foreground) routines. The initialization routine can check only timers in U27 and U32 which are clocked by E from U10. The tape timer divider and tape velocity counter in U27 cannot be checked while in reset condition since they are clocked by tape timer tach pulses, which are unavailable in reset condition.

Communications checks with Audio and Servo PWAs are then made. Fault codes which are brought up for display to indicate faulty communications to these PWAs are **111-91** and **103-33**, respectively.

Finally, the CPU fetches instructions to enable system wakeup in stop mode/standby condition. If information stored in RAM 1 is available, indicators on the control panels are lighted accordingly. RAM 1 information is listed below.

- Tape time
- Edit entrance and exit points
- Status of master record lockout (on/off)
- Status of assemble editor (on/off)
- Status of insert editor (on/off)
- Status of video and audio 1-3 individual record lockouts (when insert edit is selected)
- Status of automatic (or manual) edit
- Status of audio 1-3 monitoring (on/off)

- Status of color framer (on/off)
- Status of automatic (or manual) chroma equalization
- Status of remote 1 setup (setup code 7)

If information in RAM 1 has been lost, only STOP and EE indicators will be lighted. The VPR-80 then enters the background routine.

6-34 Background Routine

The operations list for the background routine consists principally of communications checks, and is purposely short so that completing the long list of operations done at field rate (vertical interrupt—see paragraph 6-36) will not be jeopardized. Background routine operations are listed below with corresponding fault indications, where applicable.

- Communications checks
  - Servo PWA **(FAULT 103-33)**
  - Audio PWA **(FAULT 111-91)**
- General purpose logic probe routine
- A/D converter routine

The control system CPU may have several words of information to transfer to the servo system CPU, and completing handshake protocol is relatively time consuming.

If the diagnostic probe is included as an accessory, it can also be used as a general-purpose logic probe during normal program run. Communication with the probe is done during background routine.

The communication check with the Audio PWA must be done during background routine as well as during initialization. This is necessary because if a communication disconnect occurs, and it is not detected before the next frame rate pulse occurs, the Audio PWA could turn on bias and begin erasing.

6-35 Foreground Routines (Interrupts)

The control system CPU background routine can be interrupted by any of eight prioritized interrupts: INT 0 (highest priority) through INT 7 (lowest priority). The interrupts are listed in Table 6-3. The table also lists sources of the interrupts, interrupt generator flip-flops, and mnemonics of the signals that clock the flip-flops.

Figure 6-7 shows interrupt circuits, tape timer tach, tach processor, tach modulus corrector, and timer nos. 1 and 2.

In general, the sequence of interrupt generation and servicing is as follows. The source of the interrupt clocks one of the interrupt generator flip-flops. The low flip-flop output (INT X) is presented to priority encoder U44. Encoder GS

Table 6-3. Control System Interrupt Generation

Interrupt	Interrupt Generator Flip-Flop	Flip-Flop Clocked by	Source of Interrupt
INT 0 Vertical Interval	U53-9	REFERENCE VERTICAL	AST Servo PWA via XA6-73
INT 1 Tach Frame	U49-5	OUT 0	Timer no. 1 U27-10
INT 2 Tape Direction Change	U49-9	Delta D	Tach modulus corrector via U57-8
INT 3 Control Track	U53-5	CT PLAY REF FRAME	Audio PWA via XA6-45 and U42-12, or AST Servo PWA via XA6-40
INT 4 Video Edit	U48-9	OUT 2	Timer no. 1 U27-17
INT 5 Audio Edit Erase	U48-5	OUT 3	Timer no. 2 U32-10
INT 6 Audio Edit Record Off	U52-9	OUT 4	Timer no. 2 U32-13
INT 7 Audio Edit Record On	U52-5	OUT 5	Timer no. 2 U32-17

output then asserts IRQ to CPU U10. The A0—A2 outputs of U44 identify the interrupt, and the three-bit ID word is presented to the IRQ test buffer, U46. The CPU responds with address 26XX (IRQ TEST) from address decoder U38-12. IRQ TEST enables the IRQ test buffer. The CPU then reads the interrupt ID word (ID0—ID2 on the internal data bus) and services the interrupt. When service has been completed, the CPU asserts address 20XX (IRQ ACK) from address decoder U38-15. IRQ ACK clocks IRQ acknowledge latch U45. The low output of U45, ACKX, presets the interrupt generator flip-flop, and the flip-flop Q output, INT X, returns to the inactive (high) state. This clears the interrupt, and the CPU returns to the background routine.

At high tape speeds in shuttle (or variable play) mode, interrupts tend to be stacked. For example, vertical interval (INT 0) and tach frame (INT 1) interrupts are very likely to occur together. In this event, priority encoder U44 identifies the higher priority interrupt first (INT 0). The INT 1 logic level will remain active at the input of U44 until the higher priority interrupt has been serviced and the INT 0 output of U53-9 has been cleared. Since IRQ remains asserted at CPU U10, the CPU will again look at IRQ test buffer U46, see the ID word for INT 1, and proceed to service (and then clear) that interrupt. If IRQ is still asserted (U44-14 low), the CPU will then enable U46 again to see what interrupt has become active in the meantime. The CPU cannot return to the background routine until all interrupts have been cleared at the output of IRQ test buffer U46.

6-36 Vertical Interval (INT 0)

The highest-priority interrupt, INT 0, occurs on every reference vertical pulse from the AST Servo PWA. The control system CPU performs most of its repetitive housekeeping tasks as a result of this interrupt. Tasks performed during vertical interval can be grouped into four major categories: control functions, edit management, status checks, and communications checks. Vertical interval tasks are summarized below. Indications of faults and nonstandard conditions which are generated as a result of status and communications checks are also listed.

Control Functions

- Poll control panel switches
- Process mode switch changes
  - Audio commands
  - Video commands
  - Servo commands
- Process A/D values
  - Shuttle
  - Variable play
  - Tracking
- Measure tape velocity
- Local/remote setup
- Parking brake control
- Pinch roller control
- Update tape time display
- Update local indicators
- Update remote indicators

Status Checks

- Head hours meter
- Servo faults
- Display servo system messages:
  - Servos not locked (system **06**)
  - Control track not locked (system **07**)
  - Not field matched (system **08**)
  - Not color framed (system **09**)
  - Scanner stalled (system **11**)

Auto Edit Management

- Preview modes
  - Edit preview
  - Exit preview
  - Edit review
- Auto edit
  - Open-ended edit
- Frame accurate timing

Communications Checks

- Primary Control Panel PWA (fault **110-21**)
- Secondary Control Panel PWA (fault **109-03**)
- Reference PWA (fault **104-23** for NTSC, or **104-29** for PAL)
- Parallel Remote PWA (fault **105-02**)
- Serial Remote PWA (fault **106-08**)

Status Checks

- Control PWA edge-mounted switches
  Reference select
  Preroll select
  Drop frame/full frame select
- Servo parameters
  Color frame on/off
  Color frame norm/invert
  Tape/EE

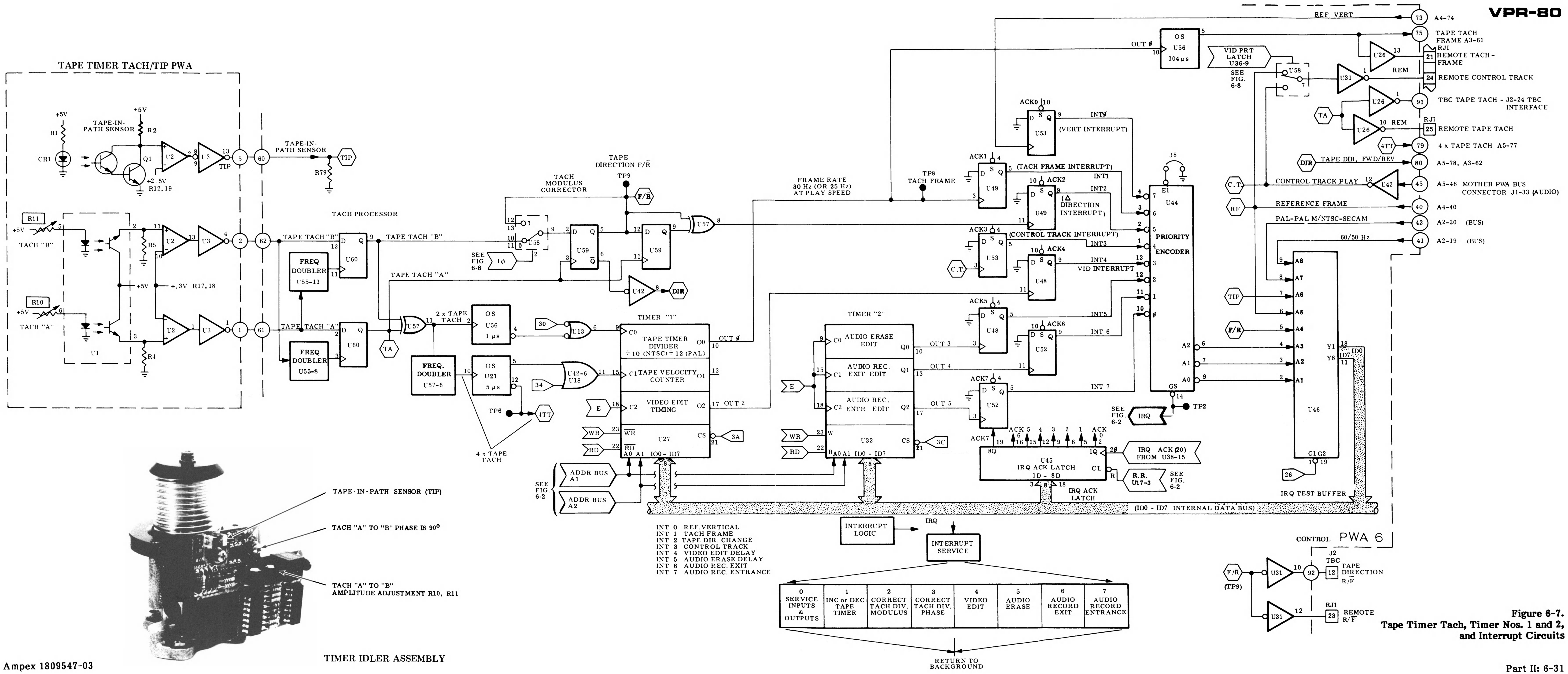

Figure 6-7.
Tape Timer Tach, Timer Nos. 1 and 2, and Interrupt Circuits

  - Ref. fr. abs. (fault **100-22**)
  - AST Driver PWA high voltage (fault **101-102**)
- Process A/D values
  - +11 Vdc unreg. (system **17/18**)
  - Tape speed override
  - Manual tracking (system **16**)
- Power supply limits (system **20** and faults **108-01** through **108-07**)
- Tape in path (system **21**)

6-37 Tach Frame (INT 1)

Each time tach frame interrupt (INT 1) occurs during tape motion, tape time is incremented (or decremented) by one frame.

The CPU loads the applicable divisor into the tape timer divider (U27, timer 0). The divisor is either 10 (for NTSC) or 12 (for PAL) systems. At normal play speed the tape timer tach produces 150 tach pulses per second (pps). The tach processor converts this rate to 300 pps at the output of exclusive OR gate U13-6. The 1-µs, 300-pps output of U13-6, CK0, is applied to U27-9 where it counts down the divisor. Thus 300 pps divided by 10 equals 30 pps for NTSC, or 300 pps divided by 12 equals 25 pps for PAL systems.

Each time the divisor (10 or 12) in U27 is counted down to zero, U27 produces OUT 0 which clocks U49-5. The output of U49-5 is INT 1, which is asserted at frame rate. CPU U10 services this interrupt by incrementing or decrementing tape time (and display) by one frame.

During initialization routine, the divisor is placed into U27, timer 0. Thereafter, during tape motion, the divisor is automatically reloaded into the tape timer divider (U27, timer 0) on each tach frame pulse. Transferring the divisor from the internal hold register in U27 to the count register requires an external clock. This is accomplished by address 30XX (TACH LOAD) from address decoder U24-15 which is applied to OR gate U13-6. The OR gate output supplies the external clock.

6-38 Tape Direction Change (INT 2)

When tape travel changes direction, the INT 2 interrupt causes the CPU to reverse direction of tape time count.

Reversing tape direction produces an output at exclusive OR gate U57-8 which clocks flip-flop U49-9. The output of U49-9, INT 2, is prioritized (identified) by U44, and the interrupt ID word is presented to IRQ test buffer U46. At the same time, logic level at test point TP9 (F/R) changes state. The F/R logic level is also presented to IRQ test buffer U46. The CPU services this interrupt in two ways. First, it reverses the direction of tape time count (increment to decrement, or vice versa). Secondly, it adjusts the count in U27, timer 0. The I phase output at U36-12 prevents an erroneous direction reversal at tape speeds greater than play speed.

The tach modulus adjustment at U58-2 ensures that tach frame interrupt, INT 1, will remain in sync with the control track by effectively changing the divisor in the tape timer divider (U27, OUT 0) for one frame. The adjusted modulus is transferred into the count register by a clock pulse to U13-5.

Chances are nil that tape direction change will occur precisely coincident with a tach frame pulse. Therefore, the divisor in the tape timer divider will be in some state of incomplete countdown when tape direction is changed.

In response to INT 2, the CPU changes the divisor so that it will be counted down to zero by processed tach pulses (causing frame count change) at the same point as if tape direction change had not occurred. This correction is in effect for the one incomplete frame only. Thereafter, the normal divisor (10 or 12) is loaded into the tape timer divider on each tach frame pulse.

6-39 Control Track (INT 3)

During tape motion, changes in tape tension effectively change the diameter of the tape timer idler. Also, due to some inevitable tape slippage, tape may not always be metered correctly by the idler. The control track interrupt (INT 3) checks and, if necessary, corrects accuracy of tape time once per frame. The off-tape control track during play and shuttle modes, or the reference frame pulses during record mode are used as timing standard.

In play and shuttle modes, off-tape CT PLAY pulses are received once per frame by the Control PWA via XA6-45. These pulses, which occur in the middle of the frame, are buffered by U42-12 and they clock flip-flop U53-5, causing INT 3 to be asserted. Thus, if tape time is absolutely correct, INT 3 will be asserted halfway between assertions of the tach frame interrupt, INT 1. Ideally, the divisor (10 or 12) in the tape timer divider will have been counted halfway down to zero when INT 3 is asserted.

The CPU services INT 3 by looking at the remaining count in the tape timer divider. If the remaining count is 5 (NTSC) or 6 (PAL), no correction is necessary. If the remaining count is some other number, the CPU corrects the count to 5 (or 6). Thus, any drift in tach frame (INT 1) in relation to control track is corrected within the frame.

In record mode, reference frame pulses from the AST Servo PWA serve as timing standard. Assertion of INT 3 cannot be seen in hardware (as shown in Figure 6-7 or Schematic Diagram No. 1465507). The reference frame signal is routed from XA6-40 to the A5 input of IRQ test buffer U46. Beyond that point, assertion of INT 3 is in the firmware domain, but principles of operation are the same as for assertion of INT 3 in play and shuttle modes.

6-40 Video Edit (INT 4)

Video edit interrupt (INT 4) provides precise timing for control of video erase current and switching of video at auto edit entrance and exit points. This interrupt is also generated when nonedit record mode is entered.

Manually entered edit entrance and exit points, which are held in RAM storage, provide only coarse timing for implementation of the video switching involved in editing. The CPU switches the video input path from tape to EE on the vertical interval interrupt (INT 0) prior to the entrance point. The CPU then successively loads three values into the video edit timer (U27, timer 2). Each value, equivalent to a precise (fine) timing interval, is counted down to zero by the 1-MHz E clock from the CPU before the next value is loaded. When each interval is counted down to zero, INT 4 is asserted with 1-µs accuracy. The sequence is as follows:

The first interval loaded into the video edit timer is X* milliseconds (ms). When X-ms expires, INT 4 is asserted, and the CPU services the interrupt by switching video erase on at the edit erase head on the scanner. The CPU then loads and counts down an interval of Y* ms. The second assertion of INT 4 causes the CPU to switch the video record/play relay to RECORD. The third interval to be loaded and counted down is Z* ms. When INT 4 is asserted for the third time, the video record command is sent to the Record Amplifier and Edit Erase PWA. All three of the above switching operations take place within one vertical interval (one field). Edit erasing begins with field 2 of the selected entrance point frame.

At the exit point, reverse switching of video erase and then the record/play relay and record command is timed by the video edit timer in the same fashion. The CPU then switches video from EE back to tape. Tape/EE switching is done in response to instructions in firmware. No hardware timing is involved in tape/EE switching.

When entering nonedit record mode, INT 4 is also generated three times. INT 4 times the switching of video erase, record/play relay, and the record command in the same fashion as in edit recording.

When making assemble edit and nonedit recordings, the longitudinal video erase head stack is also switched on. After enough time has elapsed in record mode to allow the start of the recording to travel off the scanner, the edit erase (flying erase) head is switched off and the longitudinal (bulk) video erase head stack is turned on. When making insert edits, this switching operation is not done, and all video erasing is accomplished by the flying erase head.

CPU commands for video switching are routed via internal data bus to video port latch U36. When U36 is clocked by address 22XX (VID PRT) from decoder U38-14, video erase, video record relay, and video record commands are routed to the Record Amplifier and Edit Erase PWA.

6-41 Audio Edit (INT 5—7)

The three audio edit interrupts (INT 5—7) provide precise timing for control of audio erase current and switching of audio record command at auto edit entrance and exit points. Whereas, one interval timer (U27, timer 2) is sufficient to handle fine timing requirements of video edit switching, timing involved in switching three audio channels requires three interval timers (U32, timers 0—2) and three separate interrupts (INT 5—7).

Audio edit erase interrupt (INT 5) is generated when the interval value in U32, timer 0, is counted down to zero. The audio edit record off interrupt is INT 6, generated by U32, timer 1. The audio edit record on interrupt is INT 7, generated by U32, timer 2. Interrupts INT 5 and INT 7 are also generated when nonedit record mode is entered. Interrupts INT 5 and INT 6 are also generated when nonedit record mode is exited.

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* Precise value differs between NTSC and PAL video standards.

The following sequence applies to any of the three audio channels. In auto edit mode audio erase current is turned on three frames in advance of the entrance point. This is necessary because of the physical distance between the audio erase head stack and the audio record/play head stack. The switching on of audio erase is timed by interrupt INT 5 from U32, timer 0. At the edit entrance point, interrupt INT 7 times the assertion of the audio record command to the Audio PWA at field 2 of the selected frame. At the exit point, audio erase is turned off and then the record command is removed. Audio erase is turned off in response to another assertion of INT 5, and the record command is switched off in response to interrupt INT 6.

Construction of the edit may require that another channel be turned off during that delay interval. Thus, separate entrance and exit point timers (and interrupts) are required. Ramp-up and ramp-down times of audio erase head output are equal, and therefore bear the same relationship to a frame edge. Thus, one audio erase interrupt timer (INT 5) can be used for all audio erase on and erase off timing requirements.

6-42 Tape Velocity Counter

The tape velocity counter is U27, timer 1, shown in Figure 6-7. The CPU periodically samples the value in the counter. The value in the tape velocity counter tells the CPU how much tape has travelled around the timer idler since the last sample was taken. When sampled at regular intervals, tape speed is readily computed.

The CPU clears the counter by applying address 34XX (VEL LOAD) from address decoder U24-13 to OR gate U18-11. The OR gate output clocks 0000 (on the internal data bus) into U27, timer 1. During tape motion, the value in the counter is counted down through the OR gate by 5-µs 4X tach pulses from one-shot U21-5.

The first clock pulse, CK1, changes the value to FFFF, and each succeeding CK1 pulse reduces the value by one count. The count in the tape velocity counter is sampled and recleared at frame rate. Therefore, no matter how fast tape is moving, the counter will never have been clocked by enough CK1 pulses to reach 0000 before the value in the counter is sampled again. After the first CK1 pulse, the value in U27, timer 1 is inversely proportional to tape speed. If, however, sampled value is 0000, no tape motion has taken place since the last sample.

The CPU uses tape velocity information in mode control qualification. (Refer to paragraph 6-7.) For example, with tape in motion, a stop mode command cannot be completely implemented by engaging the capstan pinch roller until reel brakes have brought the tape to a complete stop. Therefore, the pinch roller will not be engaged until the CPU sees 0000 in the tape velocity counter.

6-43 A/D Conversion

The control system analog-to-digital (A/D) converter, U47, is shown in Figure 6-8. It responds to two commands (decoded addresses) from the CPU. On the first command (A/D LOAD), the A/D converter loads one of the eight analog input values and converts it to 8-bit binary notation. On the second command (A/D DATA), the A/D converter puts the 8-bit word on the internal data bus for examination by the CPU. Analog values presented to the A/D converter are local and remote tape speed control values (shuttle and variable play) and local tracking control values. The A/D converter also converts remote TSO value and ±15 Vdc and +11 Vdc values from the power supply and backup battery voltage. All eight analog inputs are sequentially sampled and converted between assertions of vertical interval interrupt (INT 0) during background routine. The A/D conversion sequence is as follows:

CPU address/control bus bits A0, A1, and A2 form a word which selects the first of eight analog inputs to U47. These bits are applied to pins 23-25 of U47. The analog input select word is then validated by address 24XX (A/D LOAD) from decoder U38-13. Selected analog input is thus loaded into U47 for conversion. E clock pulses from the CPU are divided 2 to 1 by U43-5. The 500-kHz output of U43-5 provides clock pulses for the conversion process within U47. The conversion process requires approximately 150 µs. During this time, the CPU attends to other background routine tasks.

After approximately 150 µs, the CPU asserts address 2AXX (A/D DATA) which causes U47 to place the first digitized sample on the internal data bus. The CPU then changes address bits A0—A2 to access the second sample and asserts A/D LOAD. This sequence is repeated until all eight analog inputs to U47 have been digitized and placed on the internal data bus. The CPU then continues with background routine tasks. The A/D conversion sequence is not repeated until after the next vertical interval interrupt (INT 0).

A/D converter U47 digitizes analog voltages in the range of 0 Vdc to +5 Vdc. Therefore, precision dividers are used to proportion power supply, battery, and tracking control inputs to that range. Adjustment control R109 is provided on the remote tape speed control input. Since cable lengths to the remote control may vary, the zero (STOP) position on the remote tape speed control may not be accurate. Therefore, R109 provides an adjustment at the input of U47 for calibration of the remote control.

End-of-conversion (EOC) output of U47 is not used to prompt loading of the next analog input. The CPU simply attends to other background tasks during the conversion process, allowing ample time for conversion before loading the next analog input.

Completion of the A/D conversion sequence involves an interesting VPR-80 safety feature. Watchdog U1/U3 cannot be accessed by decoder U24 unless an A/D conversion sequence has been completed between vertical interrupts. Therefore, if tape ever travels at extremely high speed (in excess of 300 in/s) causing interrupts to accumulate so fast that the A/D conversion sequence cannot be completed, the

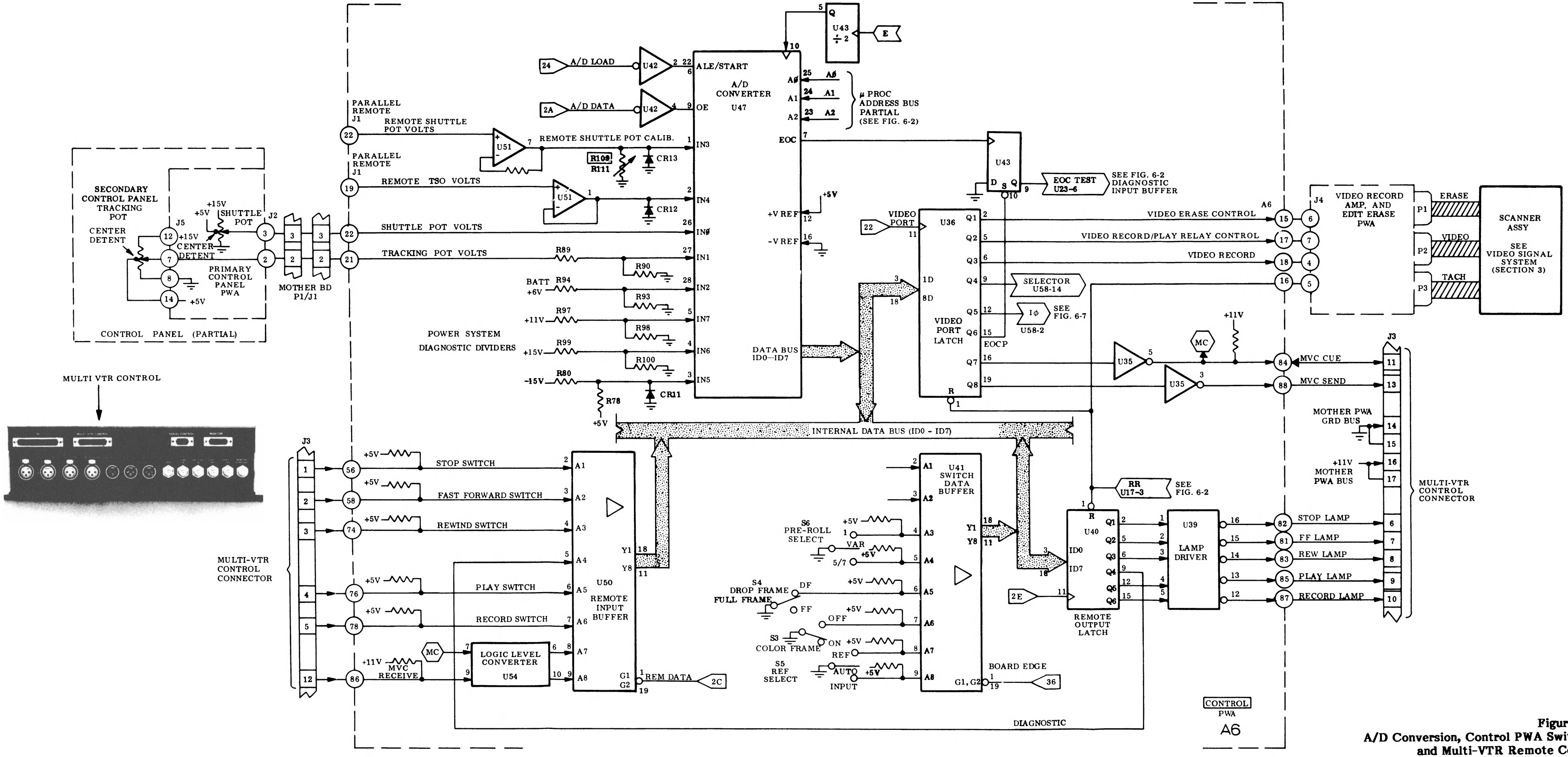


**Figure 6-8.
A/D Conversion, Control PWA Switches,
and Multi-VTR Remote Control**

watchdog will not be accessed. (Refer to paragraph 6-10.) If uncontrollable high tape speed persists for 81 µs, the watchdog will time out, and this will cause system reset to be asserted. Thus, MDA inhibit and reel brakes will be applied.

6-44 Control PWA Switches

Figure 6-8 also shows switch data buffer U41. A3—A8 inputs are tied to contacts of Control PWA edge-mounted switches S3 through S6. The U41 inputs are enabled by the assertion of address 36XX (BOARD EDGE) from decoder U24-12. The digital word repesenting the PWA edge switch positions is placed on the internal data bus to the internal data buffer (and the CPU). This occurs at field rate as a result of vertical interval interrupt (INT 0). Any change in switch position which is detected at vertical interrupt is acted upon by the CPU (refer to paragraph 6-4). The A1 and A2 inputs to U41 are unused and are pulled up through 2.2K resistors.

6-45 Simple and Multi-VTR Remote Control

Figure 6-8 shows remote input buffer U50 and remote output latch U40 which are input/output ports for simple remote control operation. A simple remote control device is interfaced to the VPR-80 through the MULTI VTR CONTROL connector on the I/O connector panel. Refer to Table 2-6 in the *VPR-80 Installation and Operation* manual for a list of specific connector pin assignments.

Stop, fast forward, rewind, play, and record switch inputs from a simple remote control source are presented to the A1—A6 inputs of remote input buffer U50. Active mode is indicated by a logic low level. When U50 is enabled by address 2CXX (REM DATA) from decoder U38-9, five bits of simple remote switch data are placed on the internal data bus to the CPU. The CPU implements any mode change request made since U50 was last enabled, and changes the simple remote lamp driver output accordingly. The CPU places the correspondingly changed lamp driver word on the internal data bus, and when remote output latch U40 is enabled by address 2EXX (REM LATCH), simple remote lamp driver outputs are altered to reflect the change of mode.

Figure 6-8 shows remote input buffer U50 and video port latch U36, which are the input/output ports for multi-VTR remote control operation. If the multi-VTR cable is connected between two VPR-80s as shown in Figure 2-17 of the *VPR-80 Installation and Operation* manual, multi-VTR auto edit capability is completed when the REM 2 indicator on the source VTR is lighted. When the REM 2 indicator is lighted, the source VTR will respond to play and cue mode commands initiated at the control panel of the record (editor) VTR.

When the VPR-80 is the record VTR, the MVC CUE (cue mode command) and MVC SEND (play mode command) signals appear at the buffered and inverted Q7 and Q8 outputs of video port latch U36 (MULTI VTR connector pins 11 and 13). These outputs are applied to the source VTR when U36 is enabled by address 22XX (VID PRT) from decoder U38-14.

When the VPR-80 is the source VTR, MVC CUE (cue mode command) is received at pin 11 of the MULTI VTR CONTROL connector and is applied to logic level converter U54. The cue mode command output of U54 is applied to the A7 input of remote input buffer U50. Also, the MVC SEND output of the record VTR becomes the MVC RECEIVE signal (play mode command) at the source VTR. It is received at pin 11 of the MULTI VTR CONTROL connector and applied to U54. The MVC RECEIVE (play command) output of U54 is routed to the A8 input of remote input buffer U50. U50 is enabled when address 2CXX (REM DATA) is asserted by decoder U38-9. The source VTR then implements the commanded mode, cue or play.

6-46 Timer Idler Assembly

The timer idler assembly is shown in Figure 6-7. It is composed of the timer idler, tape tachometer (tach), and the Tape Timer Tach/TIP PWA.

Moving tape turns the idler; the rotating idler turns the optical tach disk. The tach disk is etched with two sets of concentric, radial, light barrier stripes. One set of radial stripes is for generation of tape timer tach A pulses, and the other set is for generation of tach B pulses, producing tach A and B pulses alternately at even intervals.

A simplified schematic of the Tape Timer Tach/TIP PWA is also shown in Figure 6-7. Tach A and B pulses are generated by light interruption detectors within module U1. The U1 outputs (tachs A and B) are buffered by U2 and inverted by U3 before being applied to the tach processor on the Control PWA. Light interruption by the tach disk causes outputs of U3-1 and U3-4 to be low.

The TIP (tape-in-path) sensor circuit is composed of LED CR1 and Darlington transistor Q1, which are on opposite sides of a cutout in the Tape Timer Tach/TIP PWA. When tape is threaded on the transport, the tape path passes through the cutout, causing light interruption, and the output of U3-13 is high. If tape is not threaded through the sensor circuit cutout, Q1 is turned on, and the low output of U3-13 causes nonstandard condition (system) indication 21 to be displayed.

The tach processor on the Control PWA, acting on the inputs of tach A and B pulses, produces two clock outputs: 2X tape tach and 4X tape tach. These clock rates are, of course, directly proportional to tape speed. The 2X tape tach output of U57-11, shaped by one-shot U56-4, is the clock input to the tape timer divider, U27-timer 0. (Refer to paragraph 6-37.) The 4X tape tach output of U57-6, shaped by one-shot U21-5, is the clock input to the tape velocity counter, U27-timer 1.

(Refer to paragraph 6-42.) The 4X tape tach output at U21-12 is routed to the Servo PWA where it clocks the tape tach divider and supply and takeup reel tape pack diameter counters.

Adjustment and alignment of the Tape Timer Tach/TIP PWA outputs are covered in paragraph 6-61.

6-47 REMOVAL/INSTALLATION

The following paragraphs describe removal and reinstallation of the control panel assembly and the timer idler assembly.

6-48 Control Panel Assembly

To remove the control panel assembly from the control panel chassis, proceed as follows:

STEP 1 With power off, open hinged transport cover and release the two catches so that cover hangs below control panel as shown in Figure 6-9.

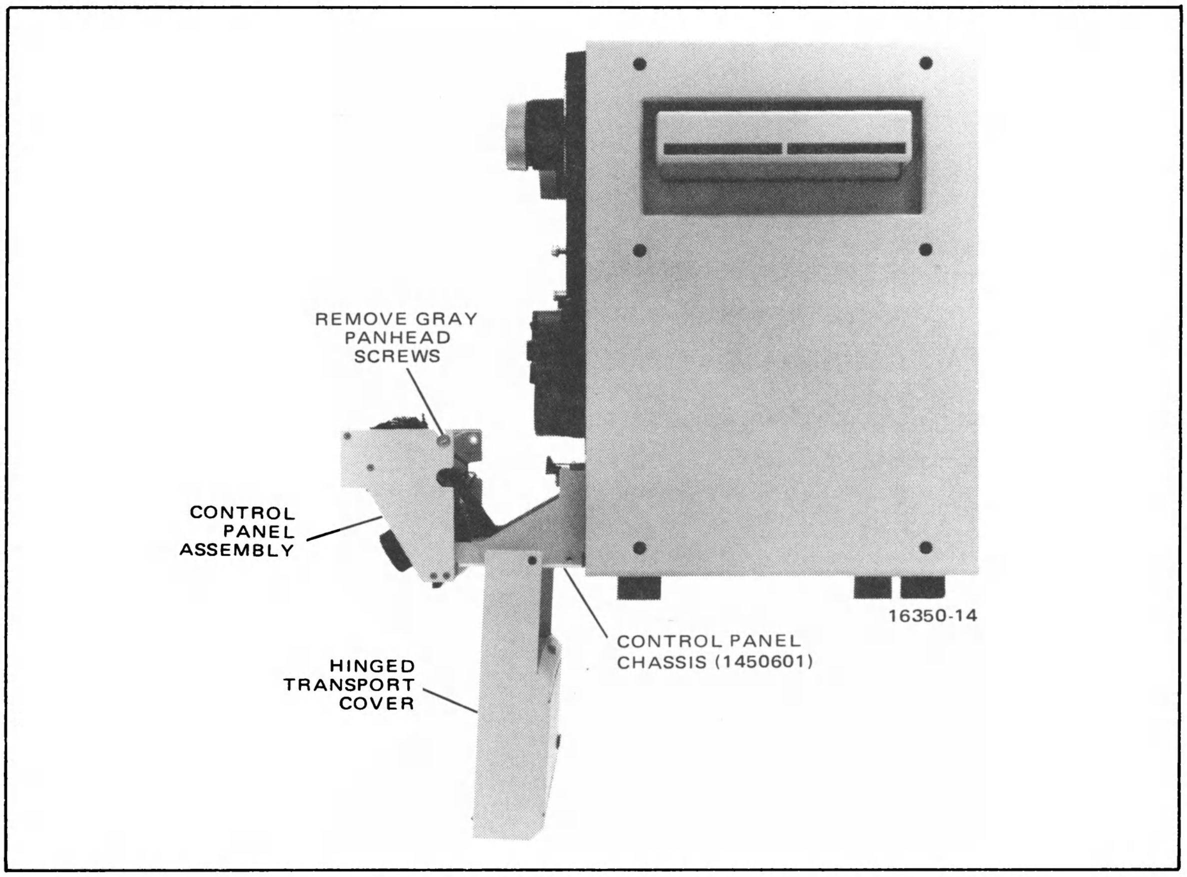


Figure 6-9. Removing Control Panel Assembly

STEP 2 Remove gray panhead screw from each end of control panel and pivot control panel forward.

STEP 3 Disconnect four connectors J2—J5 from Primary Control Panel PWA (Figure 6-10).

STEP 4 See Figure 6-11. Remove left end cap by removing four 6-32 flathead screws. This will permit the control panel assembly to shift to the right, separating the panel from the control panel chassis. Remove and save the two wavy washers from control panel chassis pivot points.

STEP 5 Reinstall control panel assembly on control panel chassis in reverse order of removal.

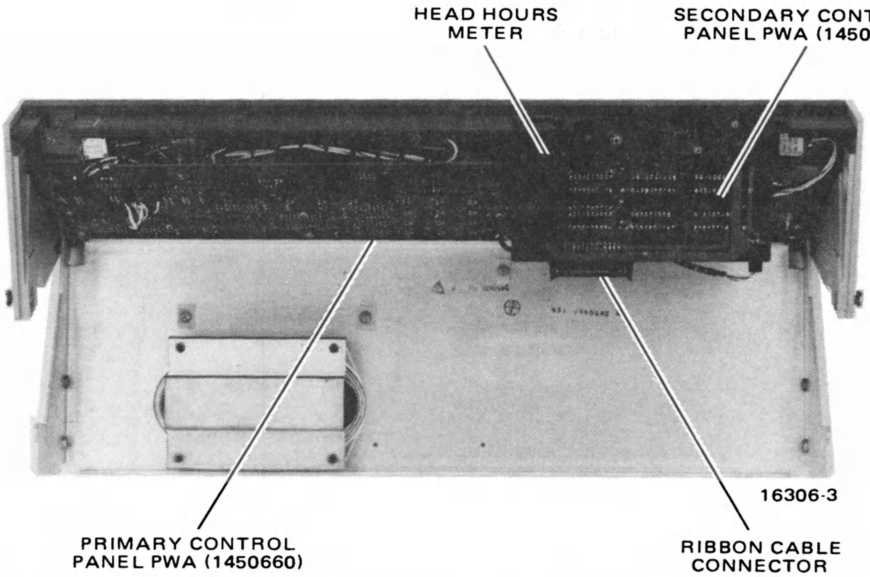

HEAD HOURS METER
SECONDARY CONTROL PANEL PWA (1450640)
16306-3
PRIMARY CONTROL PANEL PWA (1450660)
RIBBON CABLE CONNECTOR

Figure 6-10. Control Panel Assembly Rear View

6-49 Primary Control Panel PWA

To remove the Primary Control Panel PWA from control panel assembly, proceed as follows:

STEP 1 Remove control panel assembly from control panel chassis (1450601) as outlined in paragraph 6-48.

STEP 2 Remove tape speed control knob using a 5/64-inch hex-drive wrench to loosen two setscrews 90° apart.

STEP 3 Remove the six AUDIO RECORD and PLAY knobs, VIDEO RECORD knob, and EQUALIZATION knob (eight total) as follows:

a. Pry top caps off, using a small knife or screwdriver.

b. Remove knobs using a collet tool (Ampex Part No. 360-489). If tool is not available, insert small screwdriver into knob metal slot and turn knob clockwise to free it from potentiometer shaft.

STEP 4 Remove ribbon cable between J1 on Primary Control Panel PWA and J1 on Secondary Control Panel PWA.

STEP 5 Disconnect two spade lugs from each meter (eight total).

STEP 6 Remove 12 cross-recessed screws that secure the Primary Control Panel PWA to the control panel assembly and remove the PWA. These are nine 4-40-in. x 1.00-in. long screws and three 6-32-in. x 0.375-in. long screws as shown in Figure 6-11.

STEP 7 Remove component support panel (1450617) from Primary Control Panel PWA by removing nine potentiometer mounting nuts from front of panel. See Figure 6-12.

STEP 8 Reinstall Primary Control Panel PWA in reverse order of removal.

6-50 Secondary Control Panel PWA

To remove Secondary Control Panel PWA from control panel assembly, proceed as follows:

STEP 1 Remove control panel assembly from control panel chassis as described in paragraph 6-48.

STEP 2 Remove Primary Control Panel PWA from control panel assembly as described in paragraph 6-49.

STEP 3 Remove HOURS meter (refer to Figure 6-10) from secondary control panel bracket by removing two 4-40 x 0.025-in. long panhead screws.

STEP 4 Remove secondary control panel bracket (1450633) from control panel assembly (1450610) by loosening three 6-32 x 0.500-in. long hex spacers and one 6-32 nut. Slide bracket out from spacers. (See Figure 6-12.)

STEP 5 Remove secondary control panel (1450611) from secondary control panel bracket (1450633) by removing five 4-40-in. x 0.312-in. long panhead screws.

STEP 6 Remove Secondary Control Panel PWA (1450640) from secondary control panel bracket by removing seven 2-56 x 0.250-in. long panhead screws.

STEP 7 Reinstall Secondary Control Panel PWA in reverse order of removal.

6-51 Timer Idler Assembly

The timer idler assembly is removed and reinstalled, at front of transport, as follows:

STEP 1 Remove transport trim as described in Part I, paragraph 4-12.

STEP 2 Detach connector P1 at Tape Timer Tach/TIP PWA. See Figure 6-13.

STEP 3 Using a 9/64-inch ball-ended hex-drive wrench, remove three hex-recessed screws and lock washers, and detach timer idler assembly from front of transport.

STEP 4 Reinstall timer idler assembly on transport in reverse order of removal.

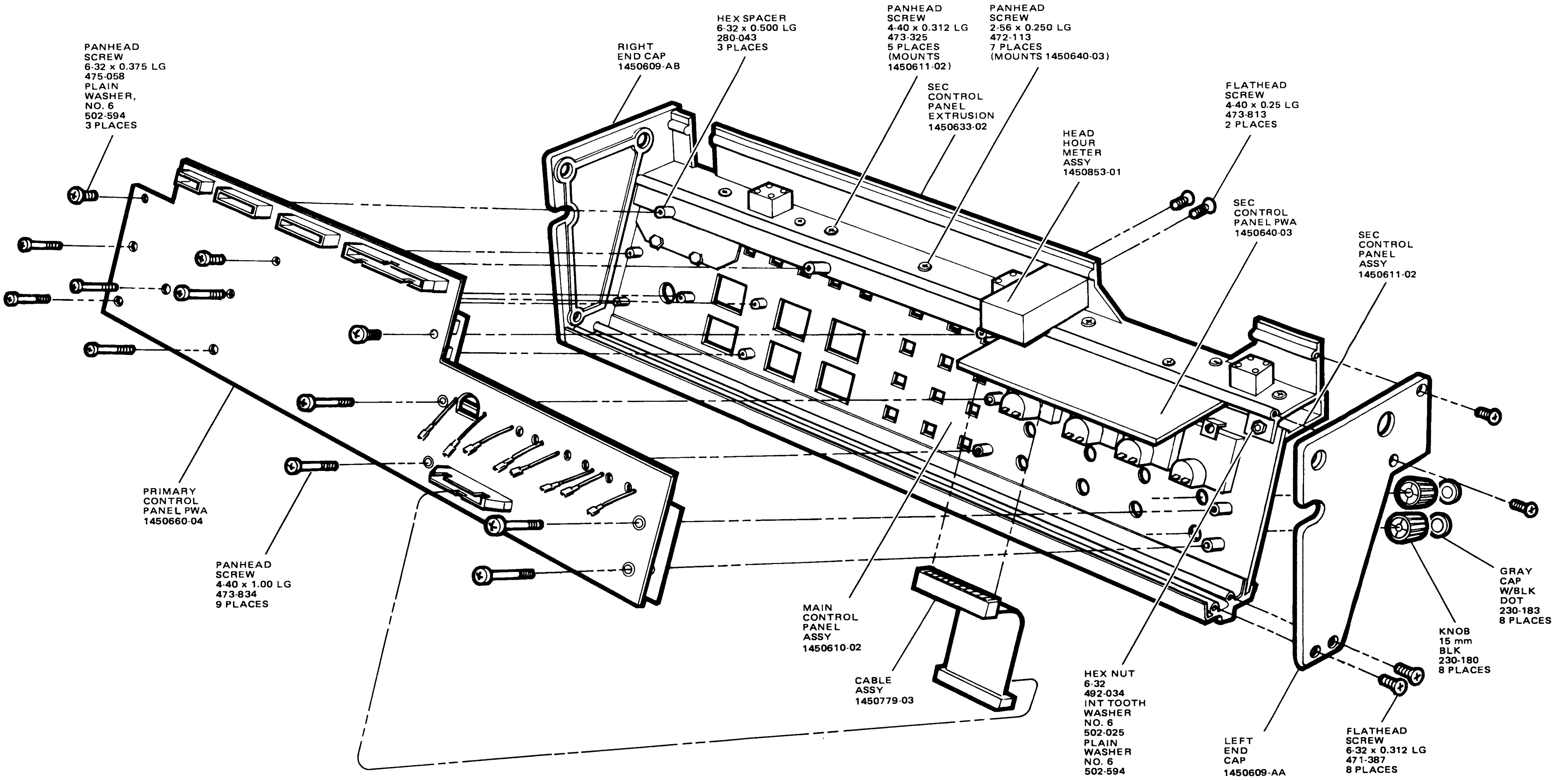

PANHEAD SCREW 6-32 x 0.375 LG 475-058 PLAIN WASHER, NO. 6 502-594 3 PLACES
RIGHT END CAP 1450609-AB
HEX SPACER 6-32 x 0.500 LG 280-043 3 PLACES
PANHEAD SCREW 4-40 x 0.312 LG 473-325 5 PLACES (MOUNTS 1450611-02)
PANHEAD SCREW 2-56 x 0.250 LG 472-113 7 PLACES (MOUNTS 1450640-03)
SEC CONTROL PANEL EXTRUSION 1450633-02
HEAD HOUR METER ASSY 1450853-01
FLATHEAD SCREW 4-40 x 0.25 LG 473-813 2 PLACES
SEC CONTROL PANEL PWA 1450640-03
SEC CONTROL PANEL ASSY 1450611-02
PRIMARY CONTROL PANEL PWA 1450660-04
PANHEAD SCREW 4-40 x 1.00 LG 473-834 9 PLACES
MAIN CONTROL PANEL ASSY 1450610-02
CABLE ASSY 1450779-03
HEX NUT 6-32 492-034 INT TOOTH WASHER NO. 6 502-025 PLAIN WASHER NO. 6 502-594
LEFT END CAP 1450609-AA
FLATHEAD SCREW 6-32 x 0.312 LG 471-387 8 PLACES
KNOB 15 mm BLK 230-180 8 PLACES
GRAY CAP W/BLK DOT 230-183 8 PLACES

Figure 6-11.
Control Panel Assembly
Exploded View

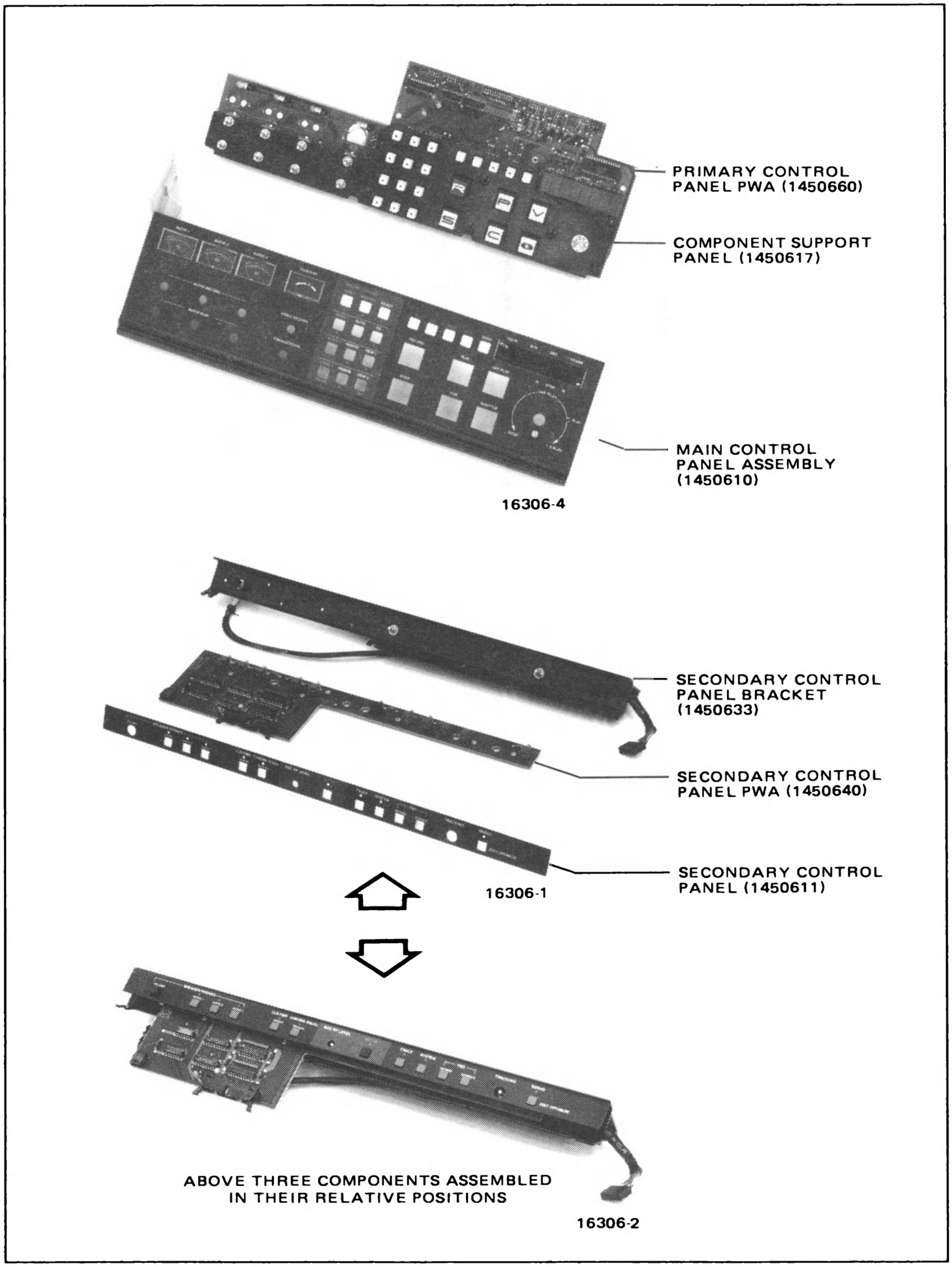

PRIMARY CONTROL PANEL PWA (1450660)
COMPONENT SUPPORT PANEL (1450617)
MAIN CONTROL PANEL ASSEMBLY (1450610)
16306-4
SECONDARY CONTROL PANEL BRACKET (1450633)
SECONDARY CONTROL PANEL PWA (1450640)
SECONDARY CONTROL PANEL (1450611)
16306-1
ABOVE THREE COMPONENTS ASSEMBLED IN THEIR RELATIVE POSITIONS
16306-2

Figure 6-12. Control Panel Assembly Major Components

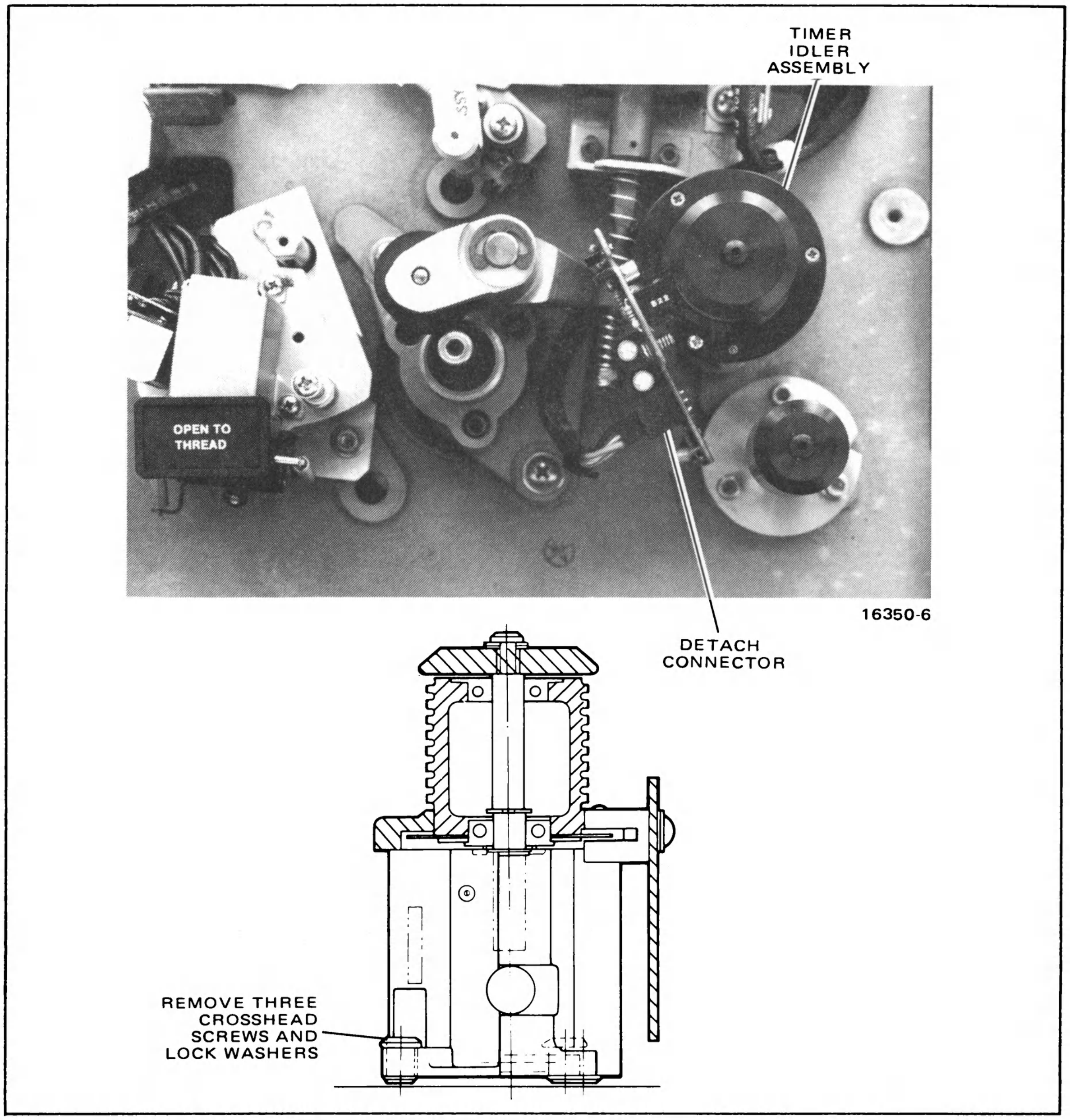


Figure 6-13. Removing Timer Idler Assembly

6-52 PART REPLACEMENT

Instructions for replacement of lamps and switches within the control panel assembly, and parts associated with the timer idler assembly are given in the following paragraphs.

6-53 Primary Control Panel PWA

The following paragraphs cover replacement of lamps and switches on the Primary Control Panel PWA.

6-54 Pushbutton Incandescent Lamps

Pushbutton lamps RECORD, PLAY, VAR PLAY, STOP, CUE, and SHUTTLE can be changed from the front of the console without removing any internal components. To change a lamp, proceed as follows:

STEP 1 Use thumb and forefinger to squeeze lens at indentations, and pull up to disengage lens from switch.

STEP 2 Replace lamp with a type 382 incandescent lamp (14V, midget flanged base, Ampex Part No. 060-407).

6-55 Meter Lamps and Illuminated Switches

The four meters are illuminated with the same type incandescent lamp (type 382) used for the RECORD, PLAY, VAR PLAY, STOP, CUE, and SHUTTLE pushbuttons. These lamps are mounted in sockets located on the Primary Control Panel PWA.

In the event of failure of an LED switch/indicator, it is recommended that the LED and switch be replaced as a unit. Proceed as follows:

STEP 1 Remove Primary Control Panel PWA from control panel assembly as described in paragraph 6-49.

STEP 2 Meter lamps (type 382) plug directly into lamp sockets DS24 through DS27. Replace lamps as required.

STEP 3 To replace an LED switch/indicator, use the following parts as required.

Switch/indicators DS1-DS5 (red LED)	Ampex Part No. 581-400
Switch/indicators DS6-DS12 and DS15, DS16 (green LED)	Ampex Part No. 581-846

STEP 4 Reinstall Primary Control Panel PWA in reverse order of removal.

6-56 Secondary Control Panel PWA

To change a switch or LED on the Secondary Control Panel PWA, proceed as follows:

STEP 1 Remove Secondary Control Panel PWA from control panel assembly as described in paragraph 6-50.

STEP 2 Replace switches and/or lamps using the following parts as required.

Switches S1 - S5 and S7 - S11 (dark gray)	Ampex Part No. 119-867
Switch S6 (black)	Ampex Part No. 119-850

Indicators (LED) DS7, DS8, DS11 (red)	Ampex Part No. 581-844
Indicators (LED) DS1 - DS6 (green)	Ampex Part No. 581-845

STEP 3 Reinstall Secondary Control Panel PWA in reverse order of removal.

6-57 Timer Idler Assembly

Use these instructions to replace timer idler bearings or Tape Timer Tach/TIP PWA on timer idler assembly.

6-58 Timer Idler Bearings

The timer idler assembly contains an upper and lower flanged ball bearing. If bearing replacement is required, bearings (Ampex Part No. 420-063) should be replaced as a pair. To replace bearings, proceed as follows:

STEP 1 Remove transport trim as described in paragraph 4-12, Part I..

STEP 2 Detach connector P1 at Tape Timer Tach/TIP PWA. Refer to Figure 6-13.

STEP 3 Using a 9/64-inch ball-ended hex-drive wrench, remove three hex-recessed screws and lock washers, and detach timer idler assembly from front of transport.

STEP 4 See Figure 6-14. Remove Tape Timer Tach/TIP PWA from timer idler assembly by removing two 4-40 panhead screws, lock washers, and flat washers. Retain compression spring.

STEP 5 Remove idler cap by removing a 6-32 buttonhead screw, No. 6 lock washer, and plain washer.

STEP 6 Remove wavy washer, shim (if present), and shim washer beneath cap.

STEP 7 Carefully lift roller, with upper bearing attached, from shaft. Discard bearing.

STEP 8 Remove two 2-56 flathead screws, and one 2-56 panhead screw and washer that secure idler flange to stanchion. Remove flange from stanchion.

STEP 9 Remove upper E-type retaining ring that retains lower ball bearing on shaft.

CAUTION

COUNTER DISK IS FRAGILE—USE CARE NOT TO DISTORT DISK. COUNTER DISK MUST BE REPLACED (LATER) WITH CORRECT SIDE UP. BEFORE REMOVING DISK, PLACE A PIECE OF LOW-TACK TAPE, LABELED UP, ON TOP OF DISK, OR MAKE A MARK WITH A FELT PEN.

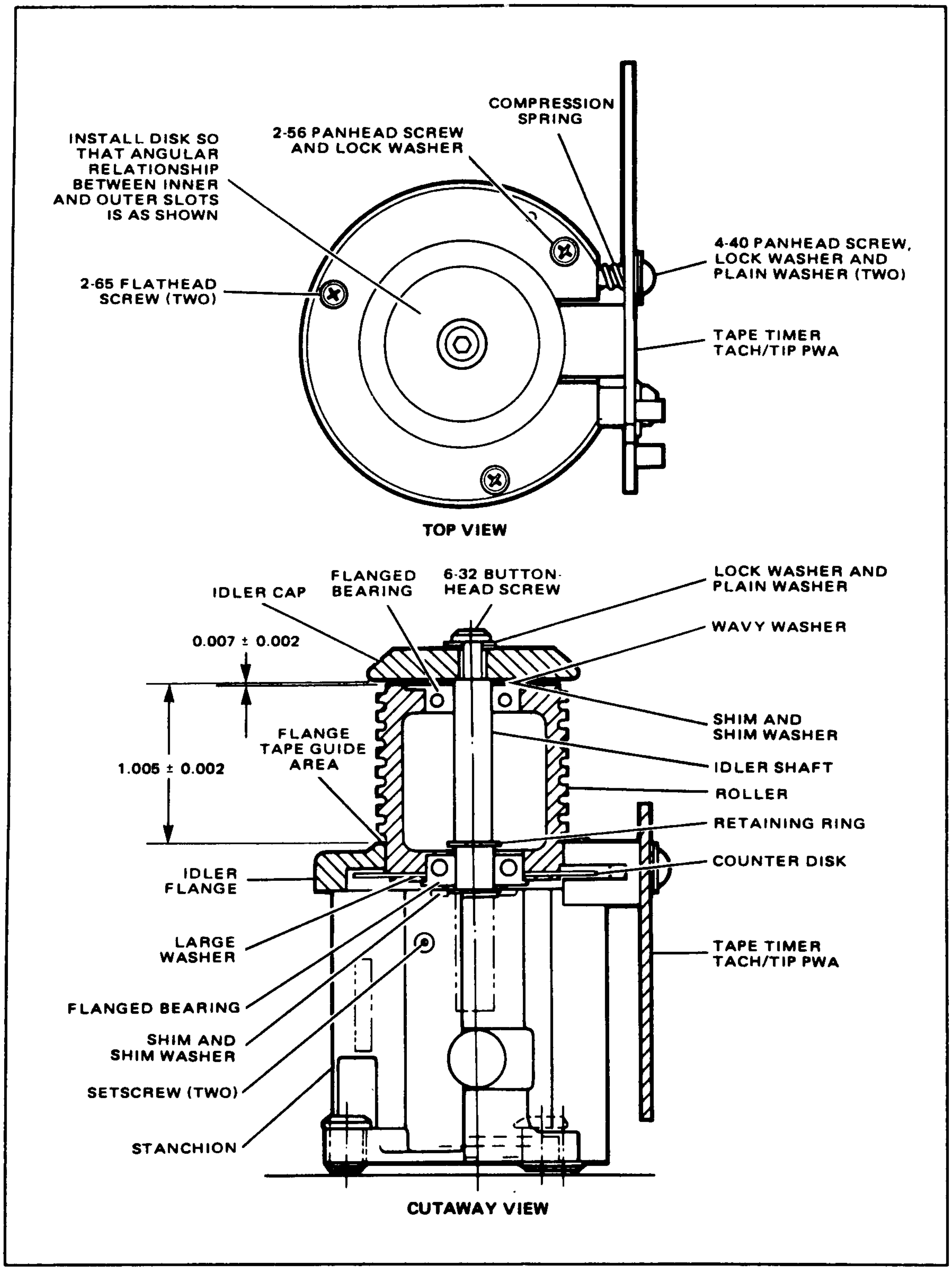


Figure 6-14. Replacing Timer Idler Bearings

STEP 10 Carefully remove lower bearing along with counter disk and large backing washer (immediately below disk) from shaft. Do not remove hardware, consisting of two shim washers and a retaining ring, below bearing.

STEP 11 Counter disk is attached to lower bearing. Free the counter disk from bearing by slightly bowing disk so it slides off bearing. Discard bearing.

Note

Perform the following steps on a clean workbench surface.

STEP 12 With the two shim washers that were left on shaft in step 10 resting on lower retaining ring, install new lower bearing on shaft, flange side down.

STEP 13 Install large backing washer on new lower bearing.

STEP 14 Install counter disk as follows: The counter disk must be installed correct side up. (If disk side was not identified as previously described, refer to Figure 6-14 for proper pattern and phase relationship of inner and outer disk holes.) Bow disk slightly while placing disk on lower bearing so that the three lobes on the disk inner diameter are deformed evenly. Use counter roller as a tool to press counter disk down against large backing washer. If tack tape was installed on disk, remove tape gently and any adhesive residue.

STEP 15 Reinstall retaining ring removed in step 9.

STEP 16 Carefully reinstall flange onto stanchion while being careful not to bend counter disk. Secure with three screws removed in step 8.

STEP 17 Reinstall roller onto lower bearing.

STEP 18 Install new upper bearing onto shaft and into center of roller.

STEP 19 Install shim washer and seat on bearing. Install shim (if present) removed in step 6.

STEP 20 Install wavy washer on top of shim. Washer must be centered on the shaft and not slip during cap replacement.

STEP 21 Using care not to dislodge wavy washer and shim(s), install timer idler cap on end of shaft and secure with hardware removed in step 4.

STEP 22 Using feeler gauge or plastic shim, check space between cap and roller. If space is not 0.007 ±0.002 inches (0.1778 ±0.0508 mm), or if roller does not spin freely, remove cap and firmly press on upper bearing to assure bearing is seated. Reinstall cap.

STEP 23 Again check requirements of step 22. If the problem still exists, hold assembly toward light to visually observe space between cap and roller. Hold stanchion with one hand and raise roller with the other. If space does not disappear, a washer is pinched between cap and shaft. Check position of wavy washer and shims and repeat requirements of steps 22 and 23.

STEP 24 Check height between idler cap and flange tape guide area. Height should be 1.005 ±0.002 inches (25.5270 ±0.0508 mm). If necessary, loosen two 6-32 setscrews (120° apart) on stanchion and adjust shaft height to dimension specified by lowering or raising idler cap. Tighten setscrews.

STEP 25 Reinstall Tape Timer Tach/TIP PWA using spring and hardware removed in step 4. Before tightening screws, ensure tach disk is centered in slot of optical sensor. Spin roller to assure free rotation of disk.

STEP 26 Reinstall timer idler on transport using hardware removed in step 3.

STEP 27 Reconnect connector P1 disconnected in step 2.

STEP 28 Check and adjust Tape Timer Tach/TIP PWA alignment as described in paragraph 6-61.

STEP 29 Reinstall transport trim removed in step 1.

6-59 Tape Timer Tach/TIP PWA

Use the following instructions to remove and replace the Tape Timer Tach/TIP PWA on timer idler assembly. To preclude the possibility of bending the fragile counter disk, the idler is first removed from the transport. Proceed as follows:

STEP 1 Remove transport trim as described in paragraph 4-12, Part I.

STEP 2 Detach connector P1 at the Tape Timer Tach/TIP PWA. Refer to Figure 6-13.

STEP 3 Using a 9/64-inch ball-ended hex-drive wrench, remove three hex-recessed screws and lock washers, and detach timer idler assembly from front of transport.

STEP 4 Refer to Figure 6-14. Remove Tape Timer Tach/TIP PWA from timer idler assembly by removing two 4-40 panhead screws, lock washers, and flat washers. Retain compression spring.

STEP 5 Reinstall Tape Timer Tach/TIP PWA using spring and hardware removed in step 4. Before tightening screws, ensure tach disk is centered in slot of optical sensor. Spin roller to assure free rotation of disk.

STEP 6 Reinstall timer idler assembly on transport using hardware removed in step 3.

STEP 7 Reconnect connector P1 disconnected in step 2.

STEP 8 Check and adjust Tape Timer Tach/TIP PWA alignment as described in paragraph 6-61.

STEP 9 Reinstall transport trim removed in step 1.

6-60 CONTROL SYSTEM ALIGNMENT

6-61 Tape Timer Tach/TIP PWA

The VPR-80 control system is very sensitive to misalignment of the Tape Timer Tach/TIP PWA. Alignment must be done in sequence given below. Refer to PWA Drawing No. 1468560 and Schematic Diagram No. 1468562 as necessary.

6-62 Tach Amplitude

Tach amplitude must be checked and adjusted if components have been replaced on Tape Timer Tach/TIP PWA. Proceed as follows:

STEP 1 Remove transport trim as outlined in paragraph 4-12, Part I.

STEP 2 Install a reel of prerecorded tape on supply turntable, and thread tape to takeup reel.

STEP 3 Connect scope channel 1 probe to U1-3 (tach A) on Tape Timer Tach/TIP PWA. See Figure 6-15.

STEP 4 Press PLAY.

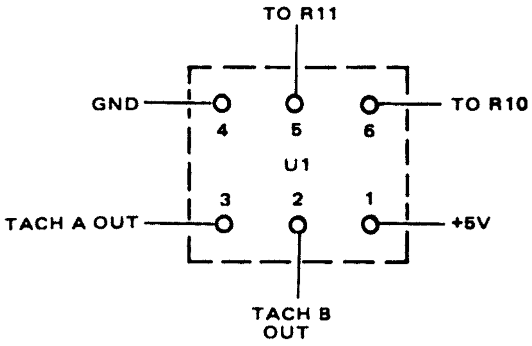


Figure 6-15. Tape Timer Tach Pickup (U1) Pinout

STEP 5 Observing scope, adjust R10 so that tach A has 600 mVp-p amplitude. See Figures 6-16 and 6-17.

STEP 6 Move scope channel 1 probe to U1-2 (tach B) on Tape Timer Tach/TIP PWA. See Figure 6-15.

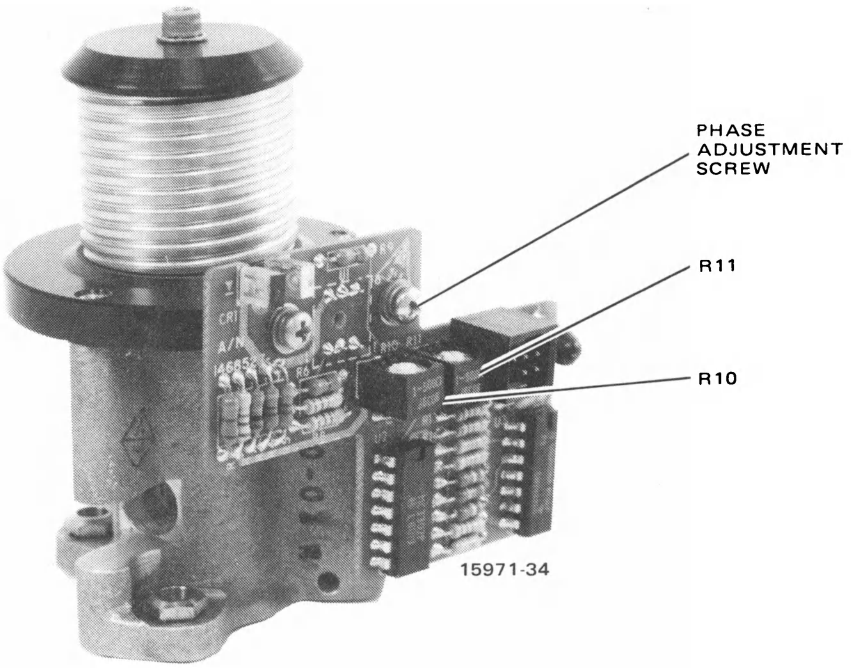


Figure 6-16. Timer Idler Assembly Adjustments

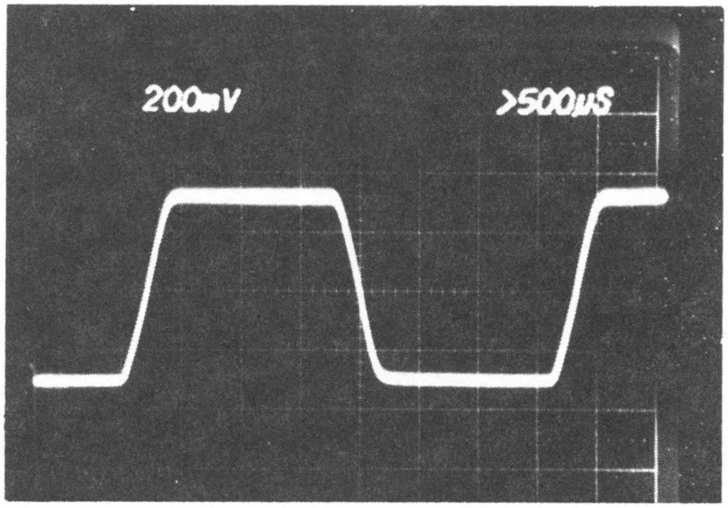


Figure 6-17. Typical Output Waveform of Tach A

STEP 7 Observing scope, adjust R11 so that tach B has 600 mVp-p amplitude. See Figures 6-16 and 6-17.

6-63 Tach A to B Phasing

Tape timer tach must be adjusted so that A and B pulses are 90° out of phase. Proceed as follows:

STEP 1 Place Control PWA (PWA6) on an extender.

STEP 2 Install a reel of prerecorded tape on supply turntable, and thread tape to takeup reel.

STEP 3 Connect scope channel 1 probe to PWA6, pin 61 (tach A). Connect scope channel 2 probe to PWA6, pin 62 (tach B). Trigger scope from channel 1.

STEP 4 Adjust horizontal sweep of scope so that square wave on channel 1 is 8 cm wide on scope graticule. See Figure 6-18.

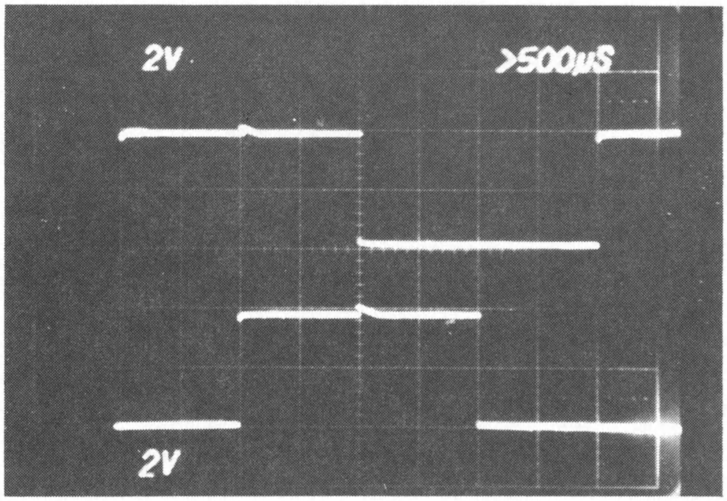


Figure 6-18. Tape Timer Tach Amplitude and Phasing Correctly Aligned

STEP 5 Press PLAY.

STEP 6 Adjust R10 on Tape Timer Tach/TIP PWA (Figure 6-16) for a symmetrical square wave at PWA6, pin 61.

STEP 7 Adjust R11 on Tape Timer Tach/TIP PWA (Figure 6-16) for a symmetrical square wave at PWA6, pin 62.

STEP 8 Adjust phase screw (Figure 6-16B) to establish a 90° out-of-phase relationship between tach pulses A and B. Tach B edges are ±2 cm from tach A. See Figure 6-18.

6-64 4X Tach Alignment

The 4X tach alignment is a very fine adjustment of R10 and R11 on the Tape Timer Tach/TIP PWA. Proceed as follows:

STEP 1 Install a reel of prerecorded tape on supply turntable, and thread tape to takeup reel.

STEP 2 Connect scope channel 1 probe to TP6 (4X TAPE TACH) on Control PWA.

STEP 3 Set scope main time base to 0.2 μs/cm.

STEP 4 Set scope-delayed time base to 50 μs/cm.

STEP 5 Press PLAY.

STEP 6 Carefully adjust R10 or R11 on Tape Timer Tach/TIP PWA to group pulses in the shortest space of time. See Figures 6-19 and 6-20.

STEP 7 Apply a small amount of Glyptol, or equivalent, to phase adjustment screw to preserve this alignment.

6-65 Performance Verification

Control system demonstration procedures provide a summary confidence check of control panel functions/indications and communication with the Control PWA in all nonedit and edit modes. A more detailed checkout (including fault isolation) requires use of the diagnostic probe accessory.

6-66 Control System Demonstration (Nonedit Modes)

The following nonedit mode demonstration checks out control system capabilities as the VPR-80 is sequenced through all nonedit modes (and conditions thereof).

Setup for the nonedit mode demonstration procedure is as follows:

- With power on, thread an expendable work tape of prerecorded program material on the transport.
- With power off, connect a convenient test signal (sine-squared pulse and bar) to the VIDEO IN connector.
- Connect an audio oscillator set for 1-kHz output at station operating level to AUDIO 1-3 connectors.
- Do *not* connect station reference video input to the REF VIDEO IN connector.
- Connect a picture monitor to the MONITOR VIDEO OUT connector.
- Set PWA edge AST ON/OFF switch 4S3 to ON position.

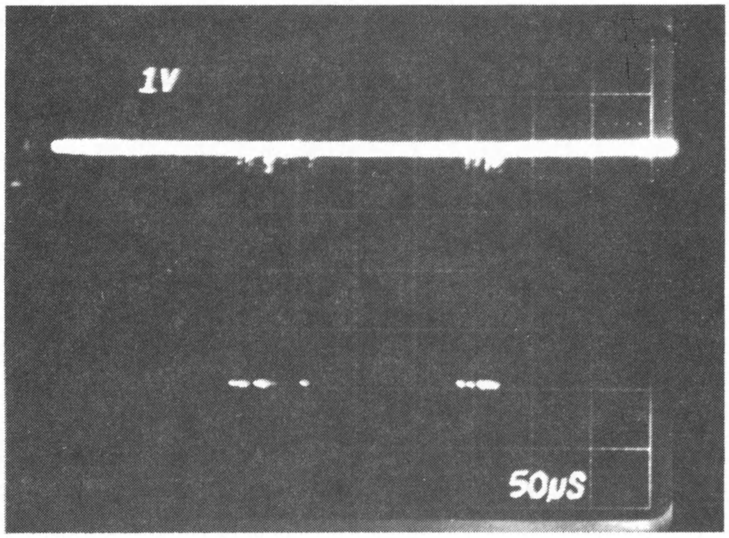


Figure 6-19. 4X Tach Misaligned

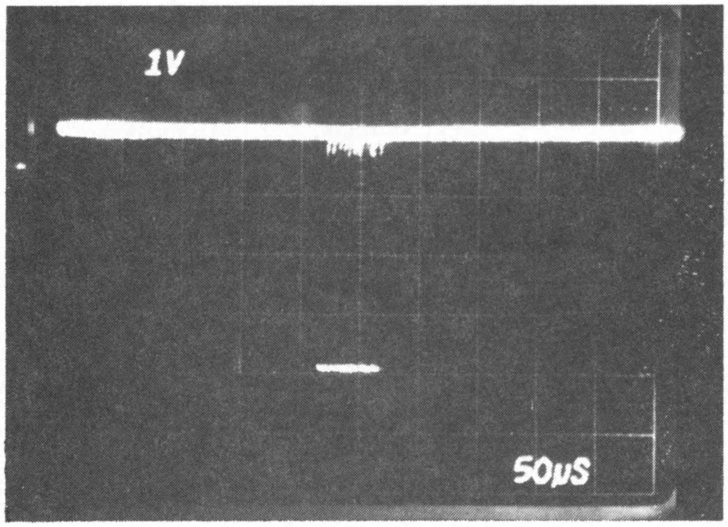


Figure 6-20. 4X Tach Correctly Aligned

- Set PWA edge CLR FRAME switch 6S3 to ON position.
- Set PWA edge REF SELECT switch 6S5 to REF position.
- Set PWA edge PREROLL SEL switch 6S6 to 5/7 position.
- Ensure that end-of-tape point (auto stop) is enabled. (Check setup code **3.**)
- Ensure that other PWA edge switches are set as required by applicable format standards and station facilities (i.e., TBC, etc.).
- Ensure that all audio and video I/O level controls are in center detent (unity) position.

Table 6-4, at the end of the demonstration procedure, summarizes control system nonedit mode capabilities which are exercised in the procedure.

Control System Demonstration (Nonedit Modes)

Step	Action	Response
1	Turn PWR switch ON.	VPR-80 wakes up in stop mode/standby condition. ● STOP indicator lights ● EE indicator lights ● CPU indicators 5DS1 and 6DS2 (green LEDs) begin blinking ● Meters display input levels
2	Press READY.	Scanner motor starts, and ● READY indicator lights ● SERVO indicator lights ● SYSTEM indicator lights ● SERVO indicator goes out when scanner motor reaches lock speed
3	Press SYSTEM.	● SYSTEM code **01** is displayed ● SYSTEM indicator goes out
4	Turn PWR switch OFF.	● All indicators go out ● Meters off ● Scanner motor runs down
5	Connect station reference video (REF VIDEO IN).	-------
6	Turn PWR switch ON.	VPR-80 wakes up in stop mode/standby condition. ● STOP indicator lights ● EE indicator lights ● CPU indicators 5DS1 and 6DS2 (green LEDs) begin blinking ● Meters display input levels

Note

Ensure that neither INSERT nor ASSEM indicator is lighted.

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

Step	Action	Response
7	Press READY.	Scanner motor starts, and • READY indicator lights • SERVO indicator lights • SERVO indicator goes out when scanner motor reaches lock speed
8	Shuttle tape forward 2 min of tape time and return to stop mode.	--------
9	Press ZERO.	• Tape time display indicates 00:00:00:00
10	Hold RECORD down, and press MASTER RECORD LOCKOUT.	• MASTER RECORD LOCKOUT indicator lights
11	Press PLAY and RECORD at the same time.	Tape is tensioned, pinch roller is engaged, tape moves forward at play speed, and attempt to enter record mode is unsuccessful. • RECORD indicator does not light • PLAY indicator lights • Tape time display advances
12	Press STOP.	Tape motion stops, tape tension is released, pinch roller is disengaged, and • PLAY indicator goes out • STOP indicator is lighted
13	Hold RECORD switch down, and press MASTER RECORD LOCKOUT switch.	• MASTER RECORD LOCKOUT indicator goes out

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

Step	Action	Response
14	Press CUE.	Tape rewinds to cue minus preroll, and • STOP indicator goes out • CUE indicator lights • Tape time display goes to 23:59:55:00 (NTSC), or 23:59:53:00 (PAL) • CUE indicator goes out • STOP indicator lights
15	Press PLAY and RECORD at the same time.	Tape is tensioned, pinch roller is engaged, tape moves forward at record speed, and • RECORD indicator lights • PLAY indicator lights • Tape time display advances • PLAY indicator goes out when record mode is entered
16	Vary AUDIO RECORD control for channels 1-3 and return to detent position.	• AUDIO 1—3 meters follow AUDIO RECORD controls
17	Vary VIDEO RECORD control and return to detent position.	• VIDEO/RF meter follows VIDEO RECORD control
18	Press STOP.	Tape motion stops, tape tension is released, pinch roller is disengaged, and • RECORD indicator goes out • STOP indicator lights
19	Press CUE.	• STOP indicator goes out • CUE indicator lights Tape rewinds to cue minus preroll, and • Tape time display goes to 23:59:55:00 (NTSC), or 23:59:53:00 (PAL) Tape travel stops, and • CUE indicator goes out • STOP indicator lights
20	Press EE.	• EE indicator goes out

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

Step	Action	Response
21	Press PLAY.	Tape is tensioned, pinch roller is engaged, tape moves forward at play speed, color bars and 1-kHz audio recorded in step 15 can be monitored, and • PLAY indicator lights • Tape time display advances
22	Turn audio VOLUME control to midrange.	-------
23	Press AUDIO 1.	1-kHz tone is audible at speaker, and • AUDIO 1 indicator lights
24	Press AUDIO 2.	Volume of 1-kHz tone increases, and • AUDIO 2 indicator lights
25	Press AUDIO 3.	Volume of 1-kHz tone increases, and • AUDIO 3 indicator lights
26	Press AUDIO 1—3.	Audio monitor is muted, and • AUDIO 1—3 indicators go out
27	Press TSO RETARD.	Tape speed decreases by 7%*.
28	Press TSO ADVANCE.	Tape speed increases by 7%*.
29	Set PWA edge AST switch 4S3 to OFF position.	-------
30	Vary TRACKING control, and return control to original setting.	Observe breakup on picture monitor.

*Evidenced by SERVO indicator which lights momentarily when TSO switches are released.

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

Step	Action	Response
31	Set PWA edge AST switch 4S3 to ON position.	-------
32	Press CUE twice.	• PLAY indicator goes out • CUE indicator flashes Tape rewinds back to tape time 00:00:00:00 (no preroll), stops, and • CUE indicator goes out • STOP indicator is lighted

Note

If left in this condition for four minutes, automatic switchover from tape to EE operation, as outlined in step 39, will occur. Therefore, if READY indicator begins flashing, press READY to reset the 3.5-minute timer.

33	Press SET UP.	• SET UP indicator is lighted • Tape time display is blanked
34	Press keypad switches 2, then 0.	• Tape time display indicates 20 • SET UP indicator remains on
35	Press ENTER.	• Tape time display shows four 2-digit hex indications

Note

Third and fourth digits from the left indicate the analog value of the TRACKING control. Make note of this hex indication.

36	Vary TRACKING control over its entire range, and return control to original setting.	Hex indication follows TRACKING control. The indication ranges from 00 to FE. 7F or 80 is indicated when in detent position.

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

Step	Action	Response
37	Press SET UP.	Setup mode is exited, and • STOP indicator remains lighted • SET UP indicator goes out • Hex indications are blanked, and tape time display (00:00:00:00) reappears
38	Shuttle tape forward 1 minute of tape time.	-------
39	Press STOP.	Stop mode still-frame playback can be observed on picture monitor. After 3.5 minutes of stop mode still-frame playback, • READY indicator begins flashing • STOP indicator remains on After 4 minutes of stop mode/still-frame playback, tape tension is relaxed, and • READY indicator stops flashing and remains on steadily • EE indicator begins flashing • STOP indicator remains on

Note

Automatic switchover from tape to EE operation (stop mode), as described above, will also occur after four minutes in the following modes/conditions:

Mode	Condition	See Step
Cue	Rewind to entrance point (no preroll)	32
Variable play	Tape speed control in variable play STOP position (max ccw)	43, 49
Variable play	Pause	47
Shuttle	Rewind or fast forward to near end-of-tape (EOT) point	51, 61
Shuttle	Tape speed control in shuttle mode STOP (detent) position	53

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

Step	Action	Response
40	Press EE.	• EE indicator stops flashing and remains on steadily • READY indicator remains on
41	Press EE (second time).	Tape is tensioned, and • EE indicator goes out • READY indicator remains on
42	Turn tape speed control to VAR PLAY STOP position (max ccw).	---------
43	Press VAR PLAY.	Variable play mode/still-frame playback can be observed, and • VAR PLAY indicator lights

Note

If left in this condition for four minutes, automatic switchover from tape to EE operation (and stop mode), as outlined in step 39, will occur. Therefore, if READY indicator begins flashing, press READY to reset the 3.5-minute timer.

Step	Action	Response
44	Rotate tape speed control toward PLAY position.	Tape advances at slow motion speeds (as observed on picture monitor). Tape speed is proportional to degree of knob rotation, and • VAR PLAY indicator remains lighted
45	Rotate tape speed control to 1.5 PLAY position (max cw).	Tape speed increases to 1.5X play speed (as observed on picture monitor), and • VAR PLAY indicator remains lighted
46	Rotate tape speed control to PLAY position.	Tape slows to normal play speed (as observed on picture monitor) and, • PLAY indicator lights • VAR PLAY indicator remains lighted

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

<table>
<tr><th>Step</th><th>Action</th><th>Response</th></tr>
<tr><td>47</td><td>Press VAR PLAY (second time).</td><td>Tape travel stops, pause condition/still-frame playback can be observed, and
• PLAY indicator remains on
• VAR PLAY indicator flashes</td></tr>
<tr><td colspan="3">Note
If left in this condition for four minutes, automatic switchover from tape to EE operation (and stop mode), as outlined in step 39, will occur. Therefore, if READY indicator begins flashing, press READY to reset the 3.5-minute timer.</td></tr>
<tr><td>48</td><td>Press VAR PLAY (third time).</td><td>Pause condition is exited, tape travel resumes at play speed, and
• PLAY indicator remains on
• VAR PLAY indicator stops flashing and remains on steadily</td></tr>
<tr><td>49</td><td>Rotate tape speed control to variable play mode STOP position (max ccw).</td><td>Tape travel stops, and after 3.5 minutes of variable play mode/still-frame playback
• READY indicator begins flashing
• VAR PLAY indicator remains on</td></tr>
<tr><td>50</td><td>Press READY.</td><td>The 3.5-minute timer is retriggered, and
• READY indicator stops flashing and remains on steadily for another 3.5 minutes</td></tr>
<tr><td>51</td><td>Press SHUTTLE.</td><td>• SHUTTLE indicator is lighted
Tape rewinds at 300 in/s. At near end-of-tape point, tape travel stops, and
• SHUTTLE indicator remains on</td></tr>
</table>

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

<table>
<tr><th>Step</th><th>Action</th><th>Response</th></tr>
<tr><td colspan="3">Note
If left in this condition for four minutes, automatic switchover from tape to EE operation (and stop mode), as outlined in step 39, will occur. Therefore, if READY indicator begins flashing, press READY to reset the 3.5-minute timer.</td></tr>
<tr><td>52</td><td>Turn tape speed control cw past shuttle mode STOP (detent) position.</td><td>Tape forward speed is proportional to the degree of rotation of the control.</td></tr>
<tr><td>53</td><td>Rotate tape speed control shuttle mode STOP (detent) position.</td><td>Tape travel stops, pinch roller is to disengaged, shuttle mode/still-frame playback can be observed, and
• SHUTTLE indicator remains on</td></tr>
<tr><td colspan="3">Note
If left in this condition for four minutes, automatic switchover from tape to EE operation (and stop mode), as outlined in step 39, will occur. Therefore, if READY indicator begins flashing, press READY to reset the 3.5-minute timer.</td></tr>
<tr><td>54</td><td>Press STOP.</td><td>• SHUTTLE indicator goes out
• STOP indicator is lighted</td></tr>
<tr><td>55</td><td>Press SET UP.</td><td>• SET UP indicator is lighted
• Tape time display is blanked</td></tr>
<tr><td>56</td><td>Press keypad switches 2, then 0.</td><td>• Tape time display indicates 20
• SET UP indicator remains on</td></tr>
<tr><td>57</td><td>Press ENTER.</td><td>• Tape time display shows four 2-digit hex indications</td></tr>
<tr><td colspan="3">Note
First and second digits on the left indicate the analog value of the tape speed control.</td></tr>
</table>

(Continued next page)

Control System Demonstration (Nonedit Modes) (Continued)

<table>
<tr><th>Step</th><th>Action</th><th>Response</th></tr>
<tr><td>58</td><td>Vary tape speed control over its entire range and return control to detent position.</td><td>Hex indication follows SHUTTLE control, and ranges from 00 to FE. 7F or 80 is indicated when in detent position.</td></tr>
<tr><td>59</td><td>Press SET UP.</td><td>Setup mode is exited, and
● SET UP indicator goes out
● STOP indicator remains lighted
● Hex indications are blanked, and tape time display is resumed</td></tr>
<tr><td>60</td><td>Rotate tape speed control to max cw position.</td><td>-------</td></tr>
<tr><td>61</td><td>Press SHUTTLE.</td><td>Tape shuttles to takeup reel at 300 in/s, and
● SHUTTLE indicator lights
At near end-of-tape point, tape travel stops, and
● SHUTTLE indicator remains lighted</td></tr>
<tr><td colspan="3">Note
If left in this condition for four minutes, automatic switchover from tape to EE operation (and stop mode), as outlined in step 39, will occur. Therefore, if READY indicator begins flashing, press READY to reset the 3.5-minute timer.</td></tr>
<tr><td>62</td><td>Press SHUTTLE (second time).</td><td>Tape rewinds at 300 in/s. At near end-of-tape point, tape travel slows down, tape is slowly unthreaded, and scanner motor turns off.
● SHUTTLE indicator flashes
When tape exits TIP sensor,
● SHUTTLE indicator goes out
● STOP indicator is lighted</td></tr>
</table>

Table 6-4. Control System Performance Verification (Nonedit Modes)

Capability	Control	Indicator	Nonedit Mode Demonstration Procedure Step No(s).
AST on/off control	AST on/off	--------------	29.31
Audio playback monitoring			
Channel 1	AUDIO 1	AUDIO 1	23, 26
Channel 2	AUDIO 2	AUDIO 2	24, 26
Channel 3	AUDIO 3	AUDIO 3	25, 26
Volume control	VOLUME		22
Audio record level control	AUDIO RECORD 1-3	AUDIO 1-3 meters	16
Cue to preroll point	CUE	CUE	14.19
Cue without preroll	CUE	CUE (flashing)	32
Master record lockout	MASTER RECORD LOCKOUT	MASTER RECORD LOCKOUT	10, 13
Near EOT point protection-forward	--------------	--------------	61
Near EOT point protection-rewind	--------------	--------------	51
Nonstandard condition display and display control	SYSTEM	SYSTEM 7-segment display	2, 3
Playback mode	PLAY	PLAY	21
Record mode	RECORD (PLAY)	RECORD	15
Scanner motor control (incl. tension control)	READY	READY	2, 7
Servo unlock/lock indication	--------------	SERVO	2, 7
Setup mode command	SET UP	SET UP	33,37,55.59
	keypad	7-segment display	34. 56
	ENTER	7-segment display	35.57

(Continued next page)

Table 6-4. Control System Performance Verification (Nonedit Modes) (Continued)

Capability	Control	Indicator	Nonedit Mode Demonstration Procedure Step No(s).
Shuttle mode	SHUTTLE tape speed control	SHUTTLE	51,53, 60, 61
Still-frame playback			
Pause			
	VAR PLAY	VAR PLAY (flashing)	47, 48
Shuttle mode	SHUTTLE	SHUTTLE	53
Stop mode	STOP	STOP	39
Variable play mode	VAR PLAY	VAR PLAY	43,49
Stop mode–automatically commanded	------------	STOP	14,19, 32
Stop mode–manually commanded	STOP	STOP	12,18, 39,54
Tape/EE operation switch-over–automatic	------------	EE (flashing)	1, 6, 39
Tape/EE operation switch-over–manual	EE	EE	20, 40, 41
Tape/EE operation switch-over–timer override	READY	SHUTTLE, STOP, or VAR PLAY	50
Tape speed control (A/D conversion)	tape speed control	7-segment display	58
Tape speed override (TSO)	ADVANCE	SERVO	28
Advance	RETARD	SERVO	27
Retard			
Tracking control Analog indication	TRACKING	(picture monitor)	30
Digital indication	TRACKING	7-segment display	36
Unthread	SHUTTLE	SHUTTLE (flashing)	62

(Continued next page)

Table 6-4. Control System Performance Verification (Nonedit Modes) (Continued)

Capability	Control	Indicator	Nonedit Mode Demonstration Procedure Step No(s).
Variable play mode play speed	VAR PLAY and tape speed control	VAR PLAY and PLAY	46
1.5X play speed	VAR PLAY and tape speed control	VAR PLAY	45
slow motion	VAR PLAY and tape speed control	VAR PLAY	44
Video record level control	VIDEO RECORD	VIDEO/RF meter	17
Zero tape timer	ZERO	7-segment display	9

6-67 Control System Demonstration (Edit Modes)

The following demonstration procedure checks out VPR-80 audio/video editing capabilities. Edit optimization is performed first. Then an insert edit (in auto edit mode) is set up, previewed, made, and reviewed. This is followed by an assemble edit demonstration, and then an open-ended insert edit.

Setup for the edit mode demonstration procedure is as follows:

- Connect two VPR-80s (one source and one record VTR) via the multi-VTR cable as shown in Section 2 of the *VPR-80 Installation and Operation* manual.

Note

If a second VPR-80 is not available, any other video source can be used (camera, VTR, or video signal generator). Use of a second VPR-80 as source VTR in this procedure demonstrates multi-VTR remote control mode (transmission of synchronous cue and play commands to the source VTR).

- Thread a work tape of prerecorded color bars on the source VTR transport.
- Thread an expendable work tape of prerecorded program material on the record VTR transport.

- Connect the three audio outputs of the source VTR to the corresponding inputs of the record (editor) VTR.
- Connect the video output of the source VTR to the input of the record VTR through a TBC time-base corrector.
- Connect station reference video input to the REF VIDEO IN connector of the record VTR.
- Connect a picture monitor to the MONITOR VIDEO OUT connector of the record VTR.
- Ensure that end-of-tape point (auto stop) is enabled. (Check setup code 3.)
- Set PWA edge REF SELECT switch 6S5 to AUTO position.
- Ensure that other PWA edge switches are set as required by applicable format standards and station facilities (i.e., TBC, etc.).
- Ensure that all audio and video I/O level controls are in center detent (unity) position.

Table 6-5, at the end of the demonstration procedure, summarizes control system edit mode capabilities which are exercised in the procedure.

Control System Demonstration (Edit Modes)

Note

Steps in the following procedures are to be taken at the record (editor) VPR-80, unless specified otherwise.

Step	Action	Response
1	Shuttle tape forward two minutes of tape time and return to stop mode.	-----
2	Press ZERO.	• Tape time display indicates 00:00:00:00
3	With VPR-80 in stop mode/ ready condition, press INSERT switch.	• INSERT indicator lights
4	Press PLAY.	Tape is tensioned, pinch roller is engaged, tape moves forward at play speed, and • PLAY indicator lights

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response
5	Press EDIT OPTIMIZE.	• SERVO indicator lights during automated edit optimize procedure (about 15 seconds) • Displacement of the VIDEO/RF meter indication can also be observed
6	Shuttle tape forward two more minutes of tape time and return to stop mode.	Display indicates 00:02:00:00
7	Press ENTR.	• ENTR indicator lights • Most recent contents of entrance register are displayed (preserved in battery-protected RAM storage)
8	Press keypad ENTER.	• Display indicates 00:02:00:00 (current tape time) • ENTR indicator remains lighted
9	Press ENTR.	• ENTR indicator goes out
10	Press ENTR.	• ENTR indicator lights • Display indicates 00:02:00:00 (entrance point set in step 8)
11	Key in 2 min., 7 sec., and 10 frames.	• Display indicates 00:02:07:10 • ENTR indicator remains lighted
12	Press keypad ENTER.	• Display indicates 00:02:07:10 • ENTR indicator remains lighted
13	Press EXIT.	• ENTR indicator goes out • EXIT indicator lights • Most recent contents of exit register are displayed (preserved in battery-protected RAM storage)
14	Key in 2 min., 14 sec., and 15 frames.	• Display indicates 00:02:14:15 • EXIT indicator remains lighted

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response
15	Press keypad ENTER.	• Display indicates 00:02:14:15 • EXIT indicator remains lighted
16	Press EXIT.	• EXIT indicator goes out • Display indicates 00:02:00:00 current tape time)
17	Press and hold down (+) and (-) switches at the same time.	• Display indicates duration of proposed edit (00:00:07:05)
18	Release (+) and (-) switches.	• Display indicates current tape time (00:02:00:00)
19	Press ENTR.	• ENTR indicator is lighted • Display indicates 00:02:07:10 (entrance point set in step 11).
20	Press (+).	• P is displayed.
21	Key in 20 (NTSC), or key in 15 (PAL).	• **P20** (or **P15**) is displayed
22	Press keypad ENTER.	• Display indicates 00:02:08:00 (trimmed entrance point)
23	Press ENTR.	• Display indicates 00:02:00:00 (current tape time) • ENTR indicator goes out
24	Press EXIT.	• EXIT indicator lights • Display indicates 00:02:14:15 point (exit point set in step 14)
25	Press (-).	• - is displayed
26	Key in 15.	• -15 is displayed
27	Press keypad ENTER.	• Display indicates 00:02:14:00 (trimmed exit point)

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response
28	Press EXIT.	• Display indicates 00:02:00:00 (current tape time) • EXIT indicator goes out
29	Press and hold down (+) and (-) switches at the same time.	• Display indicates duration of trimmed edit interval (00:00:06:00)
30	Press AUDIO 2 RECORD LOCKOUT switch.	• AUDIO 2 indicator is lighted
31	Press AUDIO 3 RECORD LOCKOUT switch.	• AUDIO 3 indicator is lighted
32	At source VTR, shuttle tape forward two minutes of tape time and return to stop mode.	-----
33	At source VTR, press ZERO.	• Display indicates 00:00:00:00
34	At source VTR, press AUTO.	• AUTO indicator is lighted
35	At source VTR, press REM 2.	• REM 2 indicator is lighted
36	At record VTR, press AUTO.	• AUTO indicator is lighted
37	Press CUE.	Both VTRs cue to selected entrance preroll point and return to stop mode. Preroll is modified by 26 frames (22 in PAL) during Auto Edits if preroll exceeds 59 frames

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response	
38	Press PLAY to begin edit preview mode.	**At record VTR:**	**At source VTR:**
		AUTO indicator remains on	AUTO indicator remains on
		PLAY indicator turns on	PLAY indicator turns on
		EE indicator is off	EE indicator turns on
		At entrance point:	
		AUTO indicator begins flashing	
		PLAY indicator remains on	
		EE indicator turns on	
		At exit point:	
		AUTO indicator stops flashing and remains on	
		PLAY indicator remains on	
		EE indicator turns off	
39	Press STOP on both VTRs.	Both VTRs exit play mode and enter stop mode	
40	Press EXIT.	● EXIT indicator is lighted ● Display indicates exit point (00:02:14:00)	
41	Press CUE.	Both VTRs cue to the selected exit preroll point and return to stop mode.	

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response
42	Press PLAY to begin exit preview mode.	**At record VTR:** AUTO indicator begins flashing. PLAY indicator turns on. EE indicator turns on. **At source VTR:** AUTO indicator begins flashing. PLAY indicator turns on. EE indicator turns off. **At exit point:** AUTO indicator stops flashing and remains on. PLAY indicator remains on. EE indicator turns off.
43	Press STOP on both VTRs.	Both VTRs exit play mode and enter stop mode.
44	Press EXIT.	• EXIT indicator goes out
45	Press CUE.	Both VTRs cue to selected entrance preroll point and return to stop mode. Preroll is modified by 26 frames (22 in PAL) during Auto Edits if preroll exceeds 59 frames.
46	Press PLAY and RECORD at the same time to begin insert edit mode.	Both VTRs enter play mode. At the record VTR: • AUTO indicator remains on • PLAY indicator turns on • RECORD indicator turns on At the entrance point, record VTR enters record mode, and • AUTO indicator begins flashing • PLAY indicator turns off • RECORD indicator remains on

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response
46	Press PLAY and RECORD begin insert edit mode. (Continued)	At exit point, record VTR exits record at the same time tomode and enters play mode, and • AUTO indicator stops flashing and remains on • PLAY indicator turns on • RECORD indicator remains on
47	Press STOP on both VTRs.	Both VTRs exit play mode and enter stop mode.
48	Press PLAY twice to begin edit review mode.	Record VTR cues back to the selected entrance preroll point, and • CUE indicator is lighted • PLAY indicator flashes Preroll is modified by 26 frames (22 in PAL) during Auto Edits if preroll exceeds 59 frames. At preroll point, record VTR enters play mode, and • CUE indicator goes out • AUTO indicator remains on • PLAY indicator continues flashing **At entrance point:** • AUTO indicator begins flashing • PLAY indicator continues flashing **At exit point:** • AUTO indicator stops flashing and remains on • PLAY indicator stops flashing and remains on

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response
49	Press STOP.	Both VTRs exit play mode and enter stop mode.
50	Press AUDIO 2 RECORD LOCKOUT.	• AUDIO 2 indicator goes out
51	Press AUDIO 3 RECORD LOCKOUT.	• AUDIO 3 indicator goes out
52	Press INSERT.	• INSERT indicator goes out
53	Press ASSEM.	• ASSEM indicator is lighted
54	Press ENTR.	• ENTR indicator is lighted • Display indicates 00:02:08:00 (trimmed entrance point set in step 22)
55	Holding ENTR switch down, press EXIT.	• Display indicates 00:02:14:00 (the new entrance point)
56	Press ENTR.	• ENTR indicator goes out • Display indicates current tape time
57	Press CUE.	Both VTRs cue to selected entrance preroll point and return to stop mode. Preroll is modified by 26 frames (22 in PAL) during Auto Edits if preroll exceeds 59 frames.
58	Press PLAY and RECORD at the same time to begin assemble edit mode.	Both VTRs enter play mode. At the record VTR: • AUTO indicator remains on • PLAY indicator turns on • RECORD indicator turns on

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response
58	Press PLAY and RECORD at the same time to begin assemble edit mode. (Continued)	At the entrance point, record VTR enters record mode, and • AUTO indicator begins flashing • PLAY indicator turns off • RECORD indicator remains on
59	After 10 seconds of assemble edit recording, press STOP on both VTRs.	Both VTRs exit play mode and enter stop mode. At the record VTR: • AUTO indicator stops flashing and remains on • RECORD indicator turns off • STOP indicator is lighted
60	Press EXIT.	• EXIT indicator lights • Display indicates 00:02:14:00 (trimmed exit point set in step 27)
61	Key in 2 mins., 20 secs., and 00 frames	• Display indicates 00:02:20:00. • EXIT indicator remains lighted
62	Press keypad ENTER.	• Display indicates 00:02:20:00. • EXIT indicator remains lighted
63	Holding EXIT switch down, press ENTR.	• Display indicates 00:02:14:00 (entrance point set in step 55). Entrance and exit points are the same.
64	Press EXIT.	• EXIT indicator goes out • Display indicates current tape time
65	At record VTR, press INSERT.	• INSERT indicator is lighted • ASSEM indicator goes out
66	Press AUDIO 2 RECORD LOCKOUT.	• AUDIO 2 indicator is lighted
67	Press AUDIO 3 RECORD LOCKOUT.	• AUDIO 3 indicator is lighted

(Continued next page)

Control System Demonstration (Edit Modes) (Continued)

Step	Action	Response
68	Press VIDEO RECORD LOCKOUT.	● VIDEO indicator is lighted
69	Press CUE.	Both VTRs cue to selected preroll point ahead of entrance (and exit) point return to stop mode. Preroll is modified by 26 frames (22 in PAL) during Auto Edits if preroll exceeds 59 frames.
70	Press PLAY and RECORD switches at the same time	Both VTRs enter play mode. At the record VTR: ● PLAY indicator turns on ● RECORD indicator begins flashing At the entrance point, record VTR enters record mode, and ● PLAY indicator turns off ● RECORD indicator stops flashing and remains on
71	After 10 seconds, press STOP on both VTRs.	Record VTR exits record mode, and ● STOP indicator is lighted ● PLAY indicator remains off ● RECORD indicator turns off

Table 6-5. Control System Performance Verification (Edit Modes)

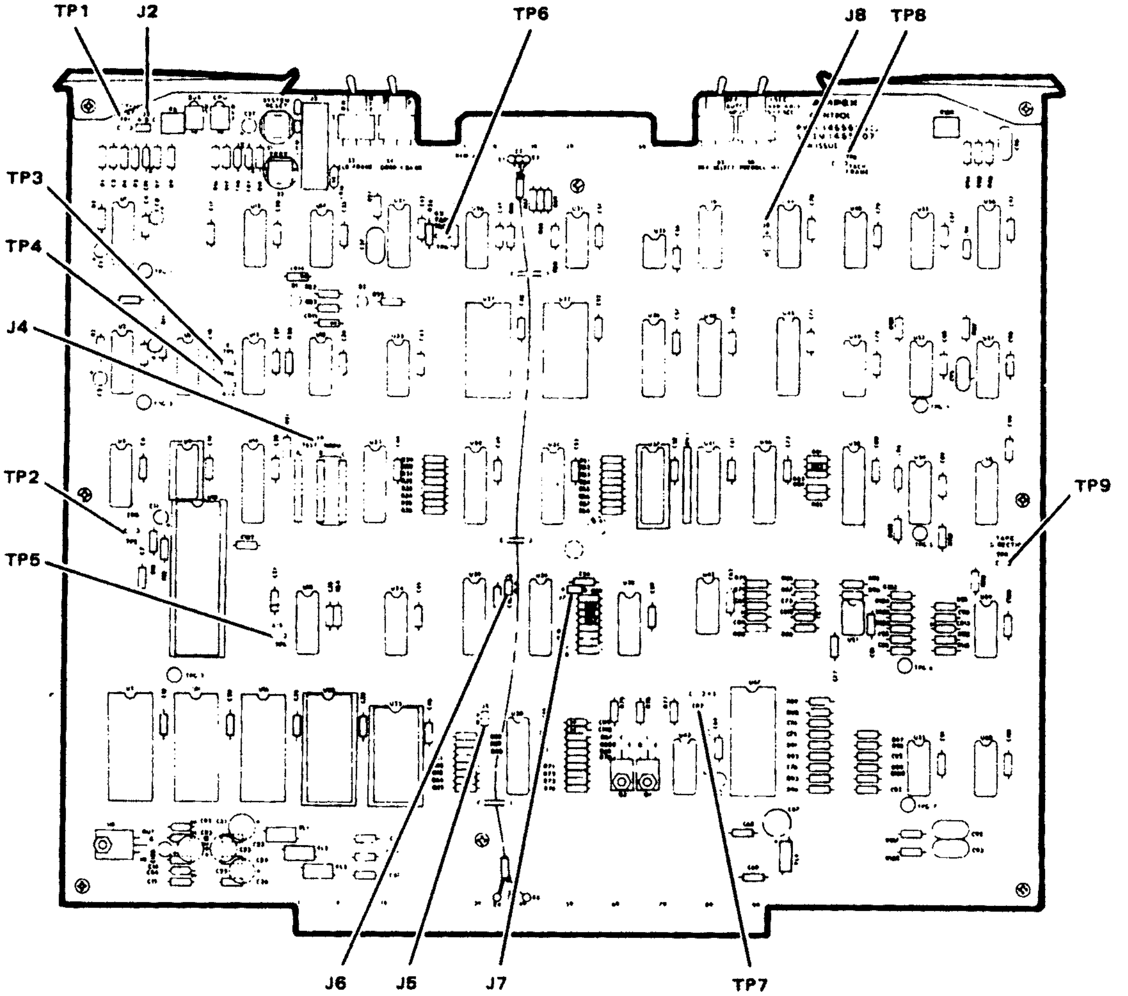
Capability	Control	Indicator	Edit Mode Demonstration Procedure Step No(s).
Auto assemble edit mode	ASSEM	ASSEM	53, 57–59
Auto insert edit mode	INSERT	INSERT	3, 45–47
Lockout of individual channels	AUDIO 2 AUDIO 3	AUDIO 2 AUDIO 3	30 31
Display of:			
Edit interval	(+) and (–)	7-segment display	17, 29
Entrance point	ENTR	7-segment display	19
Exit point	EXIT	7-segment display	24
Edit-optimize	EDIT OPTIMIZE	SERVO	5
Edit (cue) points:			
Entrance point:			
Set at current tape time.	ENTR 7-segment display	ENTR	7, 9
Set by keypad entry.	ENTR keypad	ENTR 7-segment display	10–12
Exit point:			
Set by keypad entry.	EXIT keypad display	EXIT 7-segment	13–16
Transfer:			
Entrance to exit	EXIT, ENTR	7-segment display	63, 64
Exit to entrance	ENTR, EXIT	7-segment display	54–56

(Continued next page)

Table 6-5. Control System Performance Verification (Edit Modes) (Continued)

Capability	Control	Indicator	Edit Mode Demonstration Procedure Step No(s).
Trimming:			
(+) Delayed	(+), keypad	7-segment display	19–23
(−) Advanced	(−), keypad	7-segment display	24–28
Multi-VTR control mode	AUTO	AUTO	34
	REM 2	REM 2	35
Open-ended edit mode	EXIT, ENTR	7-segment display	63, 64
	CUE PLAY RECORD	CUE PLAY RECORD	65, 71
Preview modes:			
Edit preview	AUTO CUE PLAY	AUTO CUE PLAY EE	37–39
Exit point preview	AUTO EXIT CUE PLAY	AUTO EXIT CUE PLAY EE	40–43
Review mode	AUTO CUE PLAY	AUTO CUE PLAY	48

Table 6-6. Control PWA Jumpers and Test Points



Jumper	Position	Function
J2	A-B	Watchdog timer enabled (normal).
	B-C	Watchdog timer reset disabled for diagnostics.
J4	A-B	Normal operation.
	B-C	Forces continual NO-OP instruction for test of CPU address/control bus.
J5	A-B	Machine address buffer U30 enabled (address bits SBA0–SBA7 to Servo, Reference, Audio, and control panel PWAs–also Serial Remote PWA and Time-Code Reader/Generator PWA).
	Removed	Above PWAs isolated from CPU address/control bus.

(Continued next page)

Table 6-6. Control PWA Jumpers and Test Points (Continued)

Jumper	Position	Function
J6	A-B	Machine address buffer U29 enabled (address bits SBA8–SBA11, SBE, SBR/W, SB CTL PNL SEL, and SB PERIF SEL on system address/control bus).
	Removed	System address/control bus isolated from CPU address/ control bus.
J7	A-B	Remote address buffer U34 enabled (address/control bits RA0, RA1, RA5-RA8, RE, and PAR SEL to Parallel Remote PWA).
	Removed	Remote address/control bus isolated from CPU address/ control bus.
J8	A-B	Priority encoder U44 enabled.
	Removed	Priority encoder U44 disabled.

Test Points	Function
TP1	System reset input to CPU U10 (asserted low).
TP2	Interrupt request (IRQ) input to CPU U10 (asserted low).
TP3	E–1-MHz (enable) clock output of CPU U10.
TP4	R/W–high = read/low = write output of CPU U10.
TP5	A15–address bit 15 output of CPU U10.
TP6	4X Tape tach–gated outputs of flip-flops U60-5 (tachA) and U60-9 (tach B).
TP7	+ 5V–filtered logic supply.
TP8	Tach frame–clock to flip-flop U49-5 which triggers INT 1.
TP9	Tape direction (F/R)–A4 output of IRQ test buffer U46.

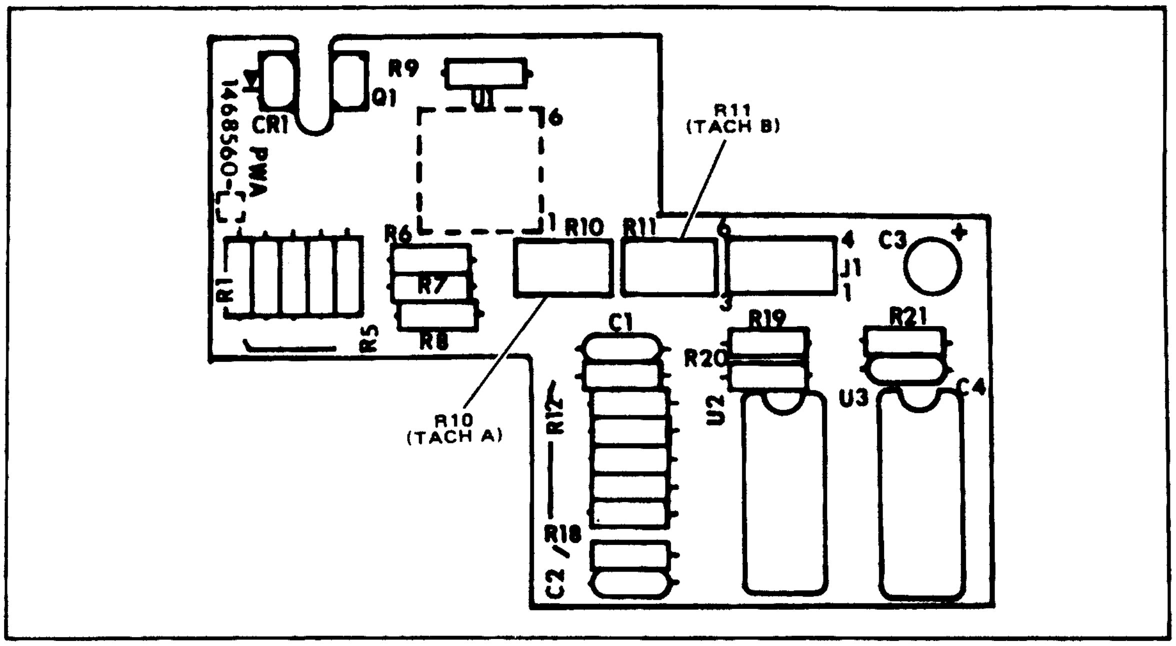


Figure 6-21. Tape Timer Tach/TIP PWA Adjustments

PART II

SECTION 7

TRANSPORT SYSTEM

7-1 GENERAL

This section provides theory of operation information for the transport system. Included are instructions for removing and reinstalling the motor drive amplifier (MDA) assembly, supply and takeup reel motor assemblies, pinch roller arm assembly, and rotating guide assembly, as well as procedures for replacing parts within these assemblies. Alignment of the Reel MDA PWA is explained, and adjustment procedures for the parking brake assembly are given. Transport system performance verification procedures are spelled out in detail.

The following drawings, which are included in the *VPR-80 Parts Lists and Schematics* manual, are referenced in this section.

Drawing	Drawing No.
Transport Assembly	1461000
Motor Drive Amplifier (MDA) Assembly	1450560
Capstan/Scanner MDA PWA	1450586
Capstan/Scanner MDA PWA Schematic	1450588
Reel MDA PWA	1450593
Reel MDA PWA Schematic	1450595

In addition, the following illustration is included at the end of this section.

Figure 7-27. Reel MDA PWA Test Points and Adjustments

7-2 THEORY OF OPERATION

7-3 Capstan/Scanner MDA

Capstan and scanner motors are powered by the Capstan/Scanner MDA PWA, which contains two separate circuits: scanner MDA and capstan MDA. Text that follows describes each circuit separately.

7-4 Capstan MDA

The capstan MDA is a position-servo-controlled analog amplifier controlled by a dc error signal from the capstan servo (see Figure 7-1). Although it is capable of driving the capstan motor in either direction, the capstan motor drives tape forward only at speeds of from 0 to 1.5X normal play speed. The motor stops abruptly when the capstan servo momentarily generates an error signal that causes a reverse drive current to be applied to the motor. This method is unlike that of the scanner MDA, which employs dynamic braking to stop the motor.

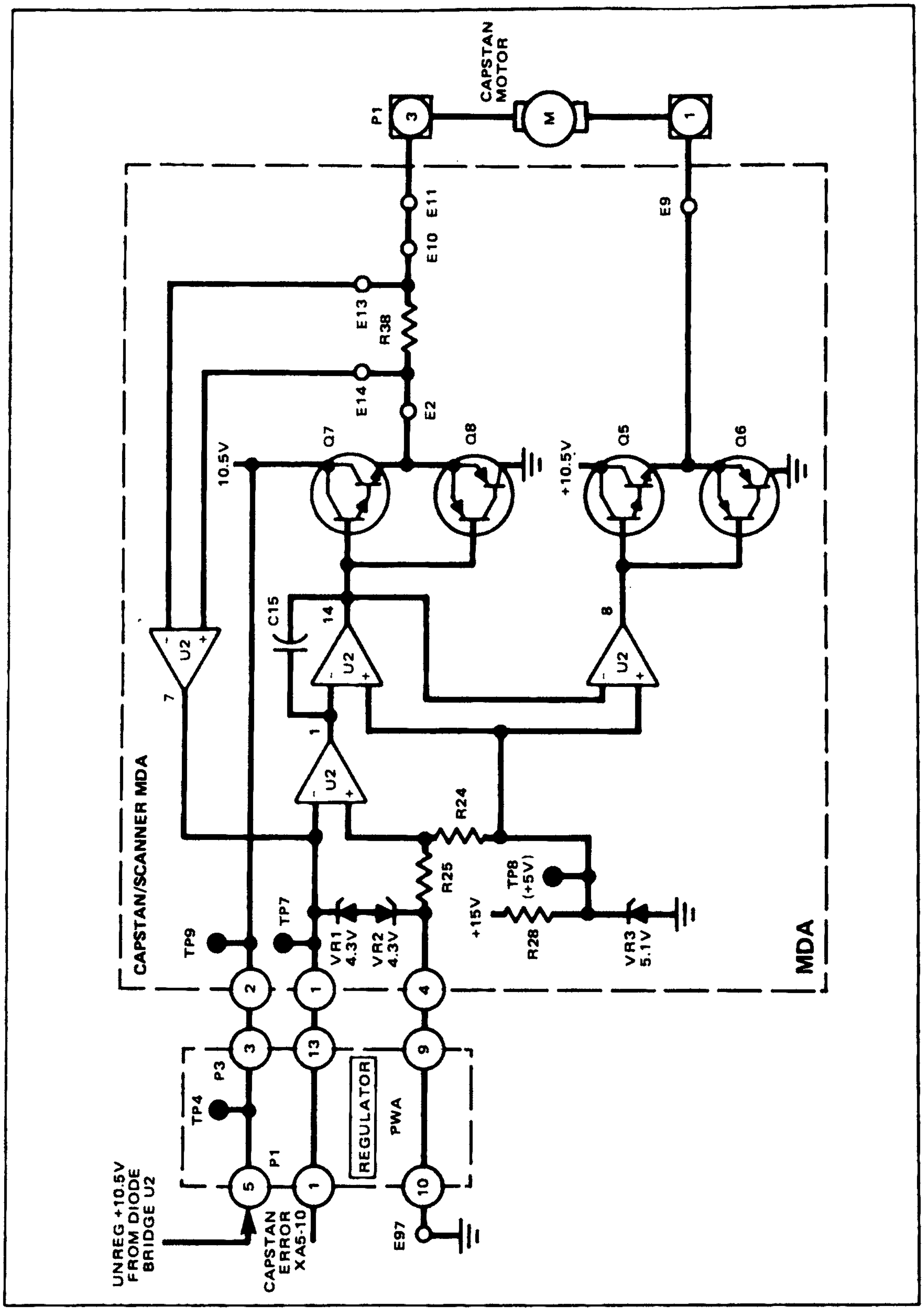


Figure 7-1. Capstan MDA Block Diagram

The unregulated +10.5-Vdc supply powers the capstan motor. The motor is controlled by a dc error signal developed on the Servo PWA, which compares capstan tach signals with a reference frequency. This dc differential capstan error signal is routed through the Voltage Regulator PWA to pins 1 and 4 of the MDA. The dc differential capstan error signal is then converted to single-ended by voltage amplifier U2-1 and applied to a summing point at input pin 13 of summing amplifier U2-14. Here, the capstan error signal is combined with a feedback current sense signal that represents current that is fed through the motor. This feedback signal makes the amplifier independent of individual motor characteristics and any fluctuations in the unregulated voltage supply used to drive the motor. Resistor R38 is in series with the motor, and the voltage drop across R38 (voltage proportional to the current passing through R38) is applied to differential amplifier U2-7 to provide feedback current sense to the summing point.

Darlington pair transistors Q5-Q8 and the motor form a bridge circuit. During operation, two of the transistors are biased on to feed current to the motor in a given direction. Voltage regulator VR3 provides a 5.1-Vdc offset voltage which is applied to differential amplifiers U2-8 and U2-14 to establish a zero-servo-error operating point. The error signal from U2-1 is amplified by U2-14 and applied to Darlington pair transistors Q7 and Q8. In addition, the error signal from U2-14 is inverted by amplifier U2-8 and applied to Darlington pair transistors Q5 and Q6. When the error signal from U2-1 is above nominal offset level, transistors Q5 and Q8 are biased on to complete a circuit path through the motor, driving the motor in one direction. When the error signal from U2-1 is below the nominal offset level, transistors Q6 and Q7 are biased on to supply current to the motor in the opposite direction. These transistors operate linearly to supply the amount of current specified by the error signal at the summing point at input pin 13 of summing amplifier U2-14.

7-5 Scanner MDA

The scanner MDA is a servo-controlled analog power amplifier that is used to drive the scanner dc motor (see Figure 7-2). The motor operates at 3600 rpm (60-Hz line standard) or 3000 rpm (50-Hz line standard). Dynamic braking is employed to slow or stop the motor.

The scanner motor is controlled by a dc error signal developed on the Servo PWA, which compares the scanner tach signal with a reference vertical signal. This dc differential scanner error signal with +5 Vdc and -5 Vdc limits is routed through the Voltage Regulator PWA to pins 8 and 9 of the MDA. The dc differential scanner error signal is then converted to single-ended by voltage amplifier U1-1 and applied to a summing point at the input pin 6 of summing amplifier U1-7. Here, the scanner error signal combines with a feedback current sense signal that represents current fed through the motor. This feedback signal makes the amplifier independent of individual motor characteristics and any fluctuations in the unregulated voltage supply used to drive the motor.

The amplified summed error signal from U1-7 is level-translated by Q1 and Q3 and applied to the base of series pass transistor Q9, which is used to control motor

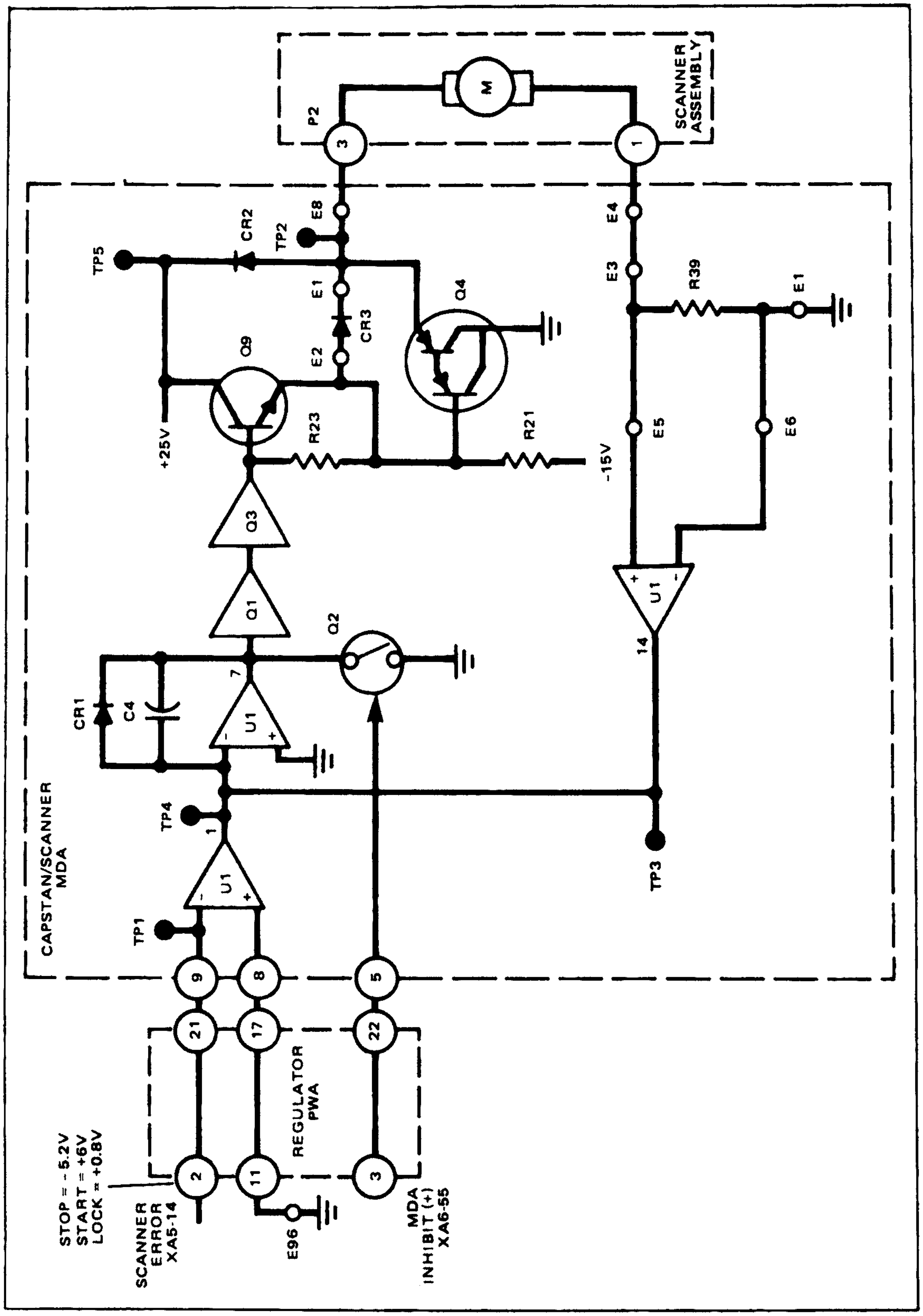


Figure 7-2. Scanner MDA Block Diagram

current. The current path through the motor is from the unregulated +25-Vdc supply, through Q9, diode CR3, the motor, and through current sense resistor R39 to ground. Voltage drop across R39 (voltage proportional to current passing through R39) is applied to amplifier U1-14 to provide feedback current sense to the summing point pin 6 of U1-7.

Dynamic braking is used to stop the motor, and when the motor stops, the active (high) MDA inhibit signal from the Control PWA is applied to transistor Q2. This high turns Q2 on and turns Q1, Q3, and Q9 off. With Q9 off, -15 Vdc is applied to the base of Darlington pair Q4 turning Q4 on. The motor back emf generates a current which is shunted by Q4 and results in motor dynamic braking.

7-6 Reel MDA

The reel MDA is a servo-controlled switching amplifier that drives supply and takeup dc reel motors in either direction at variable speeds (see Figure 7-3). Dynamic braking is used to slow or stop the motors and to control motor torque. Since operation of supply and takeup MDAs is identical, only supply reel MDA circuitry is described here.

Reel motors are powered by the unregulated +25-Vdc supply; servo error control circuitry employs regulated ±15-Vdc supplies. Motor direction and torque are controlled by the supply reel dc error signal developed on the Servo PWA. This dc supply reel error signal is routed through the Voltage Regulator PWA to pins 15 and 16 of the MDA where it is accepted as a dc differential error signal. This dc differential error signal is converted to single-ended by voltage amplifier U6-1 and applied to a summing point at input pin 6 of summing amplifier U6-7. Here, the supply reel error signal is combined with a feedback current sense signal that represents current being fed through the motor. This feedback signal makes the amplifier independent of individual motor characteristics and any fluctuations in unregulated +25 Vdc voltage supply.

Resistor R147 is in series with the motor, and voltage drop across R147 (voltage proportional to the current passing through R147) is applied to differential amplifier U6-16 followed by amplifier U6-10 to provide the feedback current sense to the summing point at pin 6 of summing amplifier U6-7. Voltage follower U5-7 provides a +7.5-Vdc offset voltage (VCC/2) to initially offset the supply reel servo zero-error point to +7.5 Vdc. The servo error signal from U6-7 is applied in parallel to inverting inputs of four error level translators (U3), and the +7.5-Vdc offset level is applied to noninverting inputs. U3 translators individually provide additional offsets of +6.8 Vdc (U3-7), +2.25 Vdc (U3-1), -2.25 Vdc (U3-16), and -6.8 Vdc (U3-10). Offset error signal levels are then fed to the four associated comparators, U1-7, U1-1, U1-16, and U1-10, respectively. The second input to the comparators is a 46.5-kHz triangular waveform generated by amplifiers U5-10/U5-1 and associated components. The triangular waveform is fed to inverting inputs of comparators U1-7 and U1-1, and to noninverting inputs of U1-10 and U1-16, enabling the reel motor to be driven in either direction depending on the polarity of the servo error signal. When the triangular waveform crosses a level established by servo error, comparators change state to provide a logic level to control the on or off state of motor drive FET switches. Thus, comparators convert the analog error signal into a pulse-width-modulated waveform. Waveform symmetry changes as dc error moves up or down to control motor torque.

Output from comparator U1-7 is fed through translators Q2/Q3/Q4 to drive enable gate U2-3. During initial power-up, MDA drive is inhibited until regulated +15 Vdc is present and stabilized, or the MDA inhibit signal (from the Control PWA) entering the PWA at pin 1 goes low. The low from gate U2-3 is fed through buffer emitter followers Q6/Q7 as a low to turn FETs Q5/Q8 on.

Figures 7-4 and 7-5 are waveform diagrams that indicate active motor-drive FETs during a triangular waveform cycle.

Figure 7-4 illustrates a zero current drive condition. During periods 1 through 4, only motor shunt FETs Q14 and/or Q25 are switched on, resulting in dynamic braking if reels are in motion.

Figure 7-5 shows a plus drive motor condition. Note that during a four-period triangular waveform cycle, motor torque is controlled by a combination of current drive and dynamic braking as follows:

Period 1 FETs Q5/Q8 are switched on. The motor drive current path is from the +25-Vdc supply through FETs Q5/Q8, inductor L1, resistor R147, reel motor, inductor L2, and through Q25 to ground to complete the current path.

Period 2 FETs Q5/Q8 are switched off. As the field collapses around inductors L1 and L2, a current in the same direction is maintained. Current path is from ground, through CR2, L1, R147, motor, L2, and Q25 to ground.

Period 3 FETs Q5/Q8 remain off, and FET Q14 switches on and shorts out diode CR2. Current flow through the motor is maintained by the collapsing field around inductors L1 and L2.

Period 4 Current path is the same as described for period 2.

When the motor is slowed down, dc servo error causes period 1 to narrow, resulting in less current drive. It also causes period 3 to widen, resulting in dynamic braking. Circuit operation is as follows:

Period 1 Operation is the same as for period 1 for a plus drive motor condition, except current from the power supply is supplied for a shorter period of time.

Period 2 Same as previous period 2 except that during the latter stage of period 2, energy stored in the inductors dissipates.

Period 3 FET Q14 shunted across the motor results in dynamic braking, and depending on motor speed, motor back emf induces reverse current which is fed back to the power supply.

Period 4 Reverse current continues to flow, depending on energy stored in inductors L1 and L2.

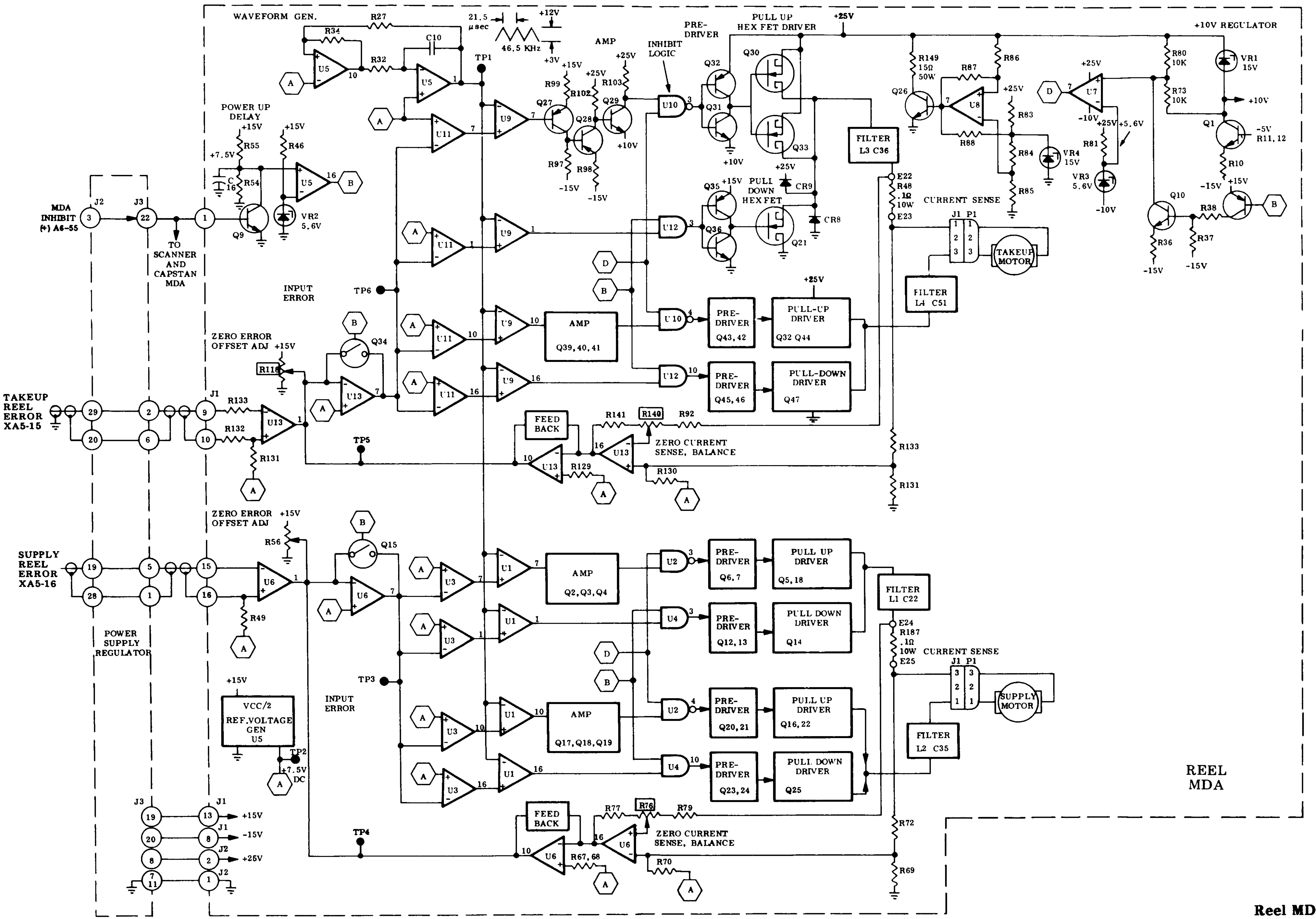


Figure 7-3.
Reel MDA Block Diagram

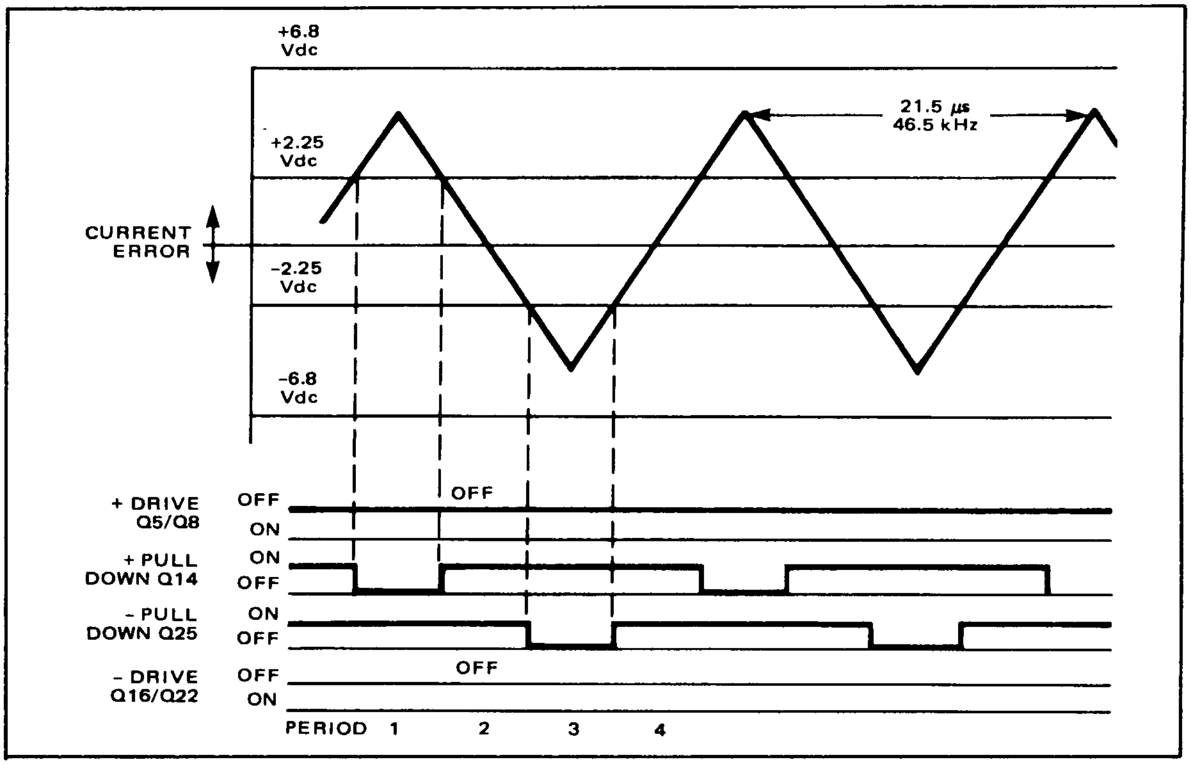


Figure 7-4. Reel MDA, Zero Drive

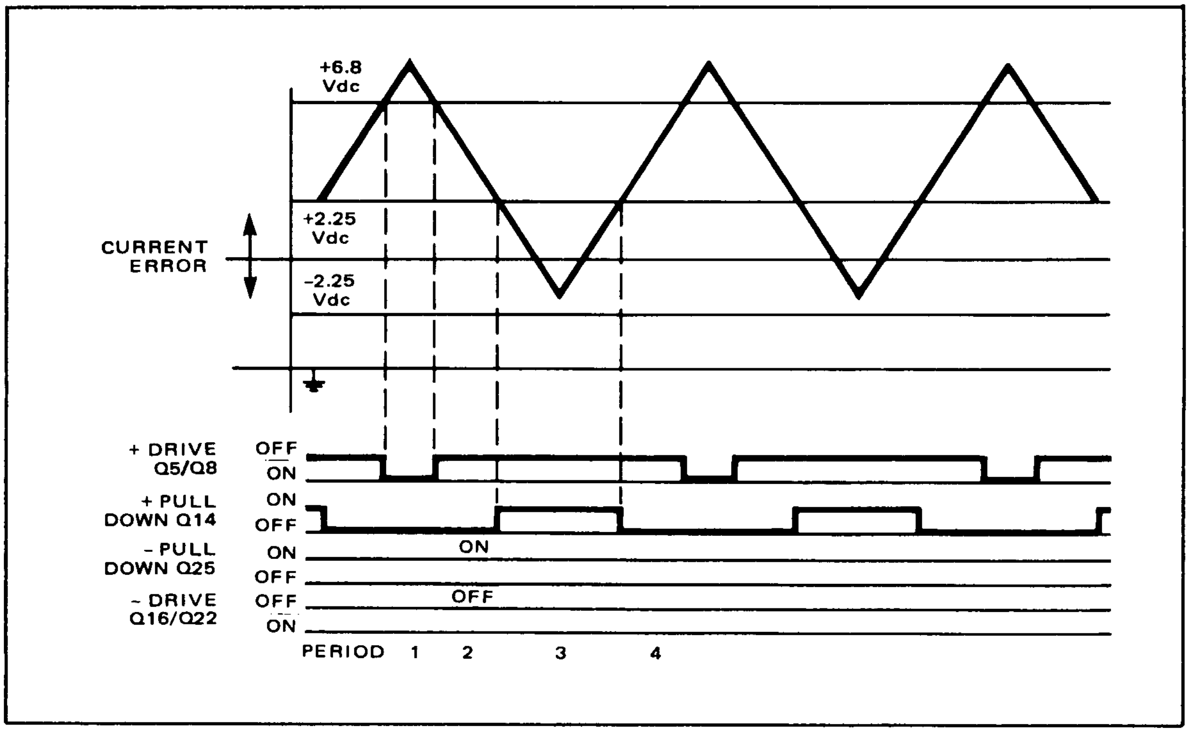


Figure 7-5. Reel MDA, Plus (+) Drive

Components VR4/U8-7/Q26 comprise a safety circuit to protect +25-Vdc power supply filter capacitors. When the motor decelerates, it feeds current back into the power supply +25-Vdc bus. Regulator VR4 establishes a voltage reference for comparator U8-7. If the +25-Vdc bus begins to increase, comparator U8-7 will change state and turn on Q26, placing a 15-ohm, 50-watt resistor across the +25-Vdc bus to bleed power supply capacitors down to +25 Vdc.

7-7 REMOVAL/INSTALLATION

The following paragraphs describe removing and reinstalling the MDA assembly, supply reel motor assembly, takeup reel motor assembly, pinch roller, and rotating guide assembly.

7-8 Motor Drive Amplifier (MDA) Assembly

The MDA assembly, shown in Figure 7-6, houses the Reel MDA PWA and the Capstan/Scanner MDA PWA on a single chassis mounted vertically in the cabinet. The Reel MDA PWA cover is hinged and can be opened (three securing screws) for PWA adjustment. If servicing is required on either PWA, first remove the complete MDA assembly from cabinet, then remove the individual PWA.

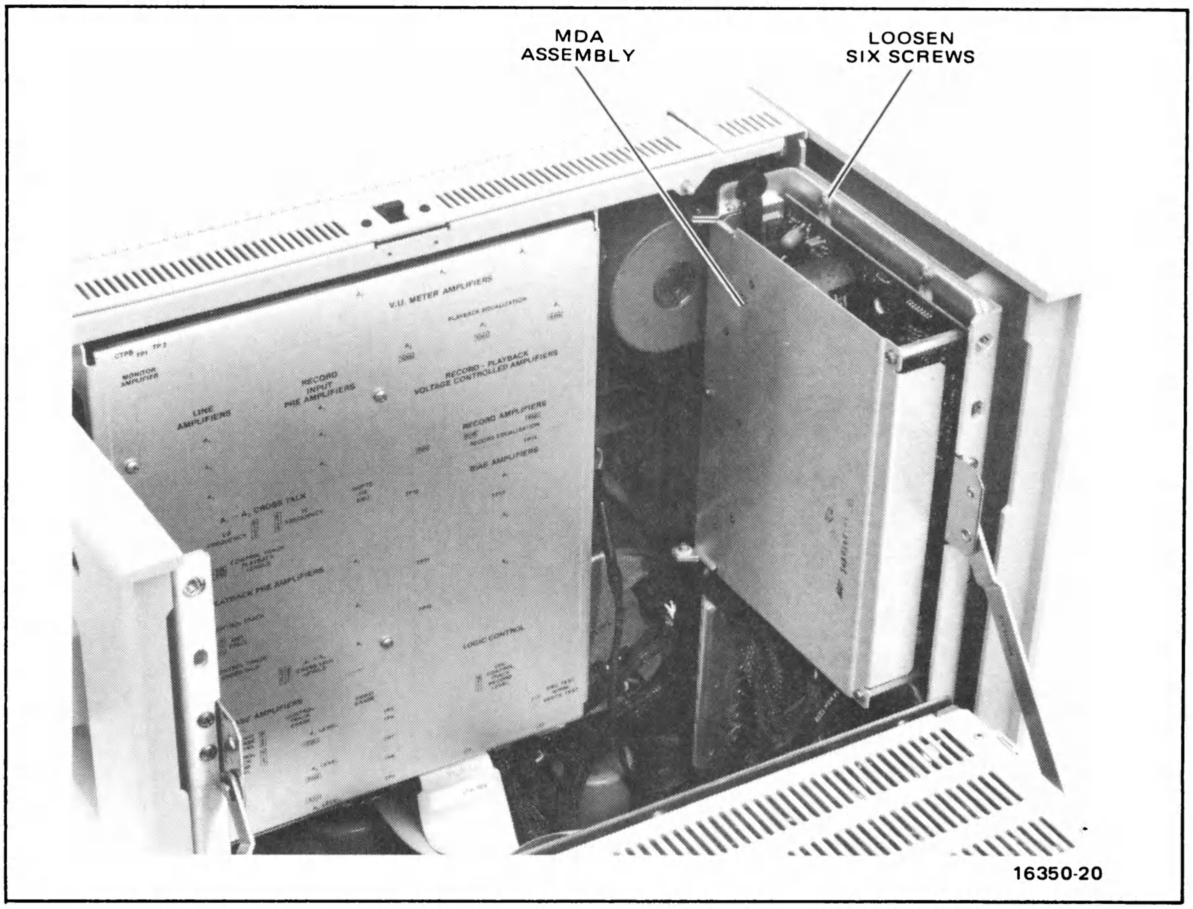


Figure 7-6. Removing Motor Drive Amplifier (MDA) Assembly

To remove the MDA assembly from the VPR-80, proceed as follows:

STEP 1 Loosen two captive screws at rear of cabinet and lower rear door assembly as shown in Part I, Figure 4-3.

STEP 2 Disconnect five MDA assembly connectors. These connectors are labeled PS P3, TU P1, SUP P1, P1 SCANNER, and P1 CAPSTAN.

STEP 3 See Figures 7-6 and 7-7. From inside the cabinet, loosen the six no. 8 cross-recessed screws that secure MDA chassis to cabinet side panel.

STEP 4 Lift MDA chassis up about 0.5 in. (1.27 cm) and detach slotted mounting holes on MDA chassis from mounting screws loosened in step 3. Then remove MDA chassis from cabinet.

STEP 5 Reinstall MDA chassis into cabinet.

7-9 Capstan/Scanner MDA

The capstan/scanner MDA is mounted on the MDA assembly chassis. To remove the capstan/scanner MDA from the MDA chassis, proceed as follows:

STEP 1 Remove MDA assembly from cabinet as described in paragraph 7-8.

STEP 2 See Figure 7-8. Disconnect connector CAP SCAN P1 from Capstan/Scanner MDA PWA.

STEP 3 Remove the three no. 8 screws and hardware that secure the Q9 heat sink to the MDA chassis.

STEP 4 Remove the five no. 8 screws and hardware that secure the Q3-Q8 heat sink plate to the MDA chassis and remove PWA and its heat sink from the MDA chassis.

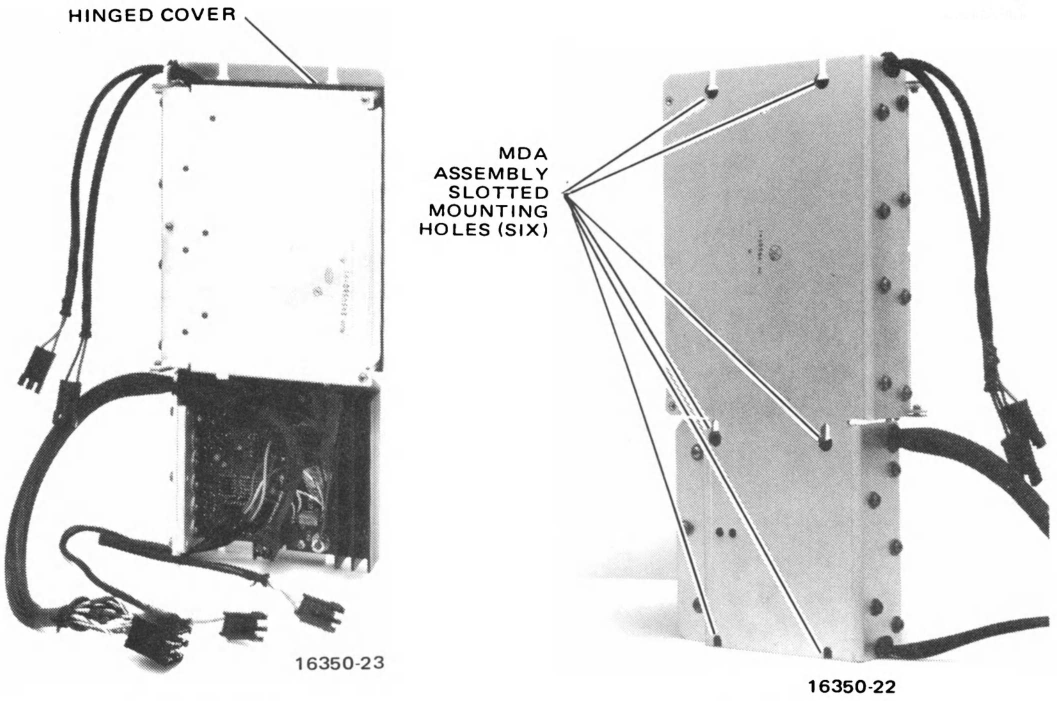
CAUTION

TO PREVENT DAMAGE TO TRANSISTORS Q3-Q8, IT IS ESSENTIAL THAT FIVE SCREWS SECURING THE Q3-Q8 HEAT SINK PLATE BE TIGHTENED BEFORE TIGHTENING THREE SCREWS SECURING THE Q9 HEAT SINK.

STEP 5 Reinstall PWA onto the MDA chassis by first securing the Q3-Q8 heat sink plate (five screws and washers) followed by securing the Q9 heat sink (three screws and washers).

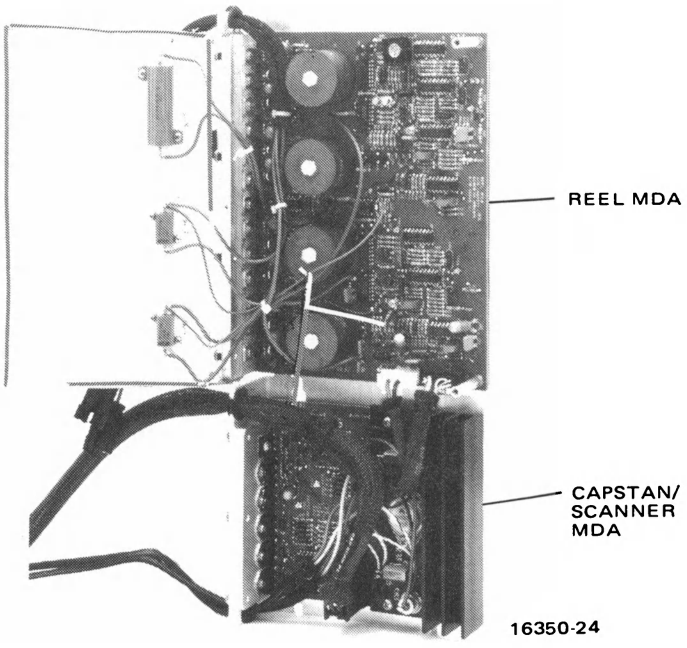
STEP 6 Reconnect connector CAP SCAN P1 to the PWA.

STEP 7 Reinstall MDA assembly into cabinet.



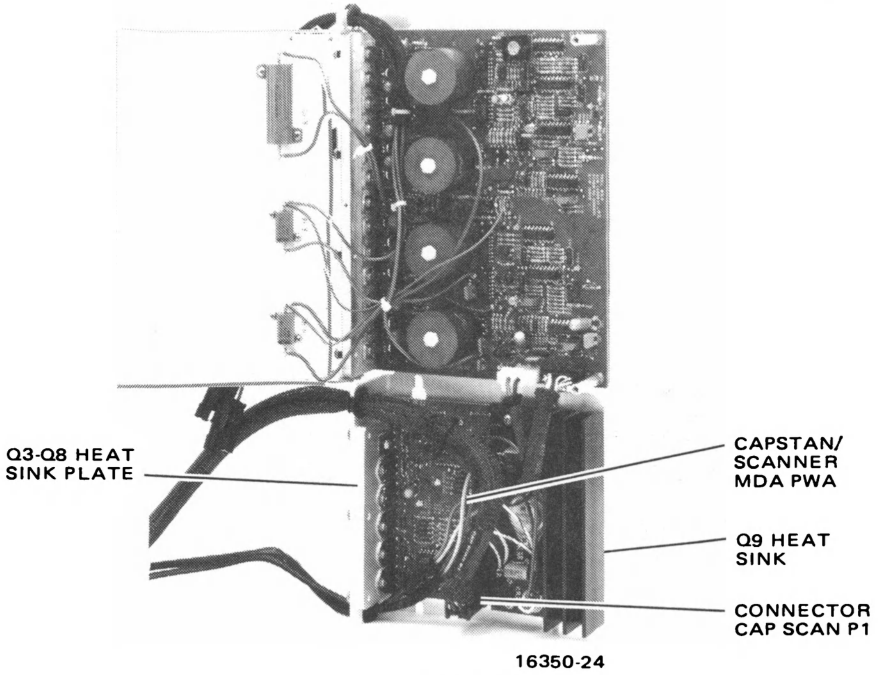
FRONT VIEW

REAR VIEW

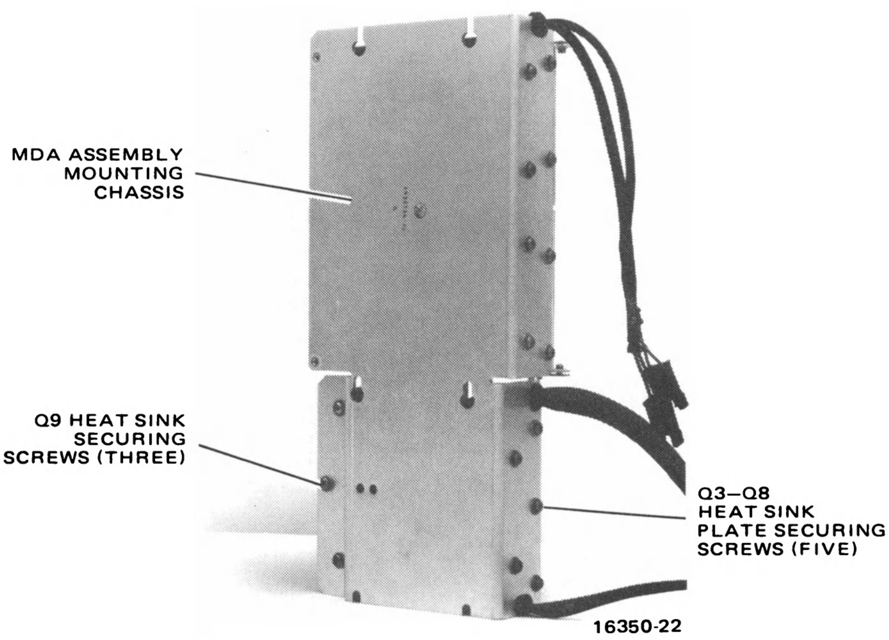


FRONT VIEW WITH REEL MDA COVER OPEN

Figure 7-7. Motor Drive Amplifier (MDA) Assembly Components



FRONT VIEW


MDA ASSEMBLY MOUNTING CHASSIS
Q9 HEAT SINK SECURING SCREWS (THREE)
Q3—Q8 HEAT SINK PLATE SECURING SCREWS (FIVE)
16350-22

REAR VIEW

Figure 7-8. Removing Capstan/Scanner MDA

7-10 Reel MDA

The reel MDA is mounted on the MDA assembly chassis. To remove reel MDA from MDA chassis proceed as follows:

STEP 1 Remove MDA assembly from cabinet as described in paragraph 7-8.

STEP 2 See Figure 7-9. Disconnect connectors labeled REEL MDA P1 and REEL MDA P2 from the Reel MDA PWA.

STEP 3 Remove eight no. 8 cross-recessed screws and hardware that secure heat sink to MDA chassis.

STEP 4 Remove three cross-recessed screws and hardware that secure hinged cover and open cover.

STEP 5 Unscrew two 1.5-in. (3.81-cm) long spacers used to secure hinged cover.

STEP 6 Remove PWA from chassis. If necessary, unsolder eight wires that connect to resistors mounted on hinged cover/heat sink.

CAUTION

TO PREVENT DAMAGE TO 13 TRANSISTORS MOUNTED ON THE HEAT SINK, IT IS ESSENTIAL THAT THE EIGHT SCREWS REMOVED IN STEP 3 BE TIGHTENED BEFORE REINSTALLING SPACERS REMOVED IN STEP 5.

STEP 7 Reinstall PWA onto MDA chassis by first securing heat sink removed in step 3 (eight screws and washers), and then reinstalling two spacers removed in step 5.

STEP 8 Close hinged cover and secure with screws and hardware removed in step 4.

STEP 9 Reinstall MDA chassis into cabinet.

7-11 Supply Reel Motor Assembly

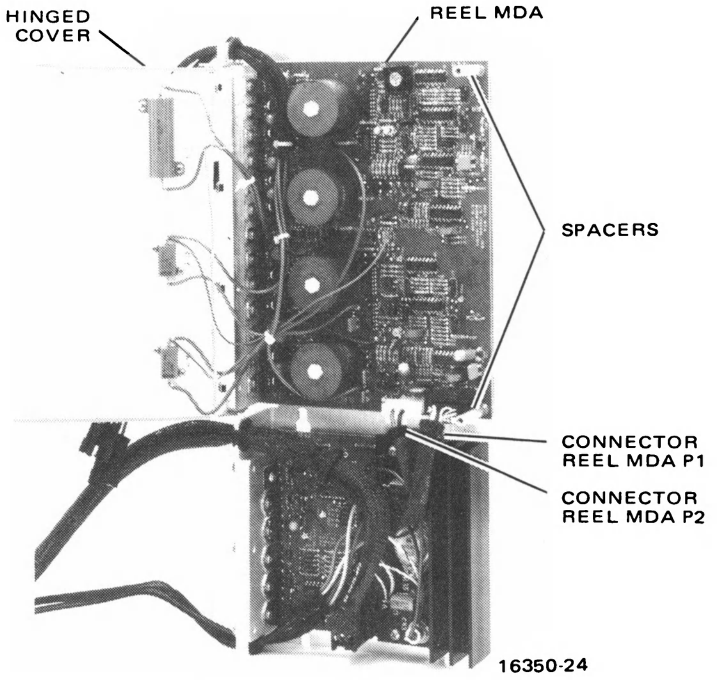
The supply reel motor assembly is removed and reinstalled as follows:

STEP 1 Remove transport trim as described in paragraph 4-12, Part I.

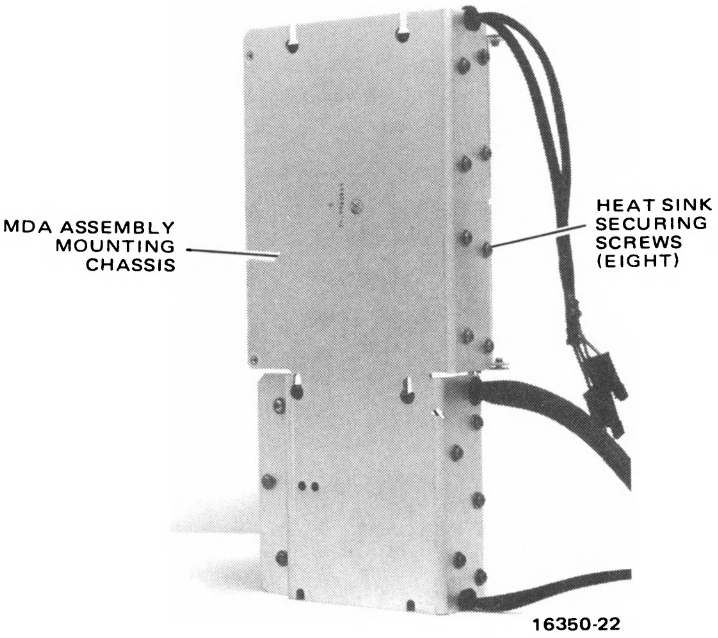
STEP 2 Loosen two captive screws at rear of cabinet and lower rear door assembly as shown in Figure 4-3, Part I.

STEP 3 Disengage four quarter-turn captive screws securing Audio PWA assembly (includes shield).

STEP 4 Detach Audio PWA assembly and lay it back to gain access to rear of transport as shown in Figure 7-10.



FRONT VIEW


MDA ASSEMBLY MOUNTING CHASSIS
HEAT SINK SECURING SCREWS (EIGHT)
16350-22

REAR VIEW

Figure 7-9. Removing Reel MDA

STEP 5 Disconnect supply reel motor assembly connector J1, and detach MDA supply reel connector SUP P1 from vertical connector mounting plate. See Figure 7-10.

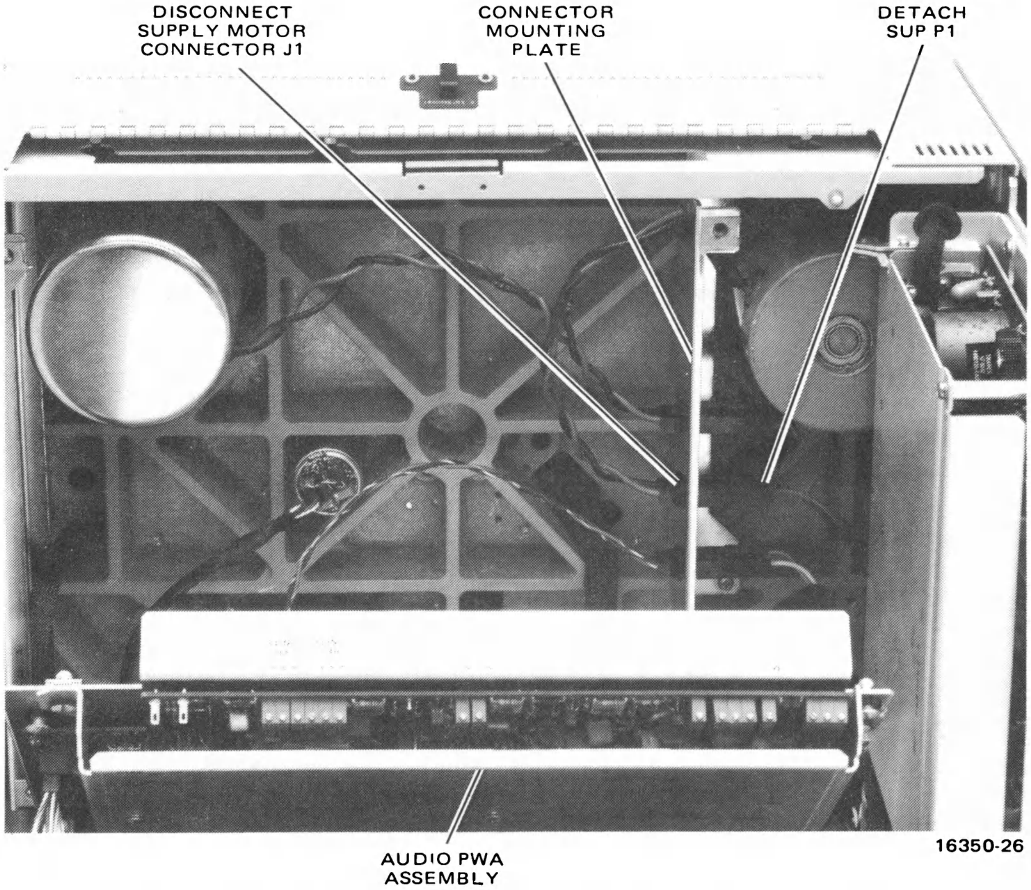


Figure 7-10. Removing Supply Reel Motor Assembly

STEP 6 At the front of the transport, detach connector SUP P2 from supply reel tach connector J2. See Figure 7-11.

STEP 7 Remove 6-32 cross-recessed screw and washer from takeup motor solenoid link.

STEP 8 Disconnect spring at location shown in Figure 7-11.

CAUTION

WHEN REMOVING SUPPLY REEL MOTOR ASSEMBLY FROM TRANSPORT, NOTE THERE IS A LOOSE LOCATOR BUSHING UNDER TWO RIGHT-HAND SCREWS THAT SECURE MOTOR MOUNTING PLATE TO TRANSPORT CASTING. DO NOT ALLOW

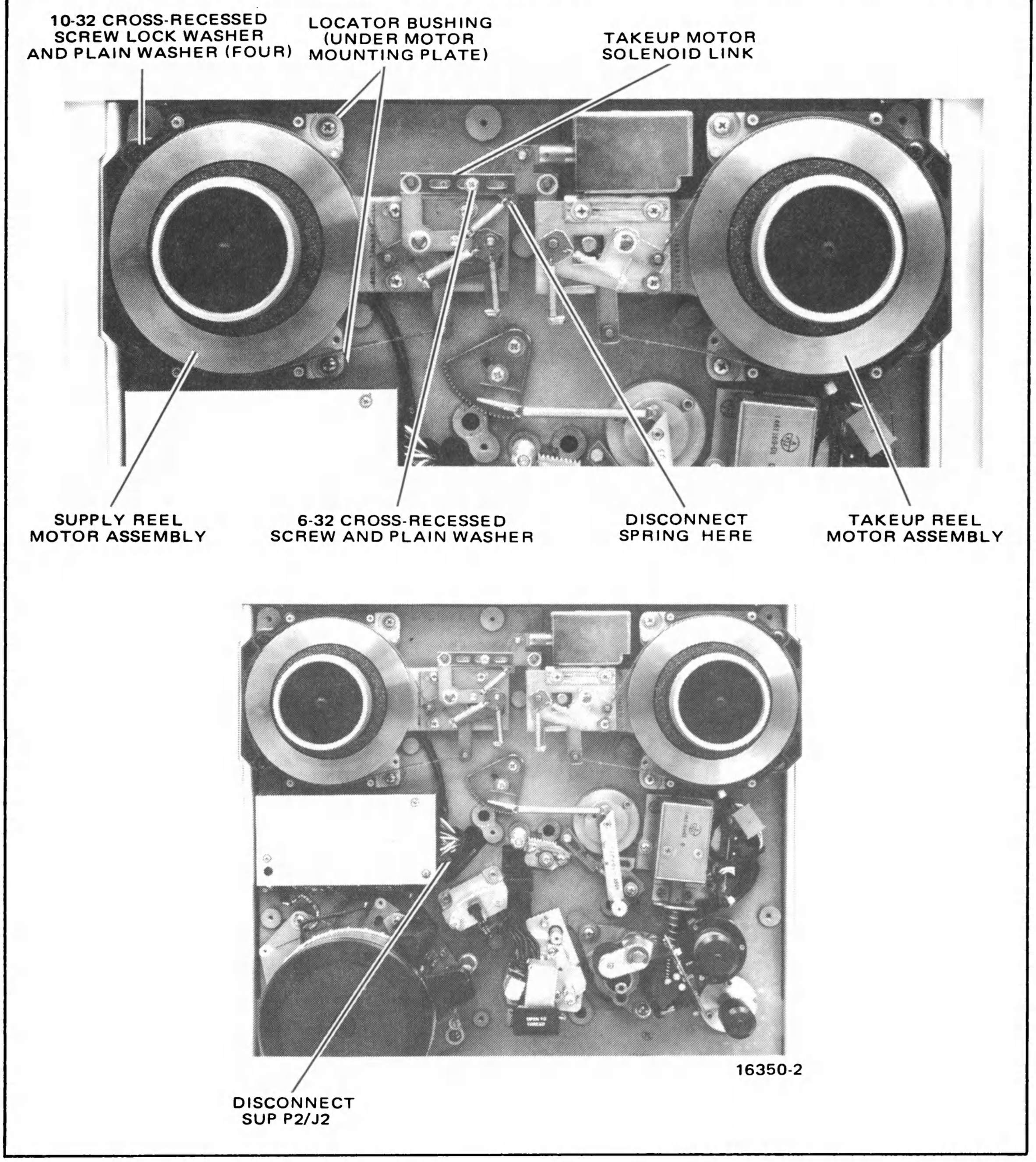

10-32 CROSS-RECESSED SCREW LOCK WASHER AND PLAIN WASHER (FOUR)
LOCATOR BUSHING (UNDER MOTOR MOUNTING PLATE)
TAKEUP MOTOR SOLENOID LINK
SUPPLY REEL MOTOR ASSEMBLY
6-32 CROSS-RECESSED SCREW AND PLAIN WASHER
DISCONNECT SPRING HERE
TAKEUP REEL MOTOR ASSEMBLY
16350-2
DISCONNECT SUP P2/J2

Figure 7-11. Removing Supply Reel Motor

LOCATOR BUSHINGS TO FALL BEHIND SHIELD COVERING RECORD AMPLIFIER AND EDIT ERASE PWA, OR (MORE LIKELY) TO FALL ON THE FLOOR AND BECOME LOST.

STEP 9 Remove four cross-recessed screws, lock washers, and plain washers that secure motor mounting plate to transport casting.

STEP 10 Remove supply motor assembly and the two right-hand locator bushings from front of transport.

STEP 11 Reinstall supply reel motor assembly and locator bushings.

7-12 Takeup Reel Motor Assembly

The takeup reel motor assembly is removed and reinstalled as follows:

STEP 1 Remove transport trim as described in paragraph 4-12, Part I.

STEP 2 Loosen two captive screws at rear of cabinet and lower rear door assembly as shown in Figure 4-3, Part I.

STEP 3 Disengage four quarter-turn captive screws securing Audio PWA assembly (includes shield).

STEP 4 Detach Audio PWA assembly and lay it back to gain access to rear of transport as shown in Figure 7-12.

STEP 5 Disconnect takeup reel motor assembly connector J1, and detach MDA takeup reel connector TU P1 from vertical connector mounting plate. See Figure 7-12.

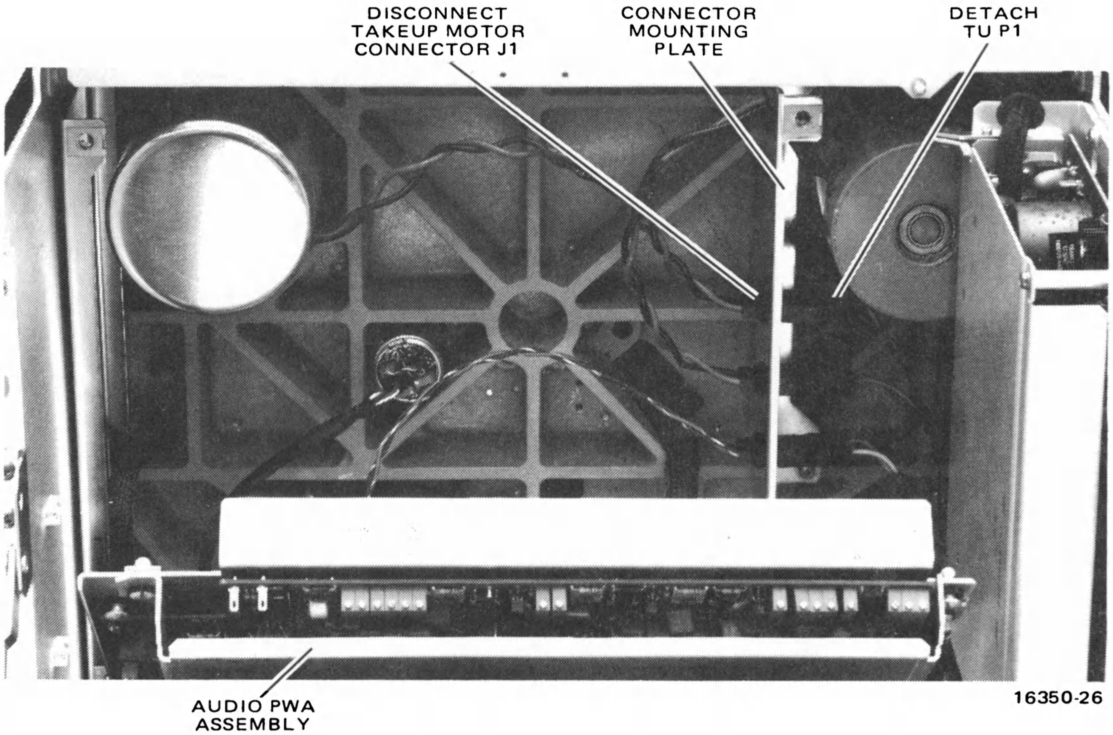


Figure 7-12. Removing Takeup Reel Motor Assembly

STEP 6 At the front of transport, disconnect takeup reel-tach connector J2 from connector TU-P2. See Figure 7-13. Also disconnect parking brake solenoid connector P3 from Solenoid Distribution PWA. See Figure 7-13.

STEP 7 Remove 6-32 cross-recessed screw and washer from takeup motor solenoid link.

STEP 8 Disconnect spring at location shown in Figure 7-13.

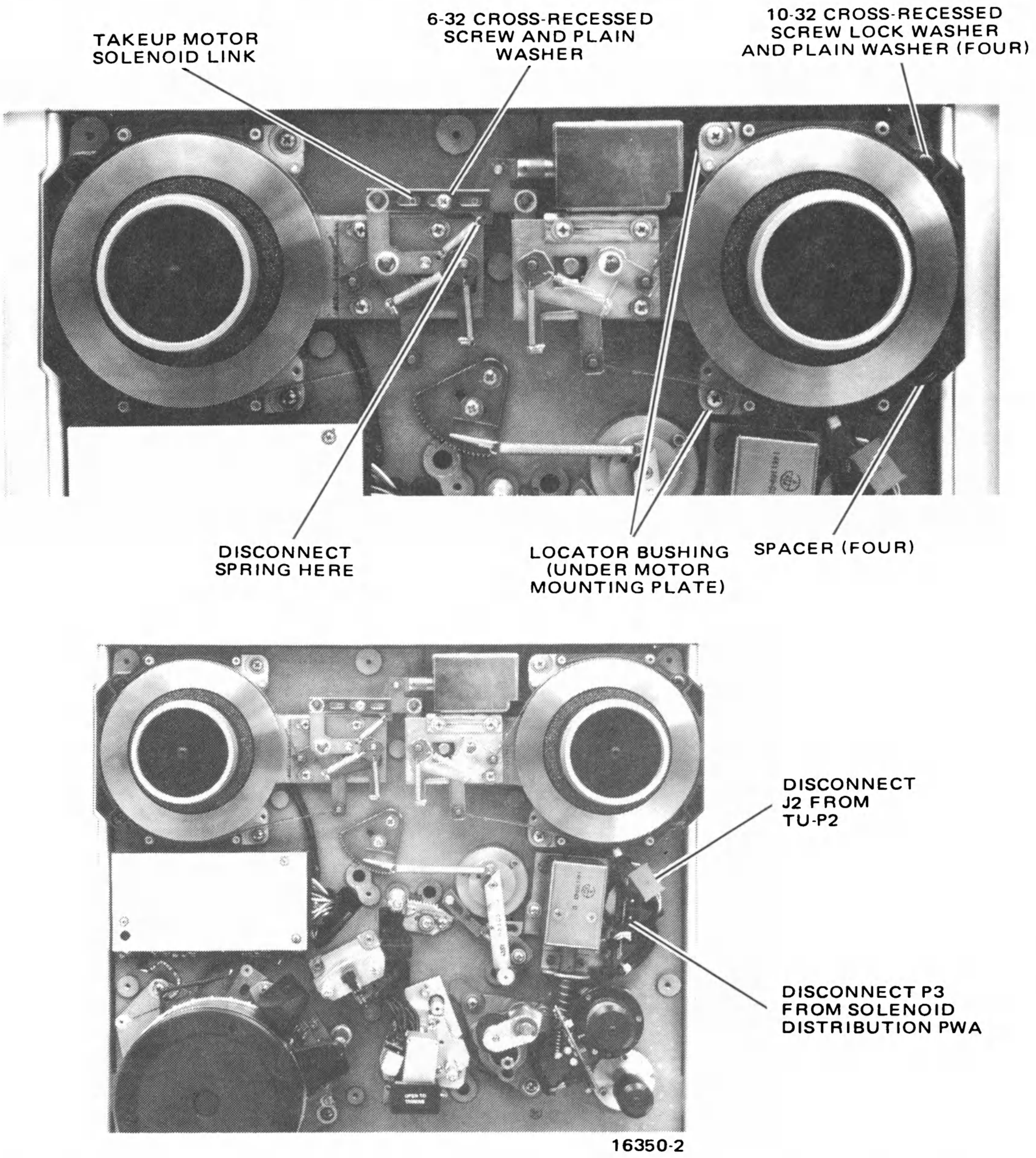

TAKEUP MOTOR SOLENOID LINK
6-32 CROSS-RECESSED SCREW AND PLAIN WASHER
10-32 CROSS-RECESSED SCREW LOCK WASHER AND PLAIN WASHER (FOUR)
DISCONNECT SPRING HERE
LOCATOR BUSHING (UNDER MOTOR MOUNTING PLATE)
SPACER (FOUR)
DISCONNECT J2 FROM TU-P2
DISCONNECT P3 FROM SOLENOID DISTRIBUTION PWA
16350-2

Figure 7-13. Removing Takeup Reel Motor

CAUTION

WHEN REMOVING TAKEUP REEL MOTOR ASSEMBLY FROM TRANSPORT, NOTE THERE IS A LOOSE LOCATOR BUSHING UNDER TWO LEFT-HAND SCREWS THAT SECURE THE MOTOR MOUNTING PLATE TO TRANSPORT CASTING. ALSO THERE ARE FOUR SPACERS LOCATED BETWEEN THE TAKEUP MOTOR MOUNTING PLATE ASSEMBLY AND TRANSPORT CASTING. DO NOT ALLOW BUSHINGS OR SPACERS TO FALL INTO TRANSPORT COMPONENTS, OR (MORE LIKELY) TO FALL ON THE FLOOR AND BECOME LOST.

STEP 9 Remove four 10-32 cross-recessed screws, lock washers, and plain washers that secure motor mounting plate to transport casting.

STEP 10 Reinstall takeup reel motor assembly (including locator bushings and spacers).

7-13 Pinch Roller Arm Assembly

The pinch roller arm assembly is removed and reinstalled as follows:

STEP 1 Remove connectors P1, P2, and P3 from the Solenoid Distribution PWA. See Figure 7-14.

STEP 2 Use a 3/8-in. spin tight tool to remove no. 10 locknut that secures the compression spring to the pinch roller solenoid shaft. Remove compression spring, but leave secondary spring in place on shaft.

STEP 3 Remove three 8-32 cross-recessed screws and hardware that secure the solenoid to transport. Disengage solenoid shaft from pinch roller arm assembly, and remove solenoid and Solenoid Distribution PWA. Do not lose secondary spring on solenoid shaft.

STEP 4 Remove retaining ring and shim washer that secure pinch roller arm assembly. Slide arm up from pinch roller pivot shaft.

STEP 5 Clean pivot shaft and arm assembly bore with isopropyl alcohol. Then lightly coat pivot shaft with dry-film lubricant (Ampex Part No. 087-581).

STEP 6 Reinstall pinch roller arm assembly, solenoid, and PWA.

CAUTION

WHEN CLEANING PINCH ROLLER, MAKE SURE NO ISOPROPYL ALCOHOL CONTACTS OIL-IMPREGNATED POROUS BRONZE BEARING.

STEP 7 Clean pinch roller with isopropyl alcohol.

STEP 8 Adjust pinch roller pressure as outlined in paragraph 4-22, Part I.

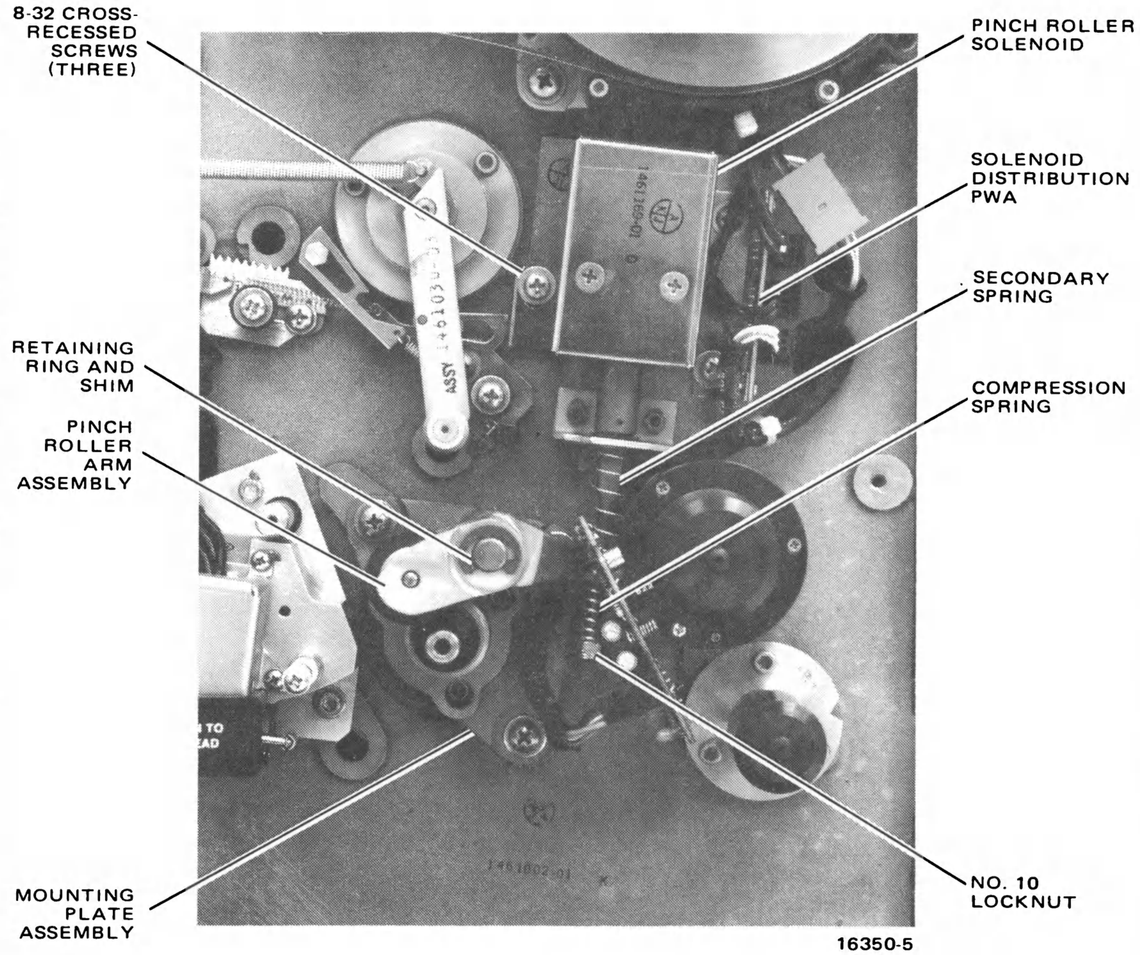


Figure 7-14. Removing Pinch Roller Arm Assembly

7-14 Rotating Guide Assembly

The rotating guide assembly is removed and reinstalled as follows:

STEP 1 Remove transport trim as described in paragraph 4-12, Part I.

STEP 2 Using a 9/64-in. hex-drive wrench, remove three hex-recessed screws and lock washers shown in Figure 7-15. Remove rotating guide assembly from the front of transport.

STEP 3 When replacing guide assembly, note location of factory-adjusted perpendicularity adjusting screw on guide base. Position guide on transport so that adjusting screw faces upward (toward timer idler assembly). Using screws and lock washers removed in step 2, secure guide to transport. Torque screws to 12 in.-lb (1.34 Newton-meters).

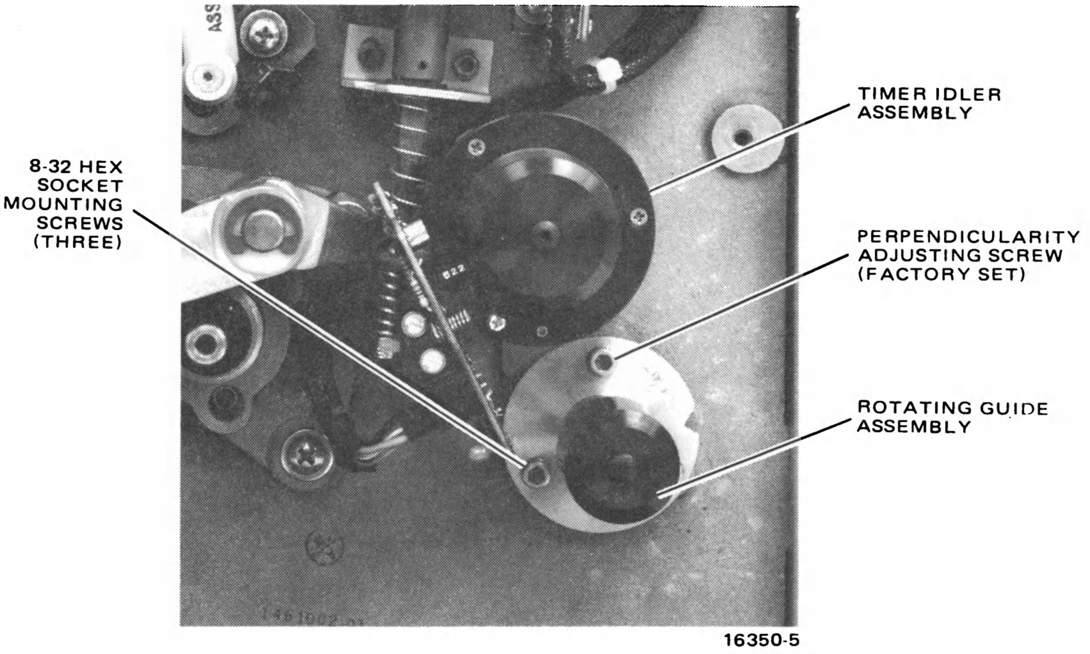

8-32 HEX SOCKET MOUNTING SCREWS (THREE)
TIMER IDLER ASSEMBLY
PERPENDICULARITY ADJUSTING SCREW (FACTORY SET)
ROTATING GUIDE ASSEMBLY
16350-5

Figure 7-15. Removing Rotating Guide Assembly

Note

Overtorquing screws can affect guide perpendicularity, resulting in tape-guiding problems.

STEP 4 Reinstall transport trim.

7-15 PART REPLACEMENT

Instructions for replacing components on the supply reel motor assembly, takeup reel motor assembly, pinch roller arm assembly, and rotating guide assembly are given in the following paragraphs.

7-16 Supply Reel Motor Assembly

The following paragraphs cover parts replacement on the supply reel motor assembly. Instructions are given for replacing supply reel motor, parking brake band assembly, and motor brushes.

7-17 Supply Reel Motor

Note

If factory-assembled reel motor assembly with turntable (Ampex Part No. 1463290 or 1463318) is to be used for motor replacement instead of a bare motor, proceed to paragraph 7-18.

Replacing the supply motor requires removing supply reel motor assembly from the transport, and separating the turntable from the motor. Proceed as follows:

STEP 1 Remove supply reel motor assembly from transport as described in paragraph 7-11.

STEP 2 Remove hex-drive screw that secures retainer to reel knob. Remove retainer (circular plate) and nylon washer under retainer. See Figure 7-16.

STEP 3 Use a 3/32-in. hex-drive wrench to loosen three setscrews that secure turntable assembly to motor shaft. Access to screws is provided by a notch in the motor mounting plate. See section A-A in Figure 7-16.

STEP 4 Relax brake-band tension by pressing low-tension arm assembly toward turntable. See Figure 7-17. Then pull turntable assembly straight up to remove from motor shaft. If turntable assembly is not easily removed, force off shaft by turning turntable elevation adjustment setscrew clockwise. Access to elevation setscrew is through hole vacated by retainer screw removed in step 2. Use a 3/32-in. hex-drive wrench to turn screw clockwise to raise turntable. After removal, turn setscrew counterclockwise approximately an equal amount of turns or until stop is reached. When turntable assembly is removed, be sure to save small loose brass reel motor disk on the end of the motor shaft.

CAUTION

IF ELEVATION ADJUSTMENT SETSCREW SHOULD COME OUT OF TURNTABLE IT MUST BE REINSTALLED FROM BOTTOM OF TURNTABLE; IT WILL JAM IF INSTALLED FROM THE TOP.

STEP 5 There are four 10-32 cross-recessed screws and hardware that secure the reel drive motor to motor mounting plate. Two of these screws also secure the Reel Tachometer PWA to motor mounting plate. Remove four screws and hardware, and separate motor mounting plate from motor. See detail B in Figure 7-16.

Attach new motor to motor mounting plate as follows:

STEP 6 Note orientation of motor leads with respect to motor mounting plate (Figure 7-16). Loosely install two 10-32 screws, plain washers, and lock washers shown on left-hand side of Figure 7-16.

STEP 7 Refer to detail B in Figure 7-16 and install parts in sequence as follows: two nonmetalic washers, Reel Tachometer PWA, two plain washers, two lock washers, and two 10-32 screws (install loosely). See Figure 7-17. Before tightening PWA securing screws, set distance between edge of motor shaft and center point of the two optical coupler slots to 0.75 in. (19.1 mm).

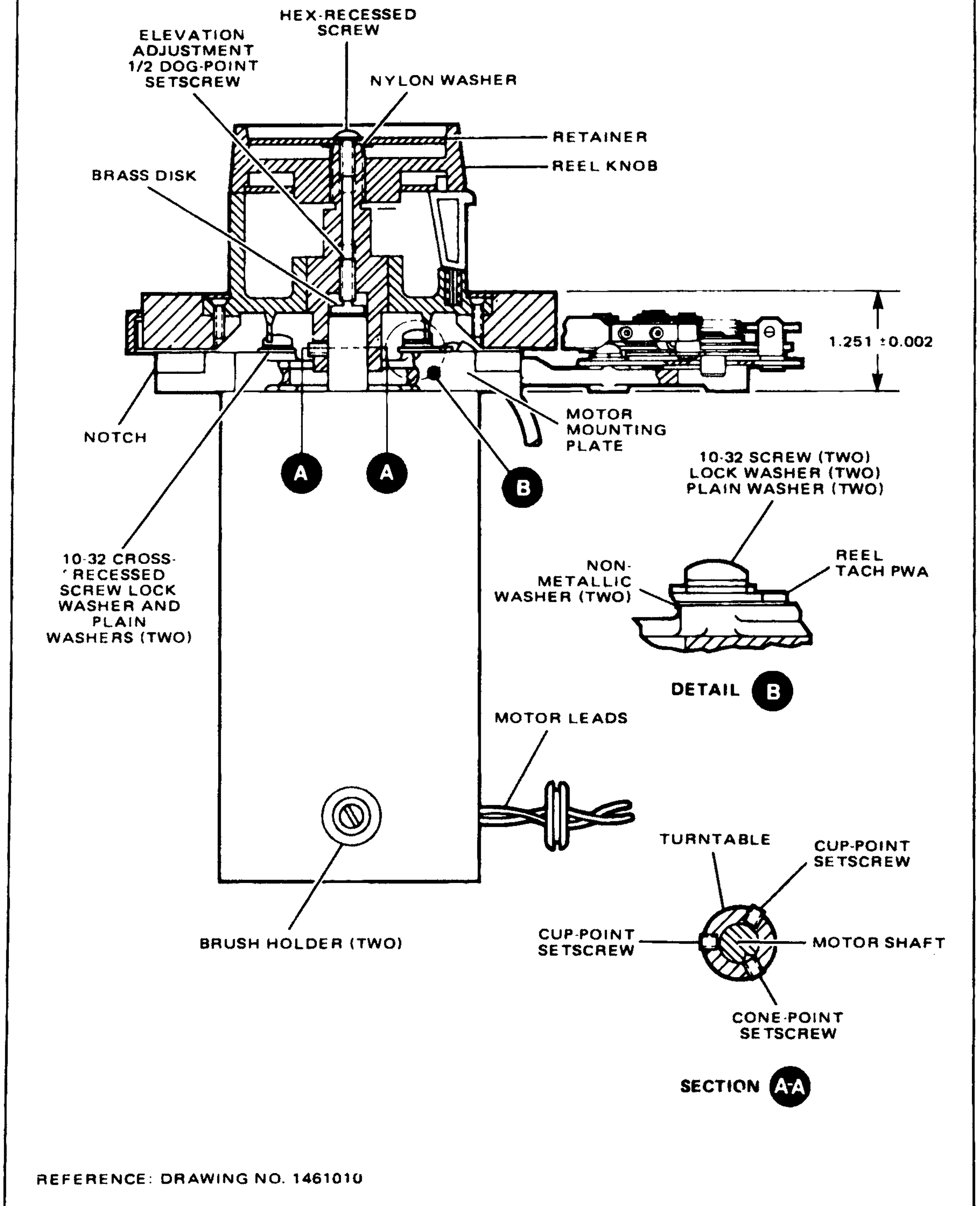


Figure 7-16. Replacing Supply Reel Motor

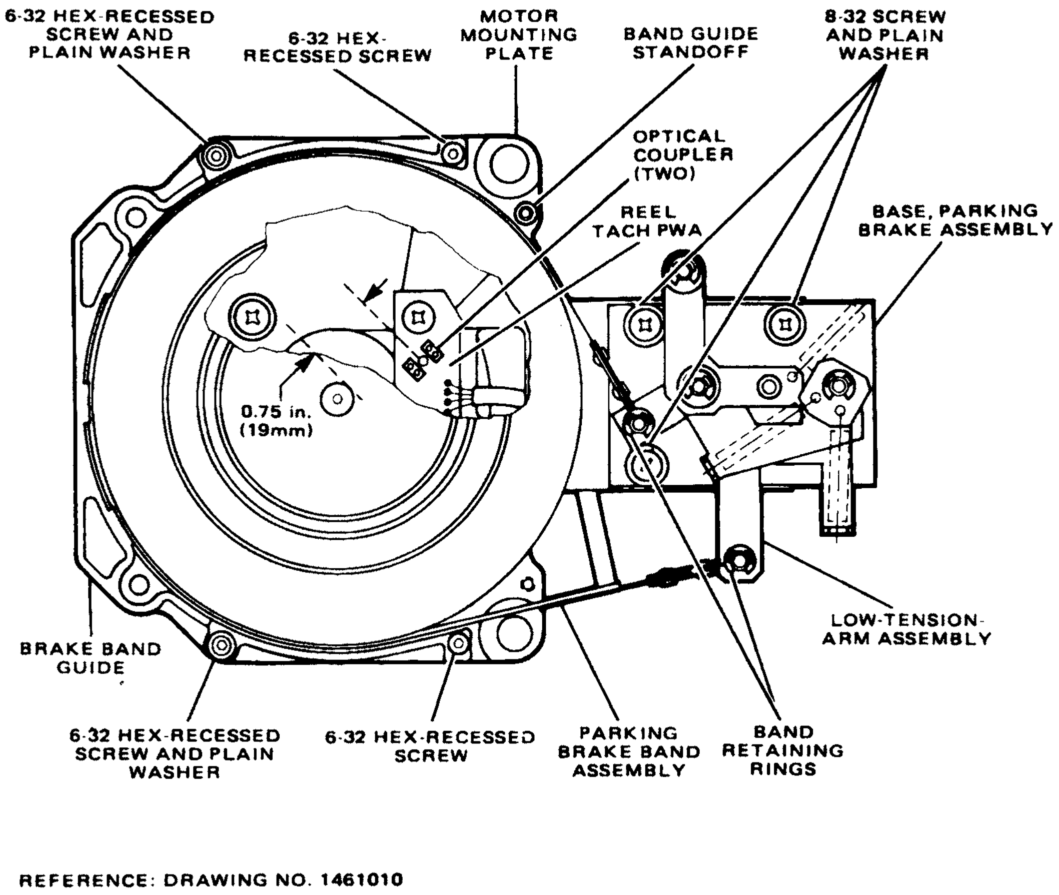


Figure 7-17. Supply Reel Motor Assembly (with Turntable) Components

STEP 8 Ensure that plain washers are not contacting traces on PWA, and then torque four screws installed in steps 6 and 7 to 13.0 in.-lb. (1.46 Newton-meters).

STEP 9 Place brass disk removed in step 4 on top of motor shaft.

STEP 10 See section A-A in Figure 7-16. Install turntable assembly on motor shaft as follows: Position motor shaft so that V-groove in shaft is visible through notch in motor mounting plate. Position turntable assembly so that cone point setscrew slides into motor shaft V-groove.

STEP 11 Before tightening setscrews, set turntable height to 1.251 in. (31.78 mm) as follows:

Note

The cork pad on the turntable is soft and does not provide a suitable surface for measuring turntable height. For this reason, a metal hub from a tape reel is placed on the turntable to compress the turntable cork pad and also serve as a reference measuring surface.

a. Remove metal hub from a tape reel.

b. Use a vernier caliper to measure hub height at its thickest point. Record measurement.

c. Place hub on turntable and loosely tighten reel knob.

d. With turntable pressed down so elevation adjustment setscrew is firm against brass reel motor disk, use vernier caliper to measure distance between bottom surface of motor mount plate and top surface of hub. Then tighten reel knob to compress cork pad a minimum of 0.005 in., or 5 mils (5 mils = 0.1270 mm) as measured by vernier caliper. Record reading.

e. Subtract hub height from value recorded in step 11d. The resulting difference should be 1.251 in. ±0.002 in. (31.78 mm ±0.0508 mm). Adjust turntable height adjustment screw as required to obtain correct height (turning screw clockwise increases height).

STEP 12 After correct turntable height is established, tighten motor shaft setscrews to 13.0 in.-lb (1.46 Newton-meters) in the following sequence. First tighten the cone point setscrew (located in motor shaft V-groove), and then tighten the two cup-point setscrews.

STEP 13 Recheck turntable height. If necessary, loosen motor shaft setscrews and reset turntable height.

STEP 14 Reinstall nylon washer, retainer, and hex-recessed head screw removed in step 2.

STEP 15 Reinstall supply reel motor assembly into transport.

STEP 16 Adjust parking brake as described in paragraph 7-34.

7-18 Supply Reel Motor with Turntable

Note

If a bare supply reel motor is to be used for replacement instead of a factory-assembled reel motor with turntable, refer to instructions given in paragraph 7-17.

Use the following procedure to replace the supply reel motor with factory-assembled reel motor with turntable (Ampex Part No. 1463290 or 1463318). Proceed as follows:

STEP 1 Remove supply reel motor assembly from transport as described in paragraph 7-11.

STEP 2 Refer to Figure 7-17 and disassemble old supply reel motor assembly as follows:

a. Remove base parking brake plate assembly (includes brake band) from motor mounting plate by removing three 8-32 cross-recessed screws (with captive lockwasher) and plain washers.

b. Remove brake band guide from motor mounting plate by removing two 6-32 hex-recessed screws with plain washer and two 6-32 hex-recessed screws (no washers).

c. Unscrew band guide standoff from motor mounting plate.

STEP 3 Transfer parts removed in step 2 to new reel motor with turntable.

STEP 4 Reinstall supply reel motor assembly onto transport (refer to paragraph 7-11).

STEP 5 Adjust parking brake as described in paragraph 7-34.

7-19 Parking Brake Band Assembly

Replace supply parking brake band assembly as follows:

STEP 1 Remove transport trim as described in paragraph 4-12, Part I.

STEP 2 Refer to Figure 7-17. Remove two 6-32 hex-recessed screws with plain washers and two 6-32 hex-recessed screws (no washers), and detach brake band guide from motor mounting plate.

STEP 3 Remove two retaining rings that secure parking brake band assembly and detach brake band.

STEP 4 Install new parking brake band assembly and secure with retaining rings removed in step 3.

STEP 5 Reinstall brake band guide and secure with hardware removed in step 2.

STEP 6 Adjust parking brake as described in paragraph 7-34.

STEP 7 Reinstall transport trim.

7-20 Supply Reel Motor Brushes

The supply reel motor has two brushes (Ampex P/N 592-458) which seldom wear out. However, if a brush should wear out or become noisy, replace brushes as follows:

STEP 1 Remove supply reel motor assembly from transport as described in paragraph 7-11.

STEP 2 To remove motor brush, use a large-bladed screwdriver and unscrew motor endplug. The brush has a spring attached which maintains pressure against motor commutator. Slide old brush out of motor brush holder.

STEP 3 Clean new brush with isopropyl alcohol and allow brush to dry before installing into motor.

STEP 4 Secure new brush and spring with endplug removed in step 2.

STEP 5 Reinstall supply reel drive motor assembly into transport. See paragraph 7-11.

7-21 Takeup Reel Motor Assembly

The following paragraphs cover parts replacement on the takeup reel motor assembly. Instructions are given for replacing takeup reel motor, parking brake band assembly, and motor brushes.

7-22 Takeup Reel Motor

Note

If factory-assembled reel motor assembly with turntable (Ampex Part No. 1463290 or 1463318) is to be used for motor replacement instead of a bare motor, proceed to paragraph 7-23.

Replacing the takeup motor requires removing the takeup reel motor assembly from the transport, and separating the turntable from the motor. Proceed as follows:

STEP 1 Remove takeup reel motor assembly from transport as described in paragraph 7-12.

STEP 2 Remove two 8-32 cross-recessed screws and washers that secure motor shield to motor mounting plate and remove shield. See Figure 7-18.

STEP 3 Remove hex-recessed screw that secures retainer to reel knob. Remove retainer (circular plate) and nylon washer under retainer.

STEP 4 Use a 3/32-in. hex-drive wrench to loosen three setscrews that secure turntable assembly to motor shaft. Access to screws is provided by a notch in motor mounting plate. See section A-A in Figure 7-18.

STEP 5 Relax brake band tension by pressing low-tension arm assembly toward turntable. See Figure 7-19. Then pull turntable assembly straight up to remove from motor shaft. If turntable assembly is not easily removed, force off shaft by rotating turntable elevation adjustment setscrew clockwise. Access to elevation setscrew is through hole vacated by retainer screw removed in step 3. Use a 3/32-in. hex-drive wrench to turn screw clockwise and raise turntable. After removal, turn setscrew

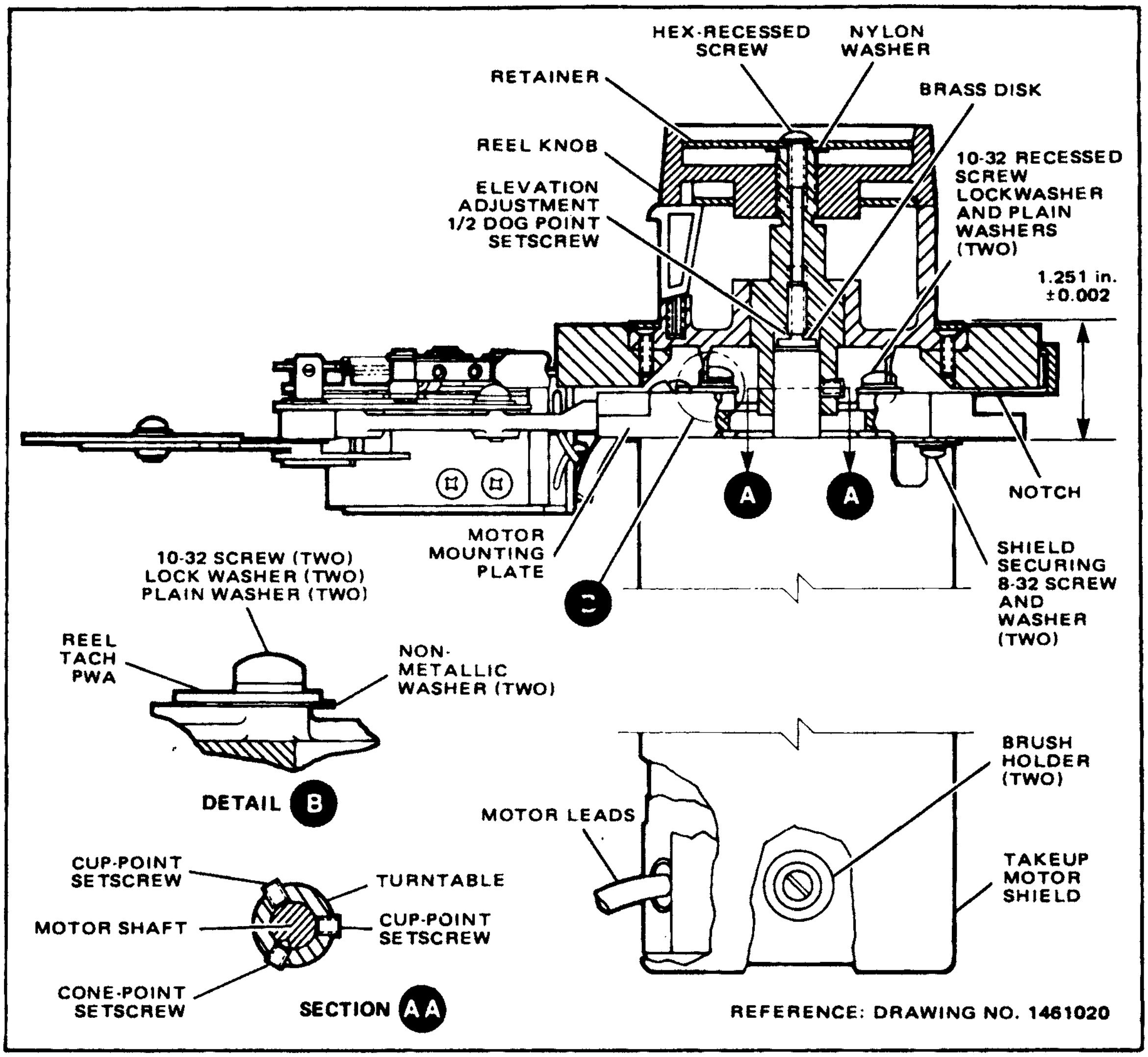


Figure 7-18. Replacing Takeup Reel Motor

counterclockwise approximately an equal amount of turns, or until stop is reached. When turntable assembly is removed, be sure to save the small loose brass reel motor disk on the end of motor shaft.

CAUTION

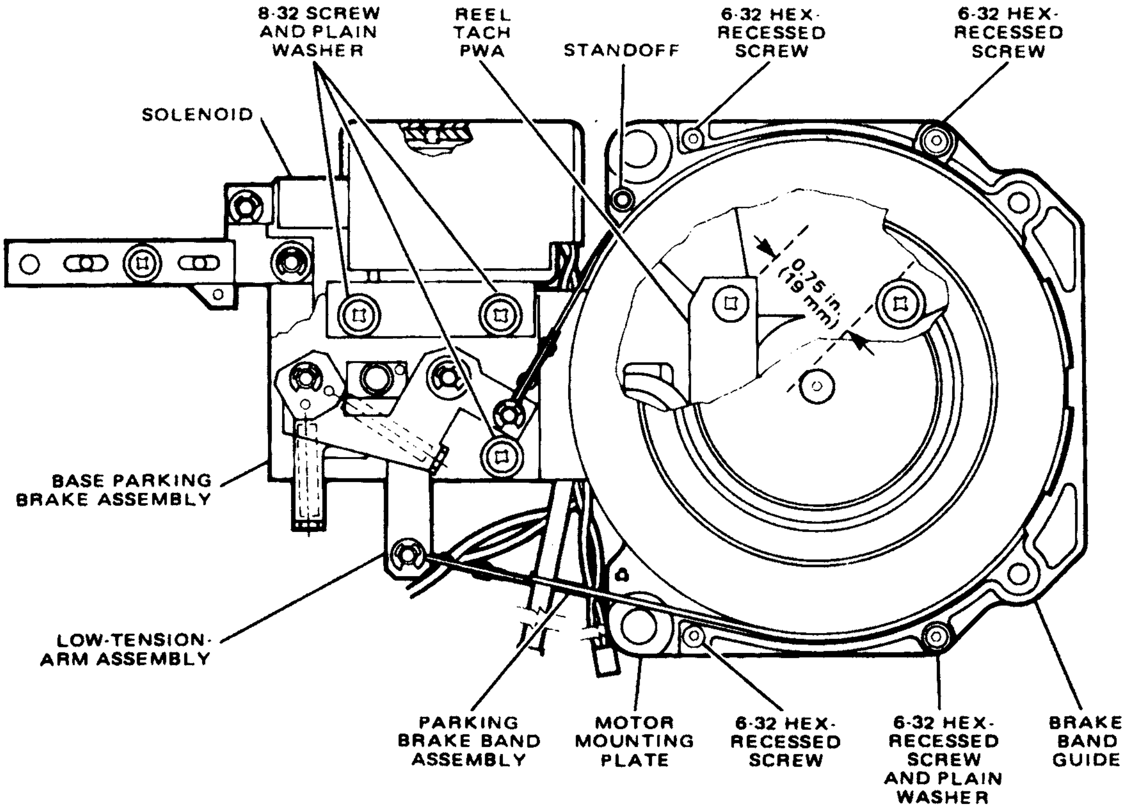
IF ELEVATION ADJUSTMENT SETSCREW SHOULD COME OUT OF THE TURNTABLE, IT MUST BE REINSTALLED FROM THE BOTTOM OF TURNTABLE; IT WILL JAM IF INSTALLED FROM THE TOP.

STEP 6 There are four 10-32 cross-recessed screws and hardware that secure reel drive motor to motor mounting plate. Two of these screws also secure Reel Tachometer PWA to motor mounting plate. Remove four screws and hardware and separate motor mounting plate from motor. See detail B in Figure 7-18.

Attach new motor-to-motor mounting plate as follows:

STEP 7 Note orientation of motor leads with respect to motor mounting plate (Figure 7-18). Loosely install two 10-32 screws, plain washers, and lock washers shown on the right-hand side of Figure 7-18.

STEP 8 Refer to detail B in Figure 7-18 and install parts in sequence as follows: two nonmetallic washers, Reel Tachometer PWA, two plain washers, two lock washers, and two 10-32 screws. See Figure 7-19. Before loosely installing PWA securing screws, set distance between edge of motor shaft and center point of two optical coupler slots to 0.75 in. (19.1 mm).



REFERENCE DRAWING NO. 1461020

Figure 7-19. Takeup Reel Motor Assembly (with Turntable) Components

STEP 9 Ensure that plain washers are not contacting traces on PWA, and then torque the four screws installed in steps 7 and 8 to 13.0 in.-lb (1.46 Newton-meters).

STEP 10 Place brass disk removed in step 4 on top of motor shaft.

STEP 11 See section A-A in Figure 7-18. Install turntable assembly on motor shaft as follows. Position motor shaft so that V-groove in shaft is visible through notch in motor mounting plate. Position turntable assembly so that cone-point setscrew slides into V-groove of motor shaft.

STEP 12 Before tightening setscrews, set turntable height to 1.251 in. (31.78 mm) as follows:

Note

The cork pad on the turntable is soft and does not provide a suitable surface for measuring turntable height. For this reason, a metal hub from a tape reel is placed on the turntable to compress the turntable cork pad and also serve as a reference measuring surface.

a. Remove metal hub from a tape reel.

b. Use a vernier caliper to measure height of the hub at its thickest point. Record measurement.

c. Place hub on turntable and loosely tighten reel knob.

d. With turntable pressed down so elevation adjustment setscrew is firm against brass reel motor disk, use vernier caliper to measure distance between bottom surface of motor mount plate and top surface of hub. Then tighten reel knob to compress cork pad a minimum of 0.005 in., or 5 mils (5 mils = 0.1270 mm) as measured by vernier caliper. Record reading.

e. Subtract hub height from value recorded in step 12d. The resulting difference should be 1.251 ±0.002 in. (31.78 mm ±0.0508 mm). Adjust turntable height adjustment screw as required to obtain correct height (turning screw clockwise increases height).

STEP 13 After correct turntable height is established, tighten motor shaft setscrews to 13.0 in.-lb (1.46 Newton-meters) in the following sequence. First tighten cone-point setscrew (located in V-groove of motor shaft), and then tighten two cup-point setscrews.

STEP 14 Recheck turntable height. If necessary, loosen motor shaft setscrews and reset turntable height.

STEP 15 Reinstall nylon washer, retainer, and hex-recessed screw removed in step 3.

STEP 16 Reinstall shield removed in step 2.

STEP 17 Reinstall takeup reel motor assembly into transport.

STEP 18 Adjust parking brake as described in paragraph 7-34.

Attach new motor-to-motor mounting plate as follows:

STEP 7 Note orientation of motor leads with respect to motor mounting plate (Figure 7-18). Loosely install two 10-32 screws, plain washers, and lock washers shown on the right-hand side of Figure 7-18.

STEP 8 Refer to detail B in Figure 7-18 and install parts in sequence as follows: two nonmetallic washers, Reel Tachometer PWA, two plain washers, two lock washers, and two 10-32 screws. See Figure 7-19. Before loosely installing PWA securing screws, set distance between edge of motor shaft and center point of two optical coupler slots to 0.75 in. (19.1 mm).

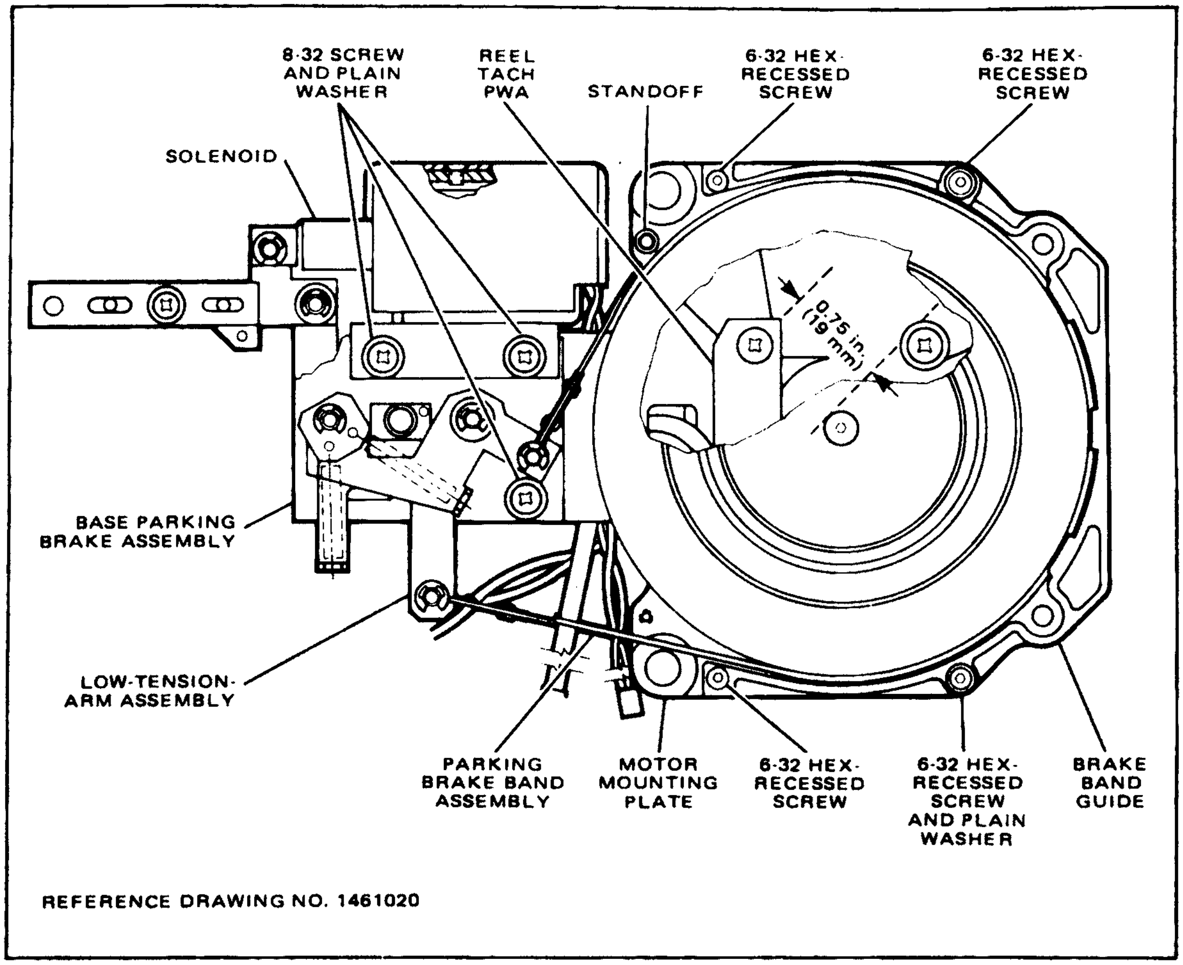


Figure 7-19. Takeup Reel Motor Assembly (with Turntable) Components

STEP 9 Ensure that plain washers are not contacting traces on PWA, and then torque the four screws installed in steps 7 and 8 to 13.0 in.-lb (1.46 Newton-meters).

STEP 10 Place brass disk removed in step 4 on top of motor shaft.

STEP 11 See section A-A in Figure 7-18. Install turntable assembly on motor shaft as follows. Position motor shaft so that V-groove in shaft is visible through notch in motor mounting plate. Position turntable assembly so that cone-point setscrew slides into V-groove of motor shaft.

STEP 12 Before tightening setscrews, set turntable height to 1.251 in. (31.78 mm) as follows:

Note

The cork pad on the turntable is soft and does not provide a suitable surface for measuring turntable height. For this reason, a metal hub from a tape reel is placed on the turntable to compress the turntable cork pad and also serve as a reference measuring surface.

a. Remove metal hub from a tape reel.

b. Use a vernier caliper to measure height of the hub at its thickest point. Record measurement.

c. Place hub on turntable and loosely tighten reel knob.

d. With turntable pressed down so elevation adjustment setscrew is firm against brass reel motor disk, use vernier caliper to measure distance between bottom surface of motor mount plate and top surface of hub. Then tighten reel knob to compress cork pad a minimum of 0.005 in., or 5 mils (5 mils = 0.1270 mm) as measured by vernier caliper. Record reading.

e. Subtract hub height from value recorded in step 12d. The resulting difference should be 1.251 ±0.002 in. (31.78 mm ±0.0508 mm). Adjust turntable height adjustment screw as required to obtain correct height (turning screw clockwise increases height).

STEP 13 After correct turntable height is established, tighten motor shaft setscrews to 13.0 in.-lb (1.46 Newton-meters) in the following sequence. First tighten cone-point setscrew (located in V-groove of motor shaft), and then tighten two cup-point setscrews.

STEP 14 Recheck turntable height. If necessary, loosen motor shaft setscrews and reset turntable height.

STEP 15 Reinstall nylon washer, retainer, and hex-recessed screw removed in step 3.

STEP 16 Reinstall shield removed in step 2.

STEP 17 Reinstall takeup reel motor assembly into transport.

STEP 18 Adjust parking brake as described in paragraph 7-34.

7-23 Takeup Reel Motor with Turntable

Note

If a bare reel motor is to be used for replacement instead of a factory-assembled reel motor with turntable, refer to instructions given in paragraph 7-22.

Use the following procedure to replace the takeup reel motor with factory-assembled reel motor with turntable (Ampex Part No. 1463290 or 1463318). Proceed as follows:

STEP 1 Remove takeup reel motor assembly from transport as described in paragraph 7-12.

STEP 2 Remove two 8-32 cross-recessed screws and washers that secure motor shield to motor mounting plate and remove shield. Refer to Figure 7-18.

STEP 3 Refer to Figure 7-19 and disassemble old takeup reel motor assembly as follows:

a. Remove parking brake plate assembly (includes brake band and solenoid) from motor mounting plate by removing three 8-32 cross-recessed screws (with captive lock washer) and plain washers.

b. Remove brake band guide from motor mounting plate by removing two 6-32 hex-recessed screws with plain washer and two 6-32 hex-recessed screws (no washers).

c. Unscrew band guide standoff from motor mounting plate.

STEP 4 Transfer parts removed in step 3 to new reel motor with turntable.

STEP 5 Reinstall motor shield which was removed in step 2.

STEP 6 Reinstall takeup reel motor assembly onto transport (refer to paragraph 7-12).

STEP 7 Adjust parking brake as described in paragraph 7-34.

7-24 Parking Brake Band Assembly

Replace the takeup parking brake band assembly as follows:

STEP 1 Remove transport trim as described in paragraph 4-12, Part I.

STEP 2 Refer to Figure 7-19. Remove two 6-32 hex-recessed screws with plain washers and two 6-32 hex-recessed screws (no washers), and detach brake band guide from motor mounting plate.

STEP 3 Remove two retaining rings that secure parking brake band assembly and detach brake band.

STEP 4 Install new parking brake band assembly and secure with retaining rings removed in step 3.

STEP 5 Reinstall brake band guide and secure with hardware removed in step 2.

STEP 6 Adjust parking brake as described in paragraph 7-34.

STEP 7 Reinstall transport trim removed in step 1.

7-25 Takeup Reel Motor Brushes

The takeup reel motor has two brushes (Ampex P/N 592-458) which seldom wear out. However, if a brush should wear out or become noisy, replace as follows:

STEP 1 Remove takeup reel motor assembly from transport as described in paragraph 7-12.

STEP 2 Remove two 8-32 cross-recessed screws and washers that secure motor shield to motor mounting plate and remove shield. Refer to Figure 7-18.

STEP 3 To remove motor brush, use a large-bladed screwdriver and unscrew motor endplug. The brush has a spring attached which maintains pressure against motor commutator. Slide old brush out of motor brush holder.

STEP 4 Clean new brush with isopropyl alcohol and allow brush to dry before installing into motor.

STEP 5 Secure new brush and spring with endplug removed in step 3.

STEP 6 Reinstall motor shield removed in step 2.

STEP 7 Reinstall takeup reel drive motor assembly into transport. Refer to paragraph 7-12.

7-26 Pinch Roller

The capstan pinch roller and its bearings form an integrated unit and are not separately replaceable. Replace capstan pinch roller with factory-assembled pinch roller and bearing assembly (Ampex Part No. 1378726) as follows:

STEP 1 Remove pinch roller arm assembly from transport as described in paragraph 7-13.

STEP 2 See Figure 7-20. Use a 0.050-in. hex-drive wrench to remove two setscrews that secure needle bearing to pinch roller arm and remove needle bearing. Save the two nylon washers, but discard old pinch roller (and bearings).

STEP 3 Place one drop of light oil lubricant (Ampex Part No. 087-579) in bearing at each end of new pinch roller. Remove any excess oil.

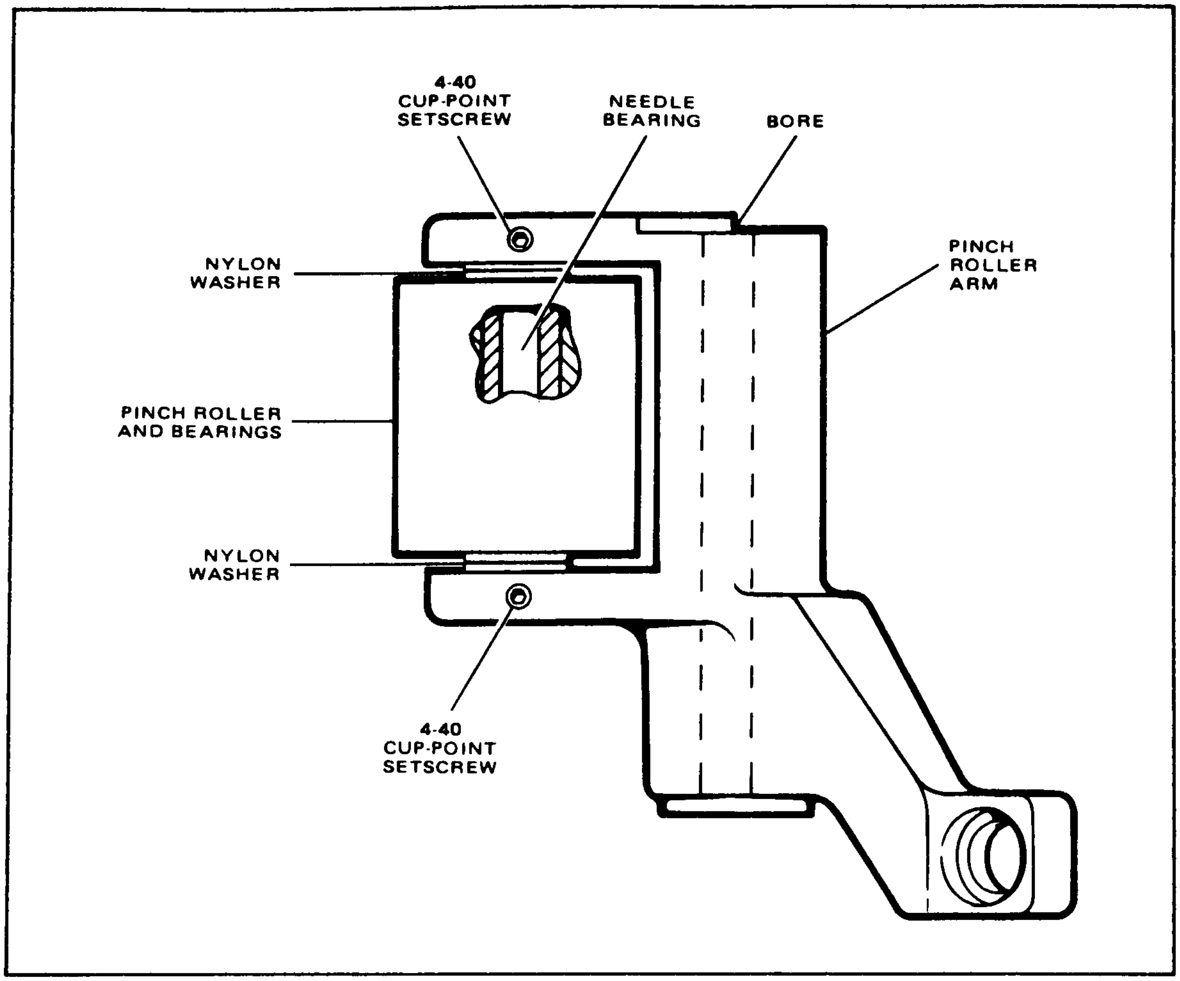


Figure 7-20. Replacing Pinch Roller

STEP 4 Ensure that needle bearing and nylon washers are clean and assemble new pinch roller assembly, two washers, and needle bearing onto pinch roller arm assembly as shown in Figure 7-20.

STEP 5 Torque arm assembly setscrews to 2.5 ±0.5 in.-lb (0.282 ±0.0564 Newton-meters).

CAUTION

WHEN CLEANING PINCH ROLLER ARM, MAKE SURE THAT NO ISOPROPYL ALCOHOL CONTACTS OIL-IMPREGNATED POROUS BRONZE BEARING.

STEP 6 Clean pinch roller with isopropyl alcohol.

STEP 7 Clean pivot shaft and arm assembly bore with isopropyl alcohol. Then lightly coat pivot shaft with dry-film lubricant (Ampex Part No. 087-581).

STEP 8 Reinstall pinch roller arm assembly, solenoid, and PWA.

STEP 9 Adjust pinch roller pressure as described in paragraph 4-22, Part I.

7-27 Rotating Guide Assembly Bearings

The rotating guide assembly contains an upper and lower flanged ball bearing. If bearing replacement is required, bearings (Ampex Part No. 420-142) should be replaced as a pair. To replace bearings, proceed as follows:

STEP 1 Remove transport trim as described in paragraph 4-12, Part I.

STEP 2 Refer to Figure 7-15. Using a 9/64-in. hex-drive wrench, remove three 8-32 hex-socket head screws and lock washers, and detach rotating guide assembly from the front of the transport.

STEP 3 See Figure 7-21. At the bottom end of the guide, use a 5/64-in. hex-drive wrench to remove the 6-32 buttonhead screw from shaft. Then remove preload compression spring and shim washer.

STEP 4 Carefully withdraw shaft from center of bearings. Remove and discard old bearings. Ensure that upper shim washer and retaining ring remain on shaft.

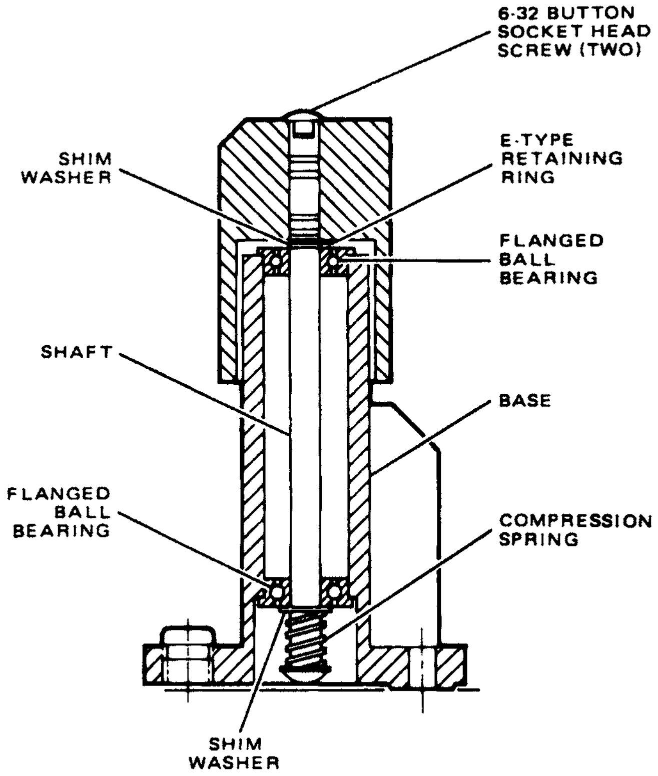


Figure 7-21. Rotating Guide Assembly Components

STEP 5 To prevent damage to bearing race, press both bearings into base as follows: Place new bearing square onto hole position on base and use a 3/8-in. spin-tight wrench as a tool to press on bearing flange to seat bearing.

CAUTION

WHEN INSERTING GUIDE SHAFT, DO NOT TIP SHAFT SIDEWAYS AS DAMAGE TO BEARING RACE CAN OCCUR.

STEP 6 Insert guide shaft straight into place through center of bearings.

STEP 7 At the bottom end of the guide, reinstall shim washer, preload compression spring, and screw removed in step 3.

Reinstall guide assembly on transport as follows:

STEP 8 Note location of factory-adjusted perpendicularity adjusting screw on guide base. Position guide on transport so that adjusting screw faces upward (toward timer idler assembly). Secure guide assembly to transport using screws and lock washers removed in step 2. Torque screws to 12 in.-lb (1.34 Newton-meters).

Note

Over-torquing screws can affect guide perpendicularity and result in tape guiding problems.

STEP 9 Reinstall transport trim removed in step 1.

7-28 TRANSPORT SYSTEM ALIGNMENT

7-29 MDA Alignment

7-30 Reel MDAs

The following steps must be completed before either takeup or supply reel MDAs can be aligned. Tape need not be threaded on the transport, and neither audio nor video inputs are necessary.

STEP 1 With VPR-80 power off, loosen two captive screws in upper rear corners of cabinet and lower rear door assembly.

STEP 2 Disconnect supply motor connector SUP J1/P1 and takeup motor connector TU J1/P1. See Figure 7-22.

STEP 3 Open top access door on card cage and remove Servo PWA.

STEP 4 On Servo PWA, remove jumpers 5J6 (SUPPLY ERROR) and 5J7 (TU ERROR). Ground the B contact of jumpers 5J6 and 5J7 to test point 5TPG5. See Figure 5-68 in Section 5.

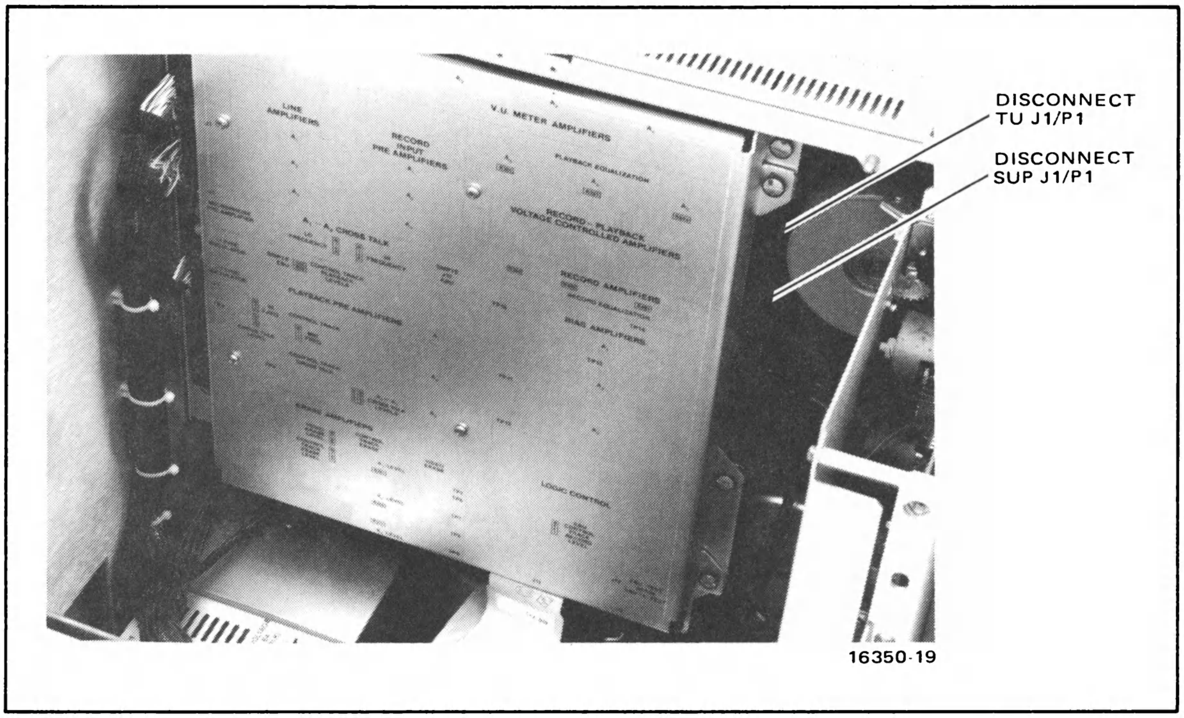


Figure 7-22. Disconnecting Reel Motors

STEP 5 Mount Servo PWA on an extender and reinstall in card cage.

STEP 6 Remove three screws and washers and open hinged cover over Reel MDA PWA.

CAUTION

BE CAREFUL NOT TO ALLOW SCREWS AND WASHERS TO DROP INTO POWER SUPPLY.

STEP 7 Block tape-in-path sensor on Tape Timer Tach/TIP PWA (timer idler assembly).

STEP 8 Turn on VPR-80 power, and press PLAY.

STEP 9 Press STOP. Leave TIP sensor blocked.

Note

Momentary activation of play mode inhibits MDA INHIBIT command.

STEP 10 Set vertical scale of scope channels 1 and 2 to 2V/cm.

STEP 11 Connect scope channel 1 probe to Reel MDA PWA test point TP1 (see Figure 7-27), and adjust scope vertical position so that sawtooth waveform is centered in the graticule, as shown in Figure 7-23. Set scope time base to 5 µs/cm.

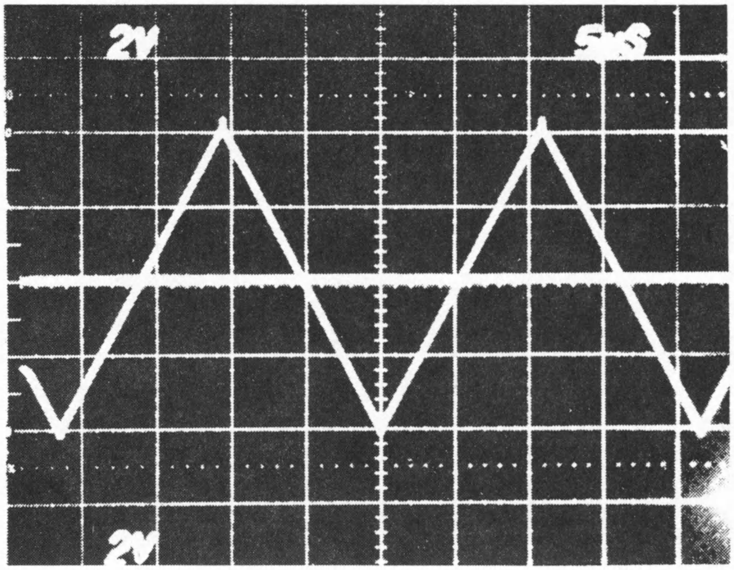


Figure 7-23. MDA Alignment—46.5-kHz Reference Oscillator Waveform

STEP 12 Ground channel 1 and 2 inputs of the scope and adjust channel 2 input to match channel 1 input exactly. Then unground channel 2 input, dc-coupled.

7-31 **Takeup Reel MDA.** Having completed steps 1 through 12 of the preceding paragraph, align takeup reel MDA as follows:

STEP 1 Connect scope channel 2 probe to test point TP6 (INPUT ERROR) on Reel MDA PWA. See Figure 7-27.

STEP 2 Adjust R118 (ZERO ERROR OFFSET ADJ) on Reel MDA PWA so that dc level (scope channel 2) is in center of isosceles waveform (scope channel 1). See Figure 7-24.

STEP 3 Reconnect takeup motor connector TU J1/P1. See Figure 7-22.

STEP 4 If necessary, adjust R140 (CURRENT SENSE ZERO BALANCE) on Reel MDA PWA to center dc level (scope channel 2) in isosceles waveform (scope channel 1).

7-32 **Supply Reel MDA.** Having completed instructions in the two preceding paragraphs, align supply reel MDA as follows:

STEP 1 Connect scope channel 2 probe to test point TP3 (INPUT ERROR) on Reel MDA PWA. Leave scope channel 1 probe connected to test point TP1.

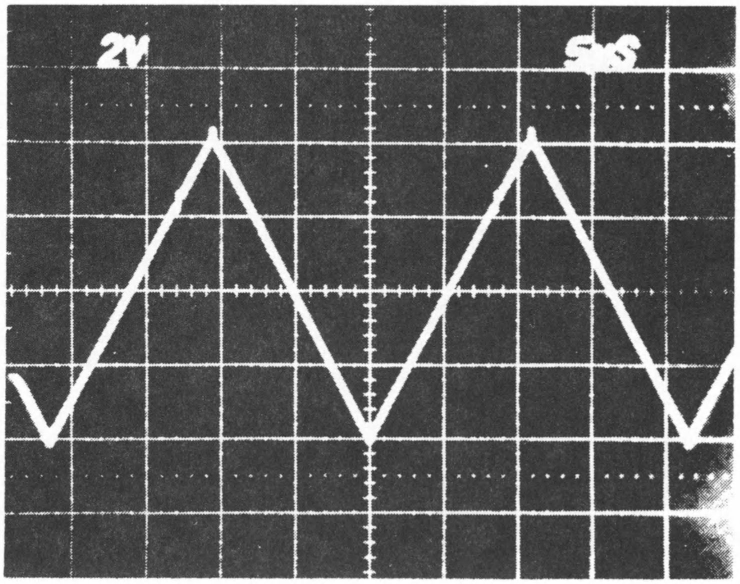


Figure 7-24. Input Error DC Level Centered in Reference Oscillator Waveform

STEP 2 Adjust R56 (ZERO ERROR OFFSET ADJ) on Reel MDA PWA so that dc level (scope channel 2) is in center of isosceles waveform (scope channel 1). See Figure 7-24 and Figure 7-27.

STEP 3 Reconnect supply motor connector SUP J1/P1. See Figure 7-22.

STEP 4 If necessary, adjust R76 (CURRENT SENSE ZERO BALANCE) on Reel MDA PWA to center dc level (scope channel 2) in isosceles waveform (scope channel 1).

STEP 5 Turn VPR-80 power off. Remove ground connection from jumpers J6 and J7 on Servo PWA. Reinstall jumpers J6 and J7 on Servo PWA. Reinstall Servo PWA. Close hinged cover over Reel MDA PWA and secure with three screws and washers.

CAUTION

BE CAREFUL NOT TO ALLOW SCREWS AND WASHERS TO DROP INTO POWER SUPPLY.

7-33 Capstan/Scanner MDA

The Capstan/Scanner MDA PWA contains no adjustable components, and therefore neither adjustments nor alignment procedures are required for this PWA.

7-34 Parking Brake Adjustments

Parking brake assembly adjustments are made with VPR-80 power off. Adjustments for supply and takeup reel brakes are essentially the same. These adjustments ensure that brake bands do not touch either turntable flywheel at any point when brakes are released. Brake actuation timing is also adjusted to provide simultaneous contact of brake bands on supply and takeup reel flywheels. Braking force is then measured at reel hub diameter (4.5 in./11.43 cm) on each turntable, and adjusted as necessary.

7-35 Clearances

First measure critical clearances and make adjustments, if necessary, as follows:

STEP 1 Remove transport trim as outlined in paragraph 4-12, Part I.

STEP 2 At supply reel turntable, measure clearance between brake band guide (Figure 7-25, A) and flywheel (B). Measure at point indicated in Figure 7-25. Clearance should be 0.02 to 0.03 in. (0.5 to 0.8 mm).

STEP 3 If clearance is not within these limits, loosen four brake band guide mounting screws (C) and reposition brake band guide. Tighten mounting screws.

STEP 4 Repeat steps 2 and 3 on takeup reel turntable.

STEP 5 At supply reel side of brake linkage, measure clearance between plate assembly (D) and low tension arm (E). These parts are shown in the inset in Figure 7-25. Clearance should be 0.05 in. (1.3 mm) minimum.

Note

Clearance between plate assembly (D) and low tension arm (E) should be at least 0.05 in. (1.3 mm). The specific dimension is not critical as long as it is not less than this minimum, which can be measured by passing a wire of 0.05-in. (1.3-mm) diameter in the space between (D) and (E). This minimum clearance must be present to allow adjustment of brake forces (paragraph 7-36).

STEP 6 If clearance is less than 0.05 in. (1.3 mm), loosen three plate assembly mounting screws (F) and reposition plate assembly. Tighten mounting screws.

STEP 7 Repeat steps 5 and 6 on takeup side of brake linkage. Plate assembly is shown as (G) in Figure 7-25. Plate assembly mounting screws are shown as (H).

7-36 Braking Forces

Measure and adjust (if necessary) braking force on supply and takeup reels, in both clockwise and counterclockwise directions, as follows:

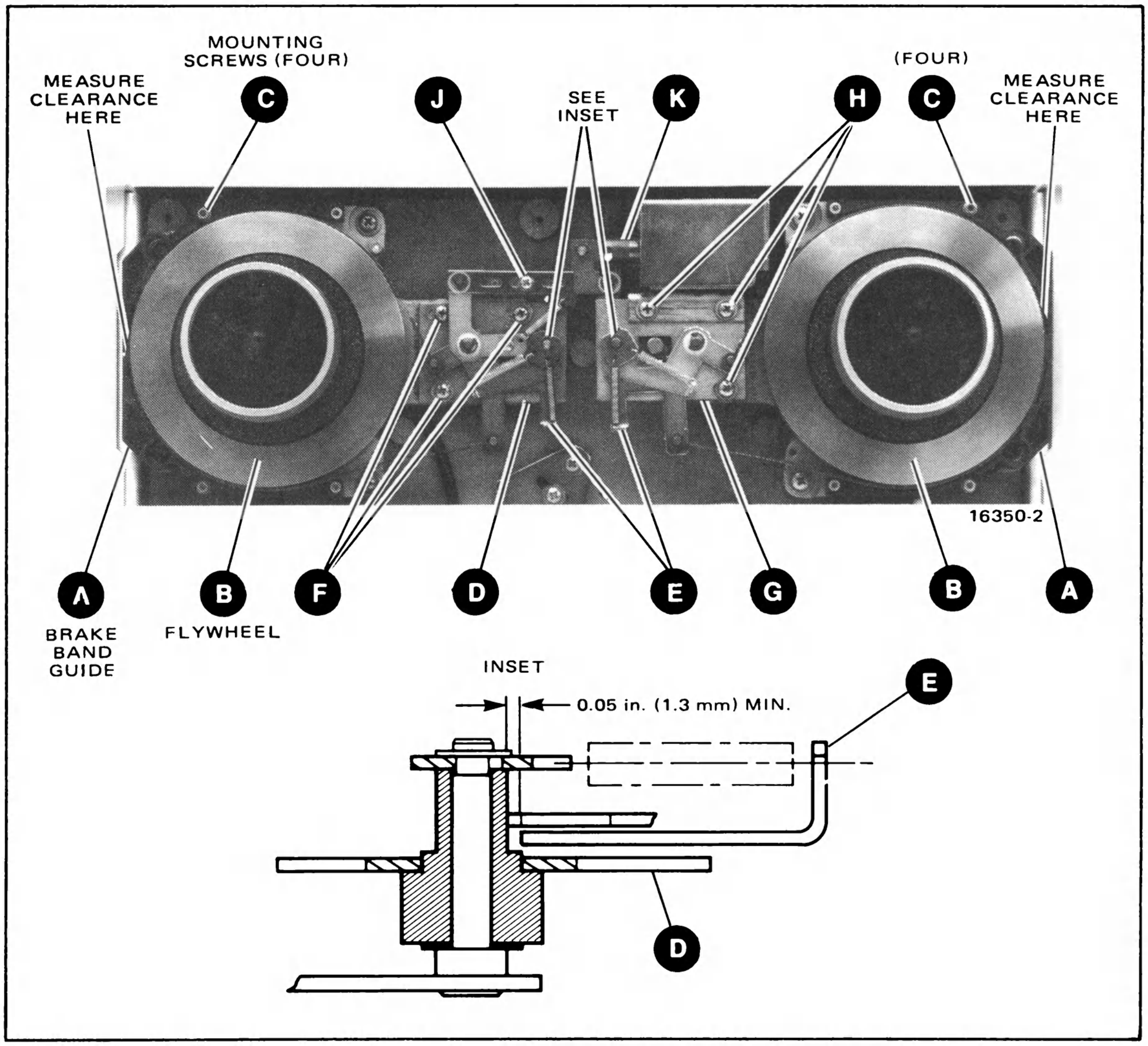


Figure 7-25. Parking Brake Adjustment

STEP 1 Cut a convenient length of lacing cord (i.e., 6 ft/1.83m) and tie it around a 4.5-in. (11.43-cm) reel hub. Mount reel on supply turntable with loose end of cord exiting from bottom of reel to the left. (Pulling cord turns reel clockwise.) Using a spring scale on end of cord, measure brake force by reading pulling force required to overcome supply reel brake force in clockwise direction. Supply reel clockwise brake force should be 11.5 oz. ±3.5 oz. (325g ±100g). See Figure 7-26.

STEP 2 If brake force is not within tolerances, loosen three screws (Figure 7-25, F). Slide plate assembly toward turntable to decrease braking force or away from turntable to increase braking force.

STEP 3 Rewind cord used in step 1 so that it exits from top of supply reel to the left. (Pulling cord turns reel counterclockwise.) Attach spring scale and

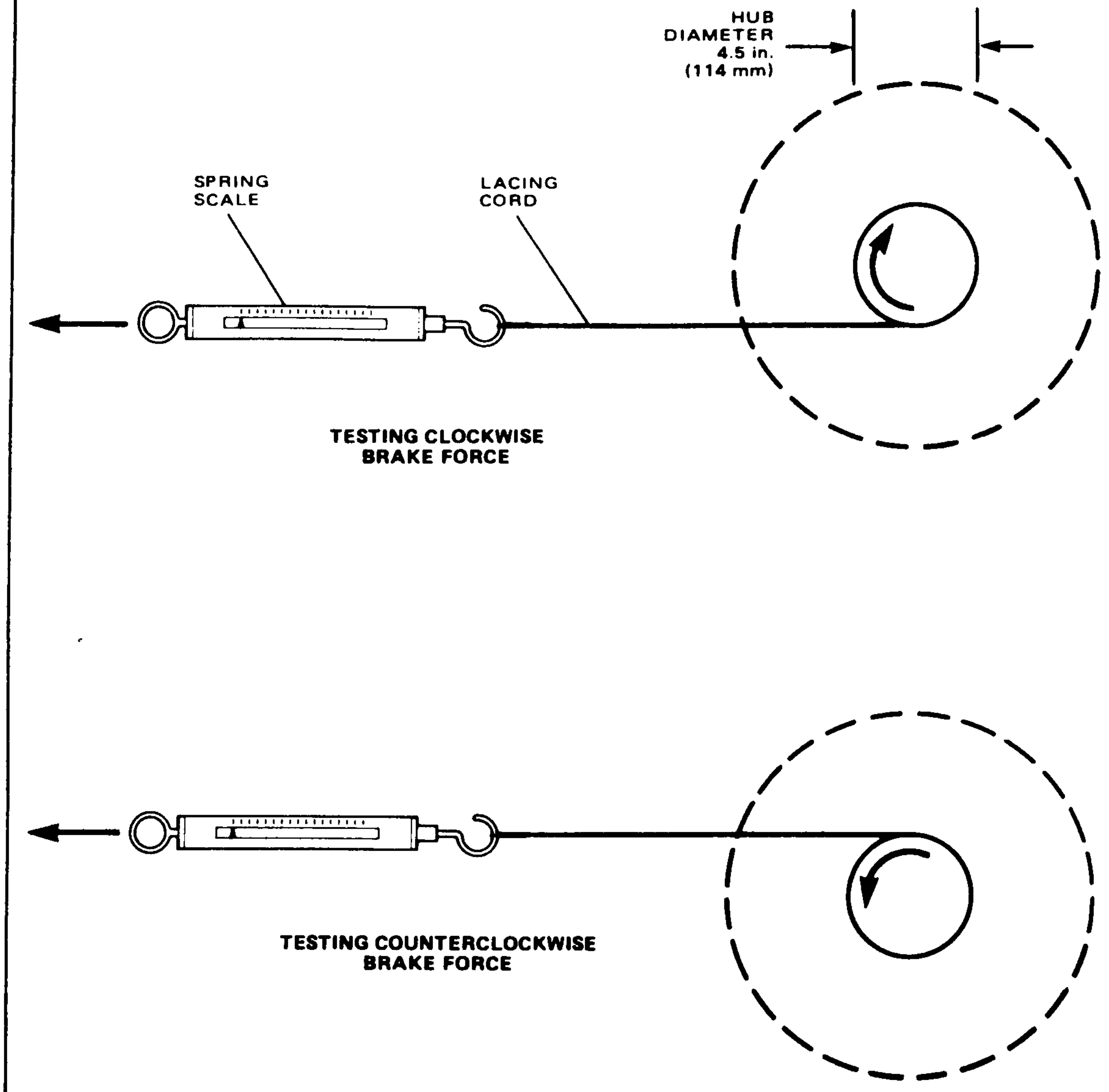


Figure 7-26. Measuring Braking Forces

measure supply reel brake force in counterclockwise direction. Supply reel counterclockwise brake force should be 2 lb, 10 oz ±10 oz (1200g ±300g).

STEP 4 Repeat step 2 if counterclockwise brake force is not within tolerances.

STEP 5 Repeat steps 1 through 4 on the takeup turntable. Clockwise brake force should be 2 lb, 10 oz ±10 oz (1200g ±300g). Counterclockwise brake force should be 11.5 oz ±3.5 oz (325g ±100g). See Table 7-1. Note that brake force values are reciprocal to supply reel turntable values.

Table 7-1. Parking Brake Forces

Brake Force	Supply Reel Turntable	Takeup Reel Turntable
Clockwise	11.5 ±3.5 oz (325 ±100g)	2 lb, 10 oz ±10 oz (1200 ±300g)
Counter-clockwise	2 lb, 10 oz ±10 oz (1200 ±300g)	11.5 ±3.5 oz (325 ±100g)

7-37 Checkout

Finally, check out brake actuation as follows:

STEP 1 Slowly depress brake solenoid plunger (Figure 7-25, K) while observing that both low tension arms (E) move simultaneously. If they do not, loosen screw (J) and adjust its position in the obround hole until both low tension arms move simultaneously when solenoid plunger is depressed.

STEP 2 Depress solenoid plunger (K) completely. Ensure complete release of brakes by spinning turntables. Be sure there is no buckling in brake bands. If necessary, solenoid can be adjusted either way by loosening upper two screws (H) and moving bracket in either direction. Movement of bracket should be within ±0.2 in. (5 mm).

7-38 Performance Verification

The following tests demonstrate compliance of VPR-80 performance to tape speed specifications in record mode, and to specification tolerance for long period (wow) and shorter period (flutter) tape speed variations. Audio flutter tapes listed in Table 7-2 are used for these performance verifications.

Table 7-2. Audio Flutter Tapes

Ampex Catalog Number	Description	Length (Minutes)
1498602	525/NTSC Audio Flutter (3 kHz at 9.6063 in/s)	5
1498603	625/PAL Audio Flutter (3 kHz at 9.4409 in/s)	5

7-39 Record Tape Speed

VPR-80 record tape speed specifications are as follows:

Video System	Specification
525/60	9.6.6 ±0.02 in/s (244.0 ±0.5 mm/s)
625/50	9.440 ±0.02 in/s (239.8 ±0.5 mm/s)

The flutter tape is a 3-kHz ±6-Hz tone recorded at specified speed. Since the flutter tape does not have a control track recording, the VPR-80 will play the tape at transport record speed. Monitoring playback of the flutter tape with an audio frequency counter will verify record mode tape speed.

Verify record tape speed as follows:

STEP 1 Thread appropriate Ampex flutter tape on transport.

STEP 2 Connect audio frequency counter to AUDIO 1 OUT connector on VPR-80 I/O connector panel. Adjust frequency counter controls as necessary to monitor a 3-kHz input.

STEP 3 Turn on VPR-80 power and press MASTER RECORD LOCKOUT. Red indicator should be lighted.

STEP 4 Press PLAY and monitor audio frequency counter, which will display 3000 Hz ±6 Hz.

7-40 Wow and Flutter

VPR-80 wow and flutter specifications are as follows:

Video System	Specification
525/60	0.12% rms or less NAB unweighted
625/50	0.15% or less, DIN weighted on own recording

Compliance of the VPR-80 to wow and flutter specifications is demonstrated with an Ampex flutter tape and the Micom (Bahrs) Model 8100-W flutter meter. Wow and flutter are measured by playing the 3-kHz frequency tone on the flutter tape. Any nonuniform motion in the transport frequency modulates the tone. This modulation is measured by fm demodulator within the flutter meter. VPR-80 flutter characteristics are measured according to standards specified by DIN 45-507 and ANSI S4.3 peak weighted and unweighted. The rms flutter is measured as specified by NAB standard.

Prior to making a flutter measurement, do the following:

STEP 1 Clean and demagnetize audio heads and other tape path components as described in Section 4, Part I of this manual.

Note

Flutter meters are sensitive to amplitude modulation resulting from poor head-to-tape contact or from signal dropouts.

STEP 2 Check tape tension and adjust, if necessary, as described in Section 4, Part I of this manual.

STEP 3 Audio channel 2, which is used for flutter measurement, should be correctly aligned. Check alignment of audio channel 2. Refer to audio signal system alignment procedures in Section 4, Part II of this manual.

The following procedure applies to use of a Micom (Bahrs) Model 8100-W flutter meter. If a different flutter meter is used, manufacturer's instructions should be followed.

To measure wow and flutter proceed as follows:

STEP 1 Thread appropriate Ampex flutter tape on transport.

STEP 2 Connect flutter meter to AUDIO 2 OUT connector on VPR-80 I/O connector panel.

STEP 3 Turn on VPR-80 power, and press MASTER RECORD LOCKOUT. Red indicator should be lighted.

STEP 4 Press PLAY and adjust VPR-80 AUDIO PLAY control for channel 2 and/or flutter meter input level control for required flutter meter input level.

STEP 5 Make a note of indications on flutter meter display. Rewind at end of flutter tape.

STEP 6 Repeat steps 4 and 5 three times, and average four readings.

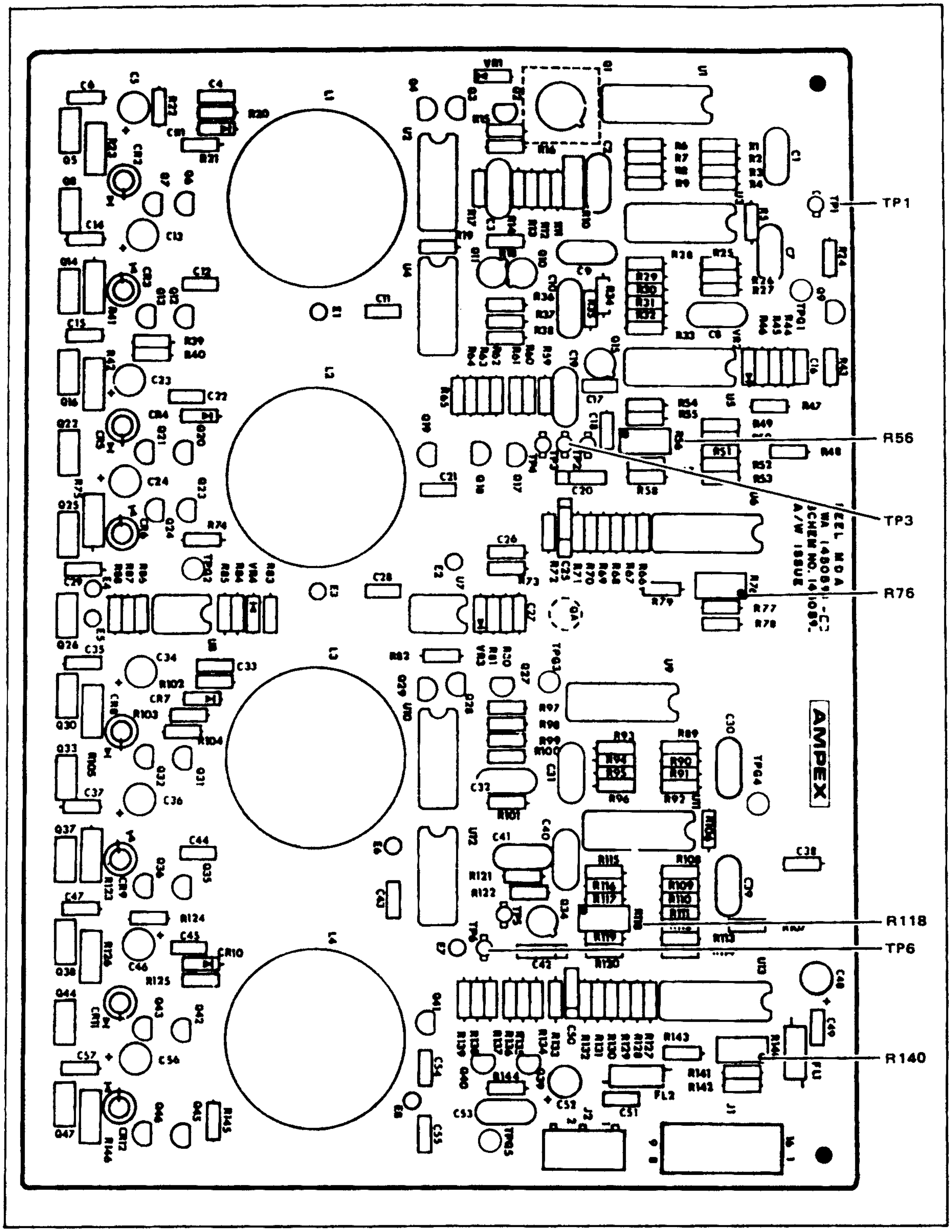


Figure 7-27. Reel MDA PWA Test Points and Adjustments

PART II

SECTION 8

ACCESSORIES

8-1 GENERAL

This section provides theory of operation discussions, removal and reinstallation instructions, and, where applicable, calibration procedures for the Parallel Remote PWA, Serial Remote PWA, and Time-Code System PWA, which are accessories to the VPR-80.

The following drawings, which are included in the *VPR-80 Parts Lists and Schematics* manual, are referenced in this section.

Drawing	Drawing No.
Parallel Remote PWA	1450466
Parallel Remote PWA Schematic	1450468
Serial Remote PWA	1472470
Serial Remote PWA Schematic	1472471
Time-Code System PWA	1450410
Time-Code System PWA Schematic	1450412

In addition, the following illustrations are included at the end of this section.

Figure 8-22. Parallel Remote PWA Mode Switch and Jumper

Figure 8-23. Control PWA Remote Shuttle Control Calibration

Figure 8-24. Serial Remote PWA Test Points, Jumpers, and Indicators

Figure 8-25. Time-Code System PWA Test Points, Jumpers, Indicators, and Adjustments

8-2 PARALLEL REMOTE PWA

The Parallel Remote PWA provides the interface between an external, remotely located control panel and the VPR-80 Control PWA. Parallel control inputs and parallel output lines to remote indicators are routed through the PARALLEL REMOTE connector (J1) at the rear of the VPR-80 cabinet. Parallel I/O lines between the Parallel Remote and Control PWAs are contained in a PWA-edge-to-PWA-edge connector which acts as a jumper plug between the two adjacent PWAs.

The Parallel Remote PWA can be used as an interface to the Ampex Computerized Editor (ACE) system, an Ampex VPR-2/2B remote control panel, or a compatible remote control device of the user's design. When used with the ACE, the system must also include machine interface (MIF) devices which provide parallel/serial conversion. In addition, the mode switch on the Parallel Remote PWA must be placed in the ACE position. When the VPR-2/2B remote control panel or the

SMC-100 slow-motion controller is used, the mode switch must be in the VPR-2 position. If other than ACE, VPR-2/2B, or SMC-100 I/O signals are interfaced, the mode switch is left in the NORMAL position. See paragraph 8-10 for details.

Parallel Remote PWA I/O connections are enabled only when the operator selects parallel remote operation by setup code, and the REM 1 indicator on the VPR-80 control panel is lighted.

Simple remote control and inputs from parallel and serial remote control accessories are enabled by the REM 1 switch on the primary control panel. The following setup procedure determines which source of remote 1 input is enabled. Select parallel remote operation as follows:

STEP 1 Press SET UP. SET UP indicator lights.

STEP 2 Press keypad switch 2.

STEP 3 Press ENTER. Display indicates enabled remote 1 input.

- If 2-1 is displayed, simple remote control is enabled.
- If 2-2 is displayed, Parallel Remote Control PWA is enabled.
- If 2-3 is displayed, Parallel Remote Control PWA (with color framer forced on) is enabled.
- If 2-4 is displayed, Serial Remote Control PWA is enabled.

STEP 4 Press keypad switch 2 to enable parallel remote control, or press keypad switch 3 to enable parallel remote control (with color framer forced on).

STEP 5 Press ENTER. Display is changed to **2-X,** as selected in step 4.

STEP 6 Press alternate action SET UP switch to exit setup mode.

Pin assignments in the PARALLEL REMOTE connector (J1) are shown in Table 8-1. Signal logic levels are expressed as high/low in the Characteristics column. For example: rev/fwd, where reverse = high and forward = low.

Table 8-1. Parallel Remote Connector Pin Assignments

Pin No.	Name	Description	Characteristics
4	+12V	Regulated	+12 Vdc
12	−12V	Regulated	−12 Vdc
18	+11V lamp drive	Unregulated	+11 Vdc
25	+5V	Regulated	+5 Vdc

(Continued next page)

Table 8-1. Parallel Remote Connector Pin Assignments (Continued)

Pin No.	Name	Description	Character-istics
31	Ground	Power supply ground	
37	Remote readout 1	BCD 1	
43	Remote readout 2	BCD 2	TTL level
49	Remote readout 4	BCD 4	
55	Remote readout 8	BCD 8	
62	Display clock	Clocks remote readout	TTL clock output
70	Shield for pins 37,43, 49, 55, and 62 (above)	Ground	
76	Rev/Fwd	Identifies direction of tape movement	TTL output: rev/fwd
1	Play switch	Initiates play mode	OC input: off/play
8	Play lamp	Lights play mode indicator	OC output: off/on
15	Stop switch	Initiates stop mode	OC input: off/stop
22	Stop lamp	Lights stop mode indicator	OC output: off/on
28	Ready switch	Initiates ready mode	OC input: off/ready
34	Ready lamp	Lights ready mode indicator	OC output: off/on
40	Reset (zero) switch	Resets time readout	TTL input: normal/reset
46	Freeze switch	Freezes display	TTL input: normal/freeze
52	Entrance switch	Sets edit entrance point	TTL input: off/entrance

(Continued next page)

Table 8-1. Parallel Remote Connector Pin Assignments (Continued)

Pin No.	Name	Description	Characteristics
58	Auto edit switch	Initiates auto edit mode	TTL input: off/auto edit
65	Search (Cue) switch	Initiates search mode	TTL input: off/search
73	Search (Cue) lamp	Indicates VTR is searching for cue point	TTL output: off/on
79	(Not used)		
5	Record switch	Initiates record mode	OC output: off/record
13	Record lamp	Lights record mode indicator	OC output: off/on
20	Shuttle switch	Initiates shuttle mode	OC input: off/shuttle
26	Shuttle lamp	Lights shuttle mode indicator	OC output: off/on
32	Slow (var play) switch	Initiates slow (var play) mode	OC input: off/slow
38	Slow (var play) lamp	Lights slow (var play) indicator	OC output: off/on
44	Servo Locked lamp	Lights servo status indicator	LED drive: on/off
50	System (Fault-Nonstd) indicator	Lights system (fault-nonstd) indicator	TTL output: on/off
56	Insert switch	Enables insert edit	TTL input: off/insert
63	Assemble switch	Enables assemble edit	TTL input: off/assemble
71	Exit switch	Sets edit exit point	TTL input: off/exit
77	Edit interval indicator	Indicates edit interval	TTL output: off/edit

(Continued next page)

Table 8-1. Parallel Remote Connector Pin Assignments (Continued)

Pin No.	Name	Description	Characteristics
2	TSO speed	Remote tape speed override voltage	Analog input: ± 12 Vdc
10	TSO command	Initiates tape speed override	TTL input: off/TSO
16	Shuttle pot volts	Remote shuttle pot voltage	Analog voltage 0 to − 12 Vdc
23	(Not used)		
29	Shuttle Pot Ground	Ground	
35	Audio 1 Record Enable switch	Enables audio 1 record	TTL input: off/audio 1
41	Audio 2 Record Enable switch	Enables audio 2 record	TTL input: off/audio 2
47	Audio 3 Record Enable switch	Enables audio 3 record	TTL input: off/audio 3
53	Video Record Enable switch	Enables video record	TTL input: off/video
59	Color Framer switch	Activates color framer	TTL input: off/clr framer
66	(Not used)		
74	Color Framer Normal/ Invert switch	Remote color framer phase control	TTL input: normal/invert
80	Color Framer Normal/ Invert switch (Gnd)	Ground	
7	Remote Active	Enables remote control operation	OC output: off/remote
14	Servos locked	Servo status	TTL output: unlocked/ locked
21	TAPE/EE switch	Selects tape/EE operation	TTL input: tape/EE
27,33, 39,45, 51	(Not used)		

(Continued next page)

Table 8-1. Parallel Remote Connector Pin Assignments (Continued)

Pin No.	Name	Description	Characteristics
57	Remote Control Track ground	Ground	
64	Remote Control Track	Capstan timing pulse	TTL output: control track
72	Shield for pin 78 (below)	Ground	
78	Remote Tape Tach	Remote tach timing	TTL output: tape tach
3	Rehearse switch	Rehearses edit interval	TTL input: off/rehearse
11	Audio 4/sync record select bit (also see pin 17 below)	The 2-bit word formed by these TTL inputs enables either audio channel 4 recording, video sync channel recording, or neither.	Pin 11 and pin 17 both high = audio channel 4 recording enabled.
17	Audio 4/sync record select bit (also see pin 11 above)		Pin 11 low and pin 17 high = video sync channel recording enabled. Pin 11 high and pin 17 low = neither audio channel 4 nor video sync channel recording enabled.
24	Record Lockout indicator	Lights record lockout indicator	TTL output: off/on
30	DF indicator	Lights drop frame indicator	OC output: off/drop frame

(Continued next page)

Table 8-1. Parallel Remote Connector Pin Assignments (Continued)

Pin No.	Name	Description	Characteristics
36	Tach Frame	One pulse per frame	TTL output: tach frame
42	(Not used)		
48	Tape Timer indicator	Lights tape time indicator	TTL output: off/tape time
54	TC Reader indicator	Lights time-code reader indicator	TTL output: off/time code
60	(Not used)		
67	Shield for pins 75 and 82 (below)	Ground	
75	Time-code out (low)	Time-code input from external time-code generator	TTL input: time code (low)
82	Time-code out (high)	Time-code input from external time-code generator	TTL input: time code (high)

8-3 Theory of Operation

A simplified diagram of the Parallel Remote PWA is shown in Figure 8-1. The PARALLEL REMOTE connector, J2, is shown in two main segments: command inputs from the remote control device on the left, and indicator/numeric display to the remote device on the right. The PWA-edge connector, J1, is shown at the bottom of the diagram. Remote data and address buffers on the Control PWA are also shown in Figure 8-1. Reference designations of components on the Control PWA are prefixed with 6. Reference designations of components on the Parallel Remote PWA are not prefixed.

Note that blank spaces for connector pin numbers are provided on the right- and left-hand sides of Figure 8-1. If a parallel remote cable is used in which pin assignments are not the same at both ends of the cable, pin contact numbers at the remote device can be entered in spaces provided.

8-4 Control System Interface

Refer back to Figure 6-4, which is an overall diagram of VPR-80 data and address/control bus structure. Interface between Control and Parallel Remote PWAs is shown at the lower left. The diagram shows the connection between the remote address buffer on the Control PWA and the address decoder on the Parallel Remote PWA. It also shows the bidirectional remote data bus between input data buffers and output data latches on the Parallel Remote PWA and the remote data buffer on the Control PWA. Another diagram that should also be reviewed is Figure 6-2, which shows additional details of bus connections between the control system CPU and remote data and address buffers.

8-5 Address/Control Bus. The control system remote address buffer, 6U34, is permanently enabled by jumper connection 6J7. The decoded address that enables the control system remote data buffer, 6U37, is 32XX (PAR REM SEL). This decoded address line is also applied to the input of remote address buffer 6U34 together with address bits A0, A1, A5—A8, and enable clock E. Address output lines of 6U34 are PAR SEL, RA0, RA1, RA5—RA8, and RE.

Address decoder U13 on the Parallel Remote PWA is enabled by PAR SEL and RA8, and is clocked by RE. Decoder U13 sorts out bits RA5—RA7 into one of the eight decoded outputs listed in Table 8-2. The following abbreviations are used in Table 8-2: IDL = input data latch; ODB = output data buffer.

8-6 Data Bus. The 8-bit Parallel Remote PWA data bus (RD0—RD7) is connected to the CPU data bus on the Control PWA by remote data buffer 6U37. Buffer 6U37 is enabled by decoded address 32XX. Direction of data transfer is governed by the R/W logic level from CPU 6U10 (high = read, low = write). On read transfers, input data buffer U12, U8, U1, or U4 is enabled by decoded address output U13. On write transfers, output data latch U9, U5, or U2 or register file U21/U18 is enabled by the decoded address output U13.

8-7 Input Data Buffers

Input data buffers U12, U8, U1, and U4 place switch closure information from the remote control panel on the remote data bus (and the CPU data bus) to CPU 6U10. Six primary mode switch inputs to U12 are first routed through U15, which translates the high logic level from +11V (used in the VPR-2/2B control panel) to +5V.

All inputs to input data buffers are pulled up through resistor networks RN1—RN4. The A4 input to U4 is an exception. See paragraph 8-10.

A logic low at the A1 input to buffer U1 indicates to the control system CPU that the VPR-80 is equipped with the accessory Parallel Remote PWA. A floating high at this input indicates that the Parallel Remote PWA is not installed.

Note that the 8Q output of output data latch U2 is brought back to the A8 input of input data buffer U4. This connection provides a communication test path for the control system CPU 6U10. CPU 6U10 writes test bit RD7 to latch U2. On the next read transfer it checks for presence of the test bit at the Y8 output of buffer U4. If the test bit is not there, fault indication **105-02** is brought up for display. As long as parallel remote operation is selected, this communications check is made at frame rate during the background program.

8-8 Output Data Latches

Output data latches U9, U5, and U2 take indicator on/off logic levels from the CPU via the remote data bus and hold this information until updated information is

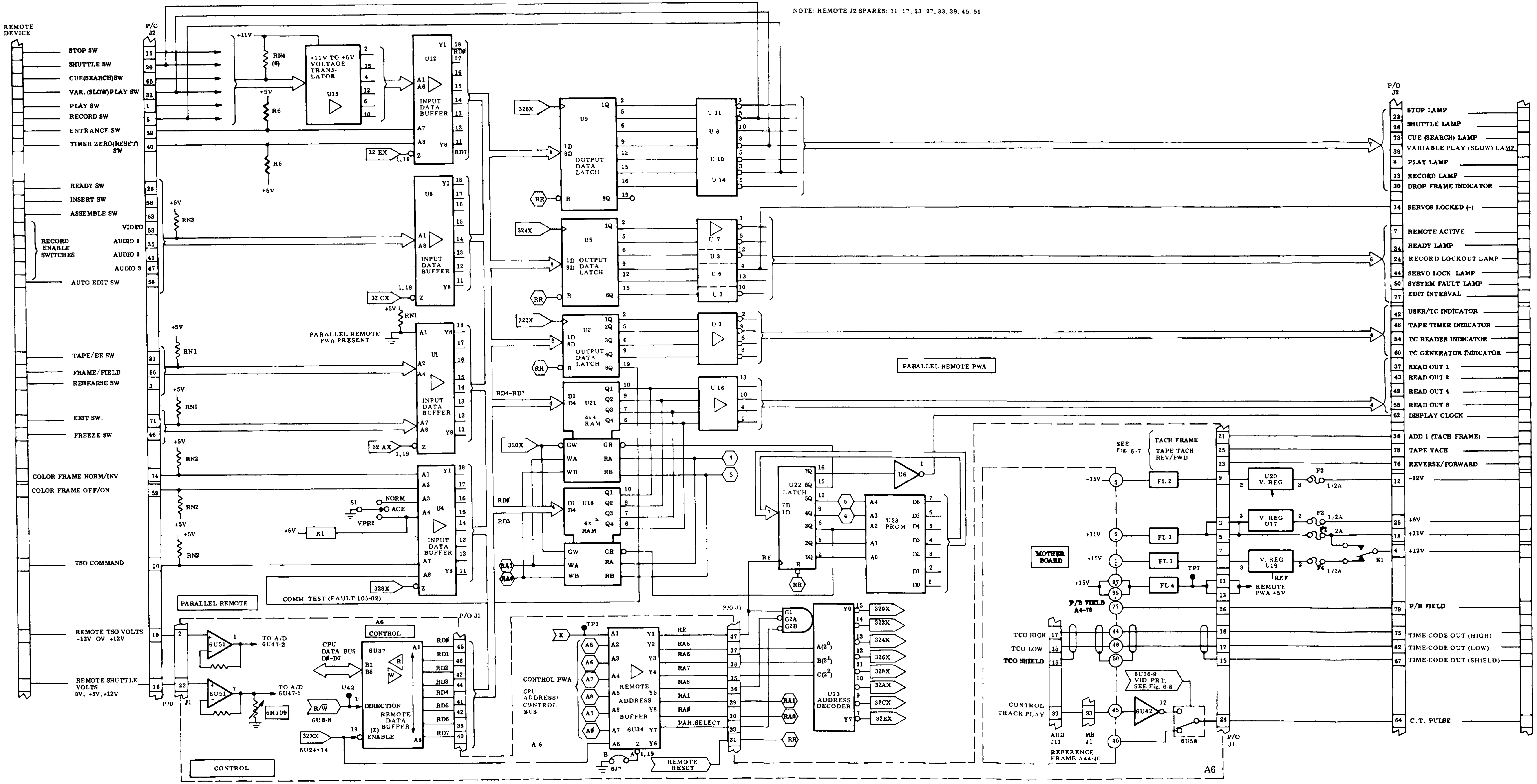


Figure 8-1. Parallel Remote PWA Block Diagram

Table 8-2. Parallel Remote PWA Decoded Addresses

Address	Source	Remarks
320X	U13-15	Write input to register file U18/U21. Write display data 1-2-4-8 from CPU.
322X	U13-14	Clocks ODL U2. Outputs: USER/TC, TAPE TIMER, and TCR/TCG remote indicators.
324X	U13-13	Clocks ODL U5. Outputs: remote active, READY, REMOTE LOCKOUT, SERVO LOCK, FAULT (SYSTEM) indicators, edit interval.
326X	U13-12	Clocks ODL U9. Outputs: STOP, SHUTTLE, CUE, VAR PLAY, PLAY, RECORD, and DROP FRAME indicators.
328X	U13-11	Enables IDB U4. Inputs: CLR FMR ON/OFF, CLR FMR normal/INVERT, normal/ACE/VPR-2, and TSO switches.
32AX	U13-10	Enables IDB U1. Inputs: TAPE/EE, FRAME/FIELD, REHEARSE, EXIT, and FREEZE switches.
32CX	U13-9	Enables IDB U8. Inputs: READY, INSERT, ASSEMBLE, VIDEO, A1–A3 RECORD ENABLE, and AUTO EDIT switches.
32EX	U13-7	Enables IDB U12. Inputs: STOP, SHUTTLE, CUE (search), VAR PLAY, PLAY, and RECORD switches.

received from the control system. Latch outputs are routed through open collector gates, line drivers, and the PARALLEL REMOTE connector to the remote control device.

Note that SHUTTLE, VAR PLAY, and RECORD indicator outputs of output data latch U9 are brought back and fed into corresponding switch inputs to level translator U15. Thus, switch ON commands provide a sealed-in ground path for the corresponding indicator.

8-9 Display Drive

The remote 8-digit numeric display of tape time (or time code) is driven by buffered 1-2-4-8 outputs of register files U18 and U21. The display clock is provided by the buffered 7Q output of latch U22.

Register files U18 and U21 each store four 4-bit words, and each file functions as a 4 x 4 random-access memory (RAM). When the CPU writes time information into them, U18 and U21 are enabled in parallel by decoded address 320X. U18 stores remote data bits RD0—RD3, and U21 stores RD4—RD7. The storage location is accessed by internal decoders to which address bits RA0 and RA1 are applied. Four-bit time words are read out of U18 and U21 under control of PROM U23.

PROM U23 is a 32-byte storage chip. In this application, only 7 bits of each byte are used. The 7-bit output words are presented in parallel to D inputs of 7-bit D latch U22. Five of the latch Q outputs are brought around to the 5-bit address input of PROM U23. These 5 bits of the last 7-bit word clocked to Q outputs of U22 are the PROM address of the next 7-bit word to appear at Q outputs of latch U22. Since U22 is clocked by RE, the PROM is repetitively cycled through its sequence of 7-bit outputs at 1 MHz.

The 7Q output of latch U22 is buffered and furnished as clock to the remote display. The clock frequency is 250 kHz. The 6Q output of U22 enables RAM U21, and the 3Q output enables RAM U18. The 4Q and 5Q outputs of U22 are applied in parallel to read address decoders in U18 and U21. Thus, outputs of latch U22, under control of the address sequence stored in PROM U23, continuously send 4-bit data to the remote display, accompanied by 250-kHz display clock.

The jumper connection at the chip select input of PROM U23 (shown in Figure 8-22) is for factory test purposes only. This jumper must be left in place.

A simplified diagram of the VPR-2/2B remote numeric display is shown in Figure 8-2. The display is essentially composed of eight hexadecimal display modules (Ampex Part No. 581-525), an 8-bit parallel-out serial shift register, and a one-shot with Schmitt-trigger input which acts as pulse detector.

The 8-4-2-1 remote readout (BCD) word is applied to all eight digit display modules in parallel. Each display module contains a latch memory to which the BCD time word is applied, an LED matrix (display), a matrix decoder, and an LED matrix driver. Display modules decode positive 8-4-2-1 BCD inputs into decimal digits 0—9 and four blanks for invalid BCD states. Module internal circuits are diagrammed on the right-hand side of Figure 8-2.

Display clock pulses are applied to pulse-detector one-shot and the 8-bit shift register. The 250-kHz clock is a square wave with the exception of every eighth pulse, which synchronizes the display. Display clock input and pulse detector and shift register output waveforms are shown in Figure 8-3. The low pulse detector output pulse width is approximately 1.8 µs. The shift register is clocked on positive-going trailing edges. The display clock is the shift enable input to the register, and it must be high when pulse detector output goes high, to enable a shift. The pulse detector one-shot times out after the 1-µs display clock sync pulse has gone low. This puts a low into the register which is shifted through to load the BCD time data into each display module. Thus, the 1-µs display clock sync pulse synchronizes the display on the QA (frames x 10) output of the shift register.

8-10 Mode Switch

Parallel Remote PWA mode switch S1, shown in Figure 8-1 and Figure 8-22, has three positions: NORMAL, ACE, and VPR-2 REMOTE PANEL. The position of the mode switch determines which logic levels are seen by the control system CPU at the A3 and A4 inputs of input data buffer U4. States of these bits govern methods of color framing and control track lock. For example, the two methods of color framing are shortest distance and retard only. With the mode switch in the ACE position (A3 and A4 inputs to U4 both high), the shortest distance method is used. In other mode switch positions, the retard only method is used.

The mode switch also controls some power supply switching. When the mode switch is in the VPR-2 REMOTE PANEL position, relay K1 is pulled up. This action disconnects regulated +12V output to the remote panel, and switches in a supply of unregulated +11V, fused at 2A. The VPR-2/2B remote control panel and the SMC-100 slow-motion controller require in excess of 1 Amp of +11V. They also use +11V as a source for their +5V regulators. The ACE system uses the regulated +12V for its tape speed control and tape speed override (TSO) analog outputs.

8-11 Other Remote I/O Signals

As shown in Figure 8-1, the Parallel Remote PWA serves only as a conduit for several I/O signals (both digital and analog). These signals are: playback field, TSO speed, tape speed control (shuttle pot) voltage, control track pulse, add 1 remote (tach frame), remote tape tach, forward/reverse direction, TCO high, low, and shield.

8-12 Removal/Installation

Removing the Parallel Remote PWA from the VPR-80, and reinstalling it, are straightforward.

8-13 Removal

Remove the Parallel Remote PWA as follows:

STEP 1 Loosen, but do not remove, seven decorative gray screws at rear of VPR-80 cabinet indicated in Figure 8-4.

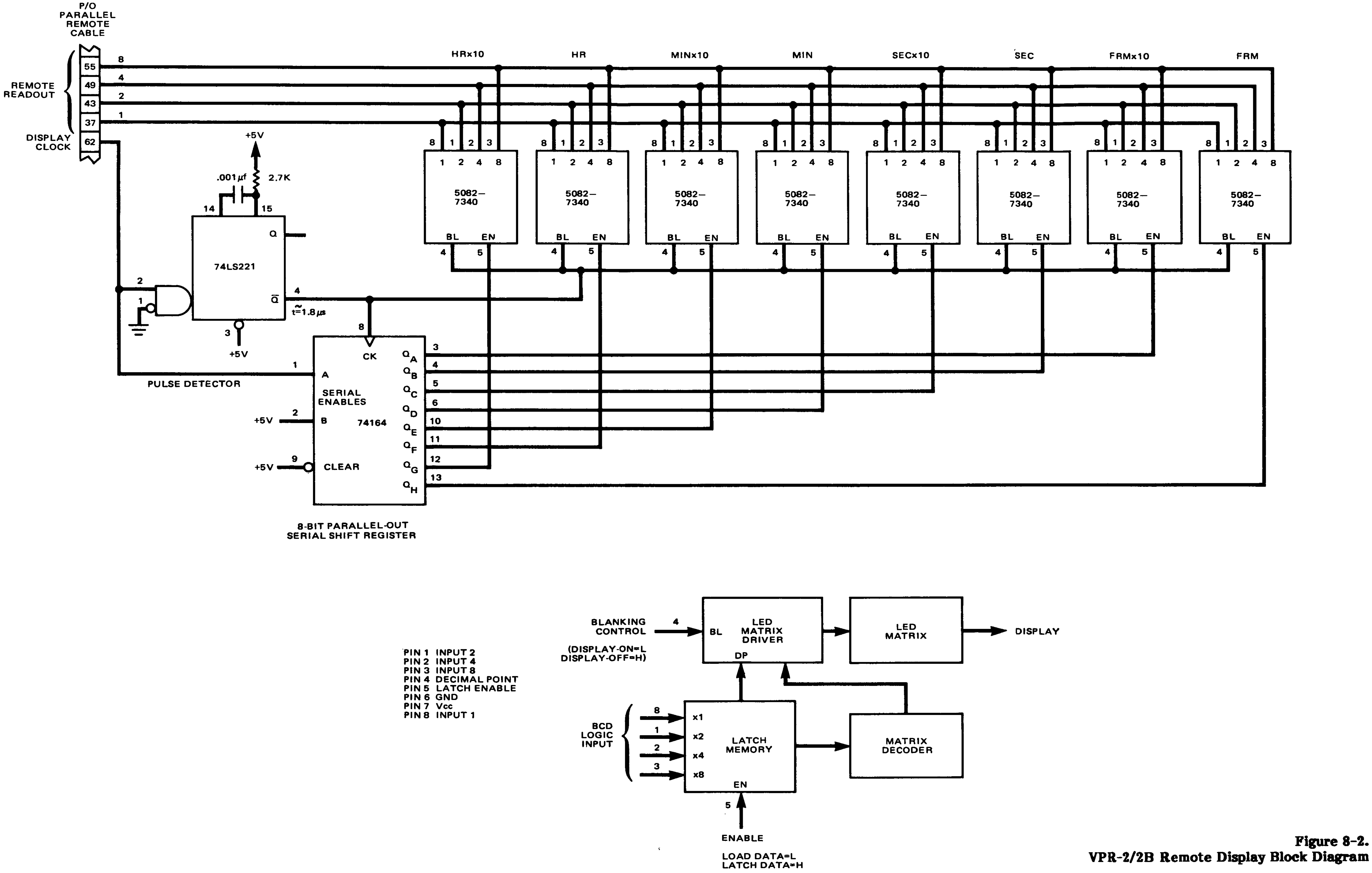
STEP 2 With VPR-80 power off, open rear-door assembly as shown in Figure 8-5.

STEP 3 Open top access door and remove PWA-edge-to-PWA-edge cable assembly (Ampex Part No. 1450783-AA) between Control and Parallel Remote PWAs.

STEP 4 Remove AST Servo, Servo, and Control PWAs.

STEP 5 Remove seven gray screws (Figure 8-4) and detach Parallel Remote PWA.

STEP 6 Reinstall Control, Servo, and AST Servo PWAs.



PIN 1 INPUT 2
PIN 2 INPUT 4
PIN 3 INPUT 8
PIN 4 DECIMAL POINT
PIN 5 LATCH ENABLE
PIN 6 GND
PIN 7 Vcc
PIN 8 INPUT 1

Figure 8-2.
VPR-2/2B Remote Display Block Diagram

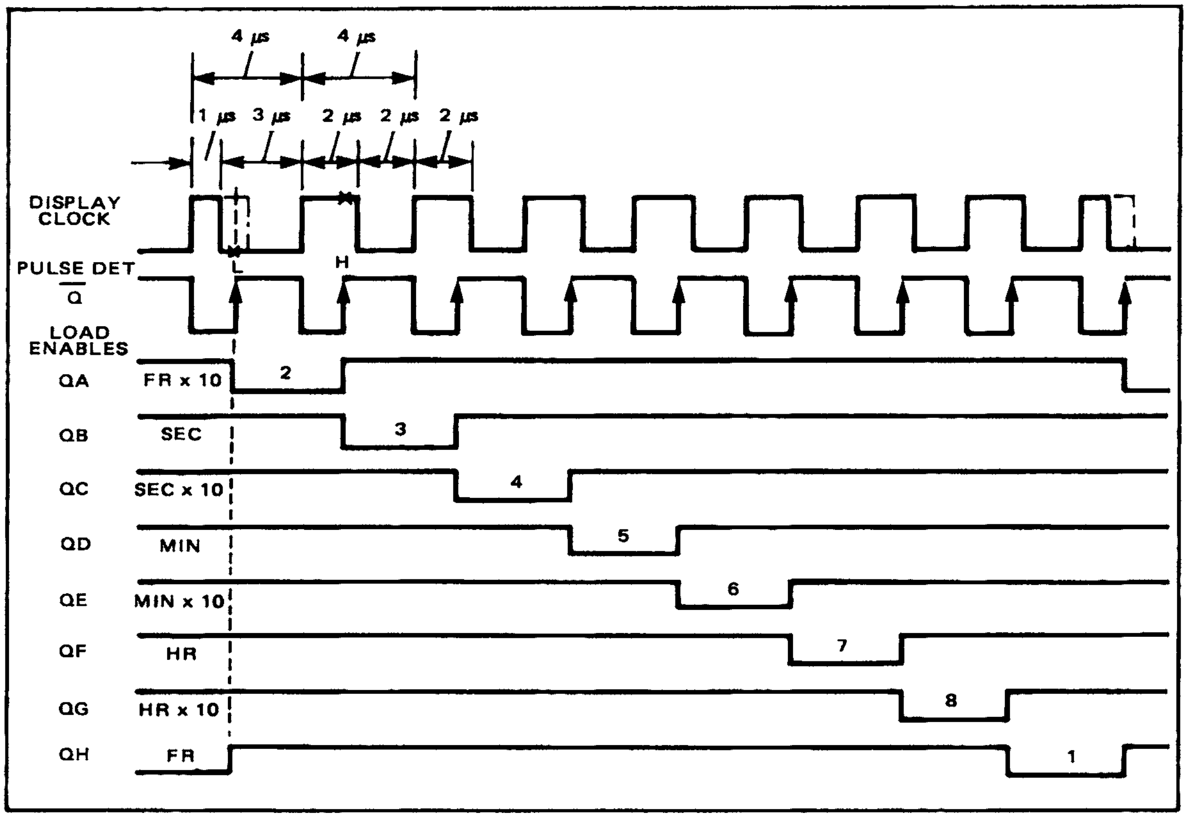


Figure 8-3. VPR-2/2B Remote Display Timing Diagram

8-14 Installation

Install Parallel Remote PWA as follows:

STEP 1 With VPR-80 power off, open rear-door assembly as shown in Figure 8-6.

STEP 2 Open top access door and remove AST Servo, Servo, and Control PWAs.

STEP 3 Ensure that jumper J3 and four fuses, F1—F4, are installed on the Parallel Remote PWA. See Figure 8-22.

STEP 4 Align connector J2 with cutout in rear panel of the VPR-80 cabinet.

STEP 5 Loosely attach Parallel Remote PWA to rear panel of VPR-80 cabinet with one 6-32 decorative gray screw (Ampex Part No. 473-895) on each side of connector J2.

STEP 6 Install and tighten five decorative mounting screws which thread into standoffs on Parallel Remote PWA. Then tighten two screws installed in step 5.

STEP 7 Reinstall Control, Servo, and AST Servo PWAs.

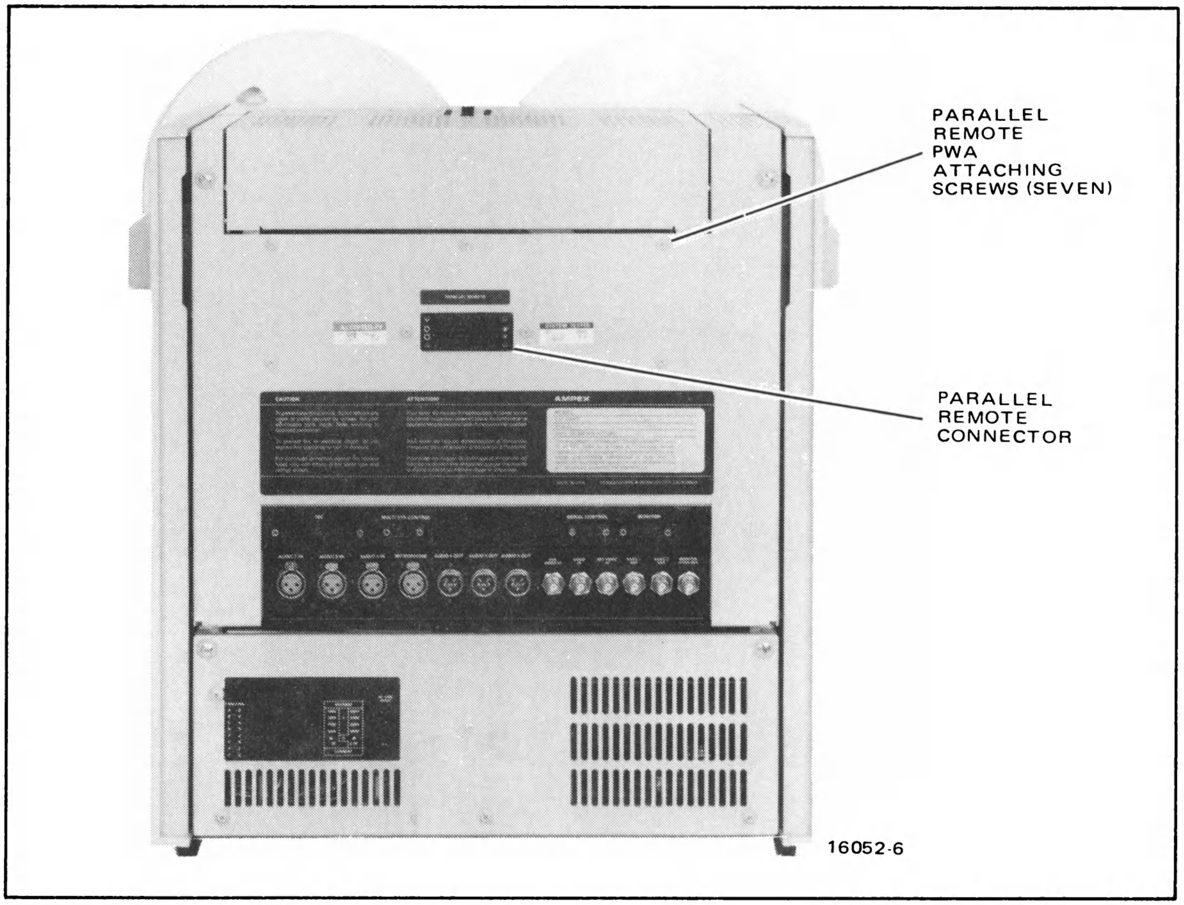

PARALLEL REMOTE PWA ATTACHING SCREWS (SEVEN)
PARALLEL REMOTE CONNECTOR
16052-6

Figure 8-4. VPR-80 Cabinet Rear View—Removing and Installing Parallel Remote PWA

STEP 8 Install PWA-edge-to-PWA-edge cable assembly (Ampex Part No. 1450783-AA), shown in Figure 8-7, between Control and Parallel Remote PWAs.

Note

Cable assembly 1450783-AA is composed of 50 pairs of contacts wired straight across from one connector to the other. Therefore, no key or keyway is provided, and the cable assembly can be installed in either direction with satisfactory results.

8-15 Remote Shuttle Control Calibration

Setup code 20 enables the technician to read the remote shuttle control voltage on the VPR-80 primary control panel. With remote shuttle control in the center detent (shuttle stop) position, he can then adjust remote shuttle input to the A/D converter (on the Control PWA) to half scale.

Calibrate remote shuttle control output voltage as follows:

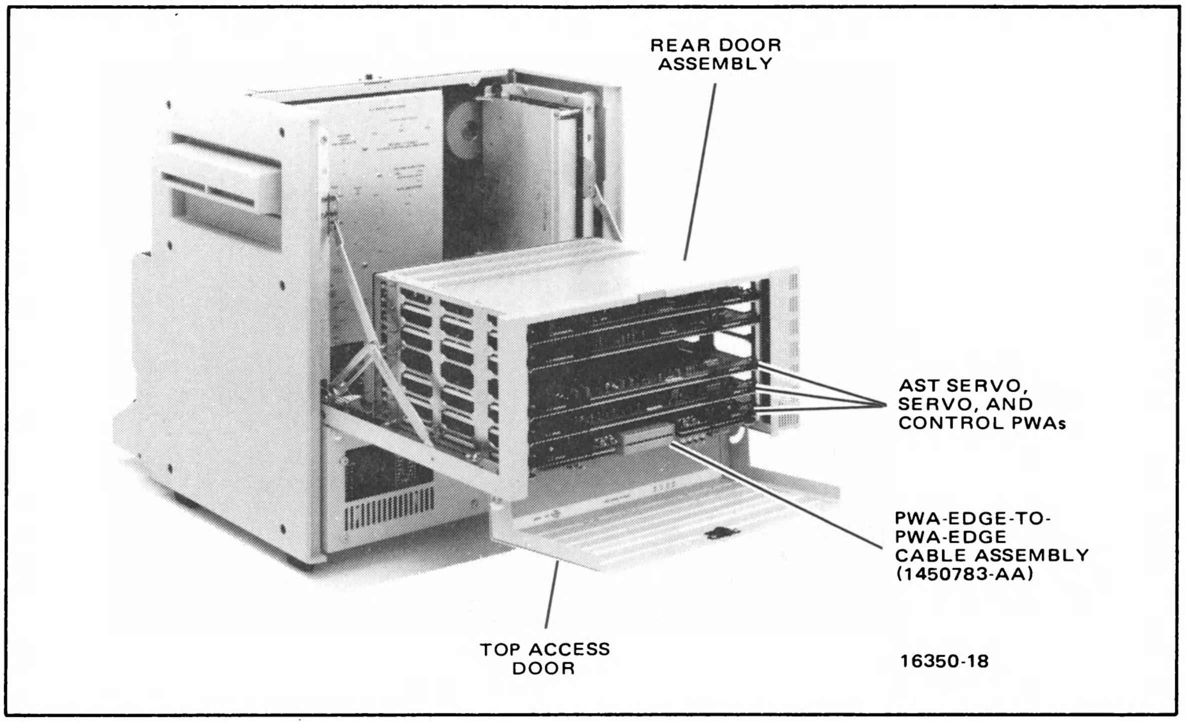

REAR DOOR ASSEMBLY
AST SERVO, SERVO, AND CONTROL PWAs
PWA-EDGE-TO-PWA-EDGE CABLE ASSEMBLY (1450783-AA)
TOP ACCESS DOOR
16350-18

Figure 8-5. Removing Parallel Remote PWA

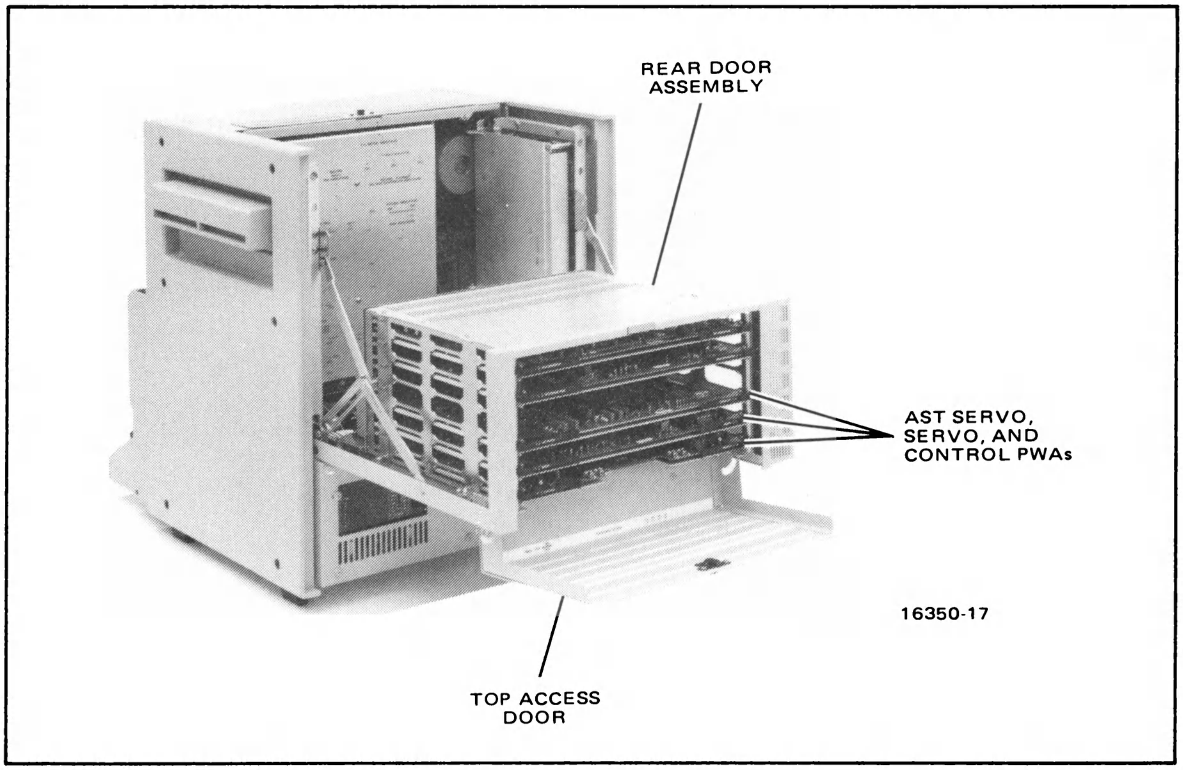


Figure 8-6. Installing Parallel Remote PWA

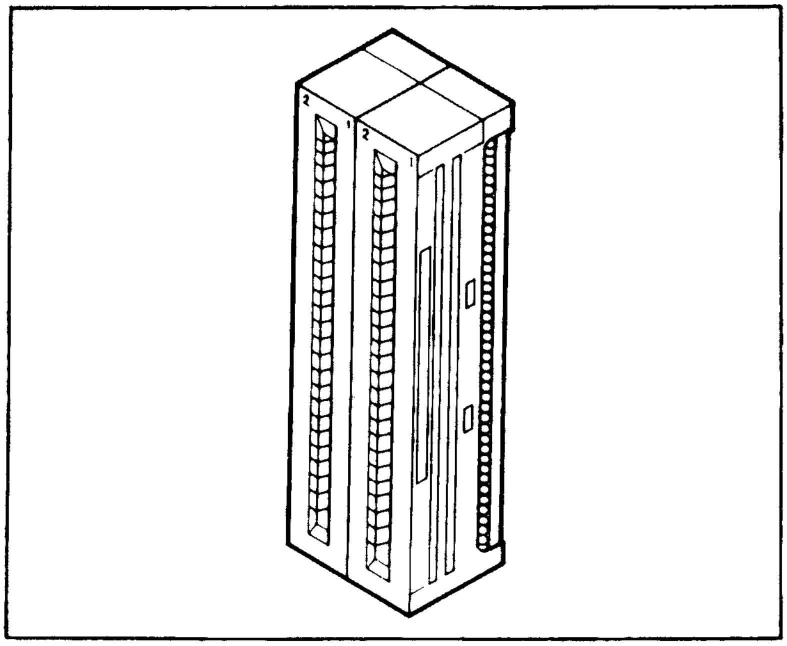


Figure 8-7. PWA-Edge-to-PWA-Edge Cable Assembly

STEP 1 Turn on VPR-80 power and press SETUP.

STEP 2 Enter 20 on keypad numeric switches.

STEP 3 Press ENTER. Timer display will show eight hexadecimal (hex) digits which are identified in Figure 8-8.

Remote shuttle control voltage is indicated by the two hex digits on the right. The 0V to -12V value is divided into 256 binary increments. Thus, the displayed range is **00-FF** (hex), where **80** (hex) represents half-scale voltage.

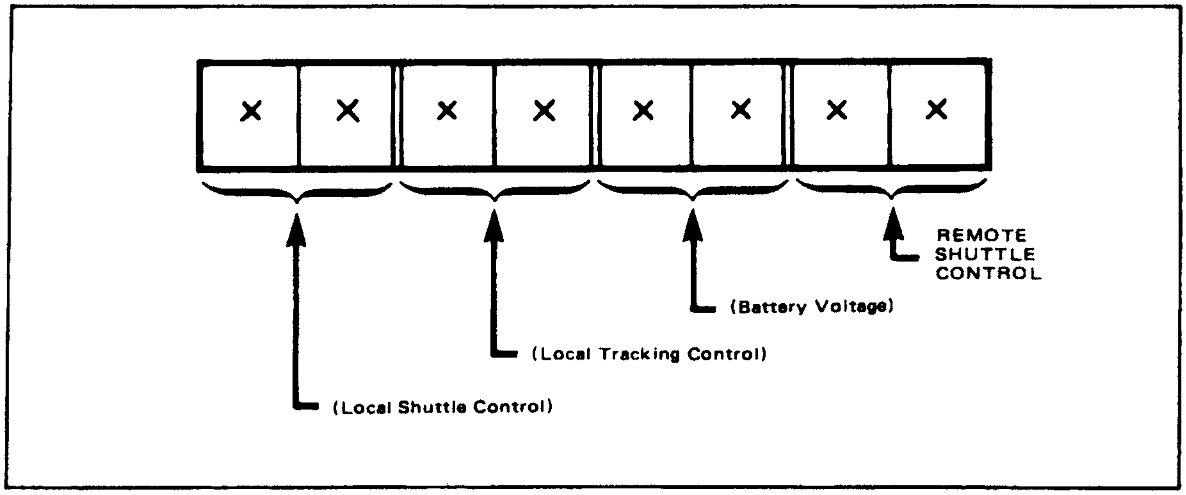


Figure 8-8. Setup Code 20 Display—Remote Shuttle Voltage

STEP 4 Turn shuttle control on remote control panel to the center detent (shuttle stop) position.

STEP 5 Adjust R109 on Control PWA for an indication of **XXXXXX80** on the tape time display. See Figure 8-8 and Figure 8-23.

STEP 6 Press alternate action SETUP switch to exit setup mode.

8-16 SERIAL REMOTE PWA

The Serial Remote PWA enables the VPR-80 to be incorporated in a serial communications network such as the Ampex Computerized Editing (ACE) system. With serial communication capability the VPR-80 can be controlled by any device that conforms to electrical and mechanical characteristics described in proposed American Standard PH22.207M*. In the following discussions such a device is referred to as the bus controller. Protocol is specified in proposed SMPTE Recommended Practice RP 113**.

All I/O connections between the Serial Remote PWA and the Bus Controller are made via the SERIAL CONTROL connector (J4) on the I/O connector panel. Connector pin assignments are shown in Table 8-3. Information is exchanged with the Bus Controller by full-duplex, four-wire communication (a dedicated pair of wires for each direction). Communication is bit-serial at 38.4K Baud. Each character is composed of one start bit (SPACE), eight data bits, one (odd) parity bit, and one stop bit (MARK).

Table 8-3. Serial Control Connector Pin Assignments

Pin No.	Signal
2	Serial Control Transmit A
3	Serial Control Receive B
7	Serial Control Transmit B
8	Serial Control Receive A
1,6,4,9	Ground
5	Not used

All communication between the Serial Remote PWA and the Control PWA is through the card cage motherboard.

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*Proposed American Standard PH22.207M: "Electrical and Mechanical Characteristics for Digital Control Interface"

**Proposed SMPTE Recommended Practice RP 113: "Supervisory Protocol for Digital Control Interface"

Simple remote control and inputs from parallel and serial remote control accessories are enabled by the REM 1 switch on the primary control panel. The following setup procedure determines which source of remote 1 input is enabled. Select serial remote operation as follows:

STEP 1 Press SET UP. SET UP indicator lights.

STEP 2 Press keypad switch 2.

STEP 3 Press ENTER. Display indicates the enabled remote 1 input.

- If **2-1** is displayed, simple remote control is enabled.
- If **2-2** is displayed, Parallel Remote PWA is enabled.
- If **2-3** is displayed, Parallel Remote PWA (with color framer forced on) is enabled.
- If **2-4** is displayed, Serial Remote PWA is enabled.

STEP 4 Press keypad switch 4 to enable serial remote control.

STEP 5 Press ENTER. Display is changed to **2-4.**

STEP 6 Press SET UP to exit setup mode.

In addition, the individual VTR must be assigned an identification number by which the bus controller can address it. The identification number is established as follows:

STEP 1 Press SET UP. SET UP indicator lights.

STEP 2 Enter 13 on the keypad. (If an identification number has been previously assigned to the VTR, it will appear on tape time display.)

STEP 3 Enter VTR identification number (any four-digit decimal number from 0001 to 9999) on the keypad.

STEP 4 Press ENTER. New VTR identification number, as selected in step 3, appears on tape time display.

STEP 5 Press alternate action SET UP switch to exit setup mode.

8-17 Theory of Operation

Serial Remote PWA logic is composed of a microprocessor, a dual asynchronous receiver/transmitter (DART), two 32 x 8 first-in/first-out (FIFO) shift registers, serial line drivers and receivers, and the control system interface. Regulated +5 Vdc is supplied to all components on the Serial Remote PWA via motherboard power distribution (PWA connector contacts 97—100). The Serial Remote PWA is block-diagrammed in Figure 8-9.

In the following discussions, component reference designations on the Control PWA are prefixed with 6. Component reference designations on the Serial Remote PWA are not prefixed. It should also be noted that the terms "read," "write", "input," and "output" are used with respect to the control system CPU.

8-18 Microprocessor

Serial Remote PWA control logic consists of microprocessor (CPU) U23, crystal oscillator U28, PROM U20, RAM U22, and address decoders U21 and U16.

The Serial Remote PWA microprocessor is a Zilog Z80 CPU. Internal architecture and instruction are more than adequately documented by the manufacturer, and consequently are not provided in this manual. However, complete details of all the Z80 I/O signal characteristics are given in Appendix A of the *VPR-80 Parts Lists and Schematics* manual. In this application, the CPU low-active WAIT and bus request (BUSRQ) inputs are held high through R9 and R10. The HALT, refresh (RFSH), and bus acknowledge (BUSAK) output are unused.

Green LED indicator DS1 (see Figure 8-24) blinks to indicate that the CPU program is running and that timing inputs supplied by reference vertical and reference frame are being received.

8-19 Clock, Reset, and Interrupt Inputs. The CPU clock is supplied by 2.4576-Mhz crystal oscillator U28. This is a single-phase clock which is also supplied to dual asynchronous receiver/transmitter (DART) U24 to achieve 38k-Baud communications.

When system reset is asserted by the control system CPU, the low output of inverter U25-6 resets CPU U23. It initializes the CPU and forces the CPU program counter to zero. During the time reset is asserted, data and address bus outputs go to a high-impedance state.

The interrupt (INT) input is low-active. It is asserted by DART U24. When the CPU recognizes interrupt at the end of the current instruction, it sends input/output request (IORQ) which enables the I/O section of dual address decoder U21. The decoder then asserts chip enable to the DART. See paragraph 8-32.

Nonmaskable interrupt (NMI) input is negative edge-triggered. It is a higher priority interrupt than INT and it is always recognized at the end of the current instruction. NMI is asserted regularly by reference vertical pulses from the AST Servo PWA. See paragraph 8-32.

8-20 R/W, I/O and Memory Request, and M1 Outputs. Memory read (RD) and write (WR) are tristate low-active outputs. RD is asserted when the CPU is ready to read information from DART U24. RD enables DART information output. WR is asserted when the CPU is ready to write information in RAM U22. WR enables information to be written into the RAM.

Input/output request (IORQ) is a tristate low-active output. The CPU asserts IORQ in response to INT from DART U24. IORQ enables the I/O section of dual address

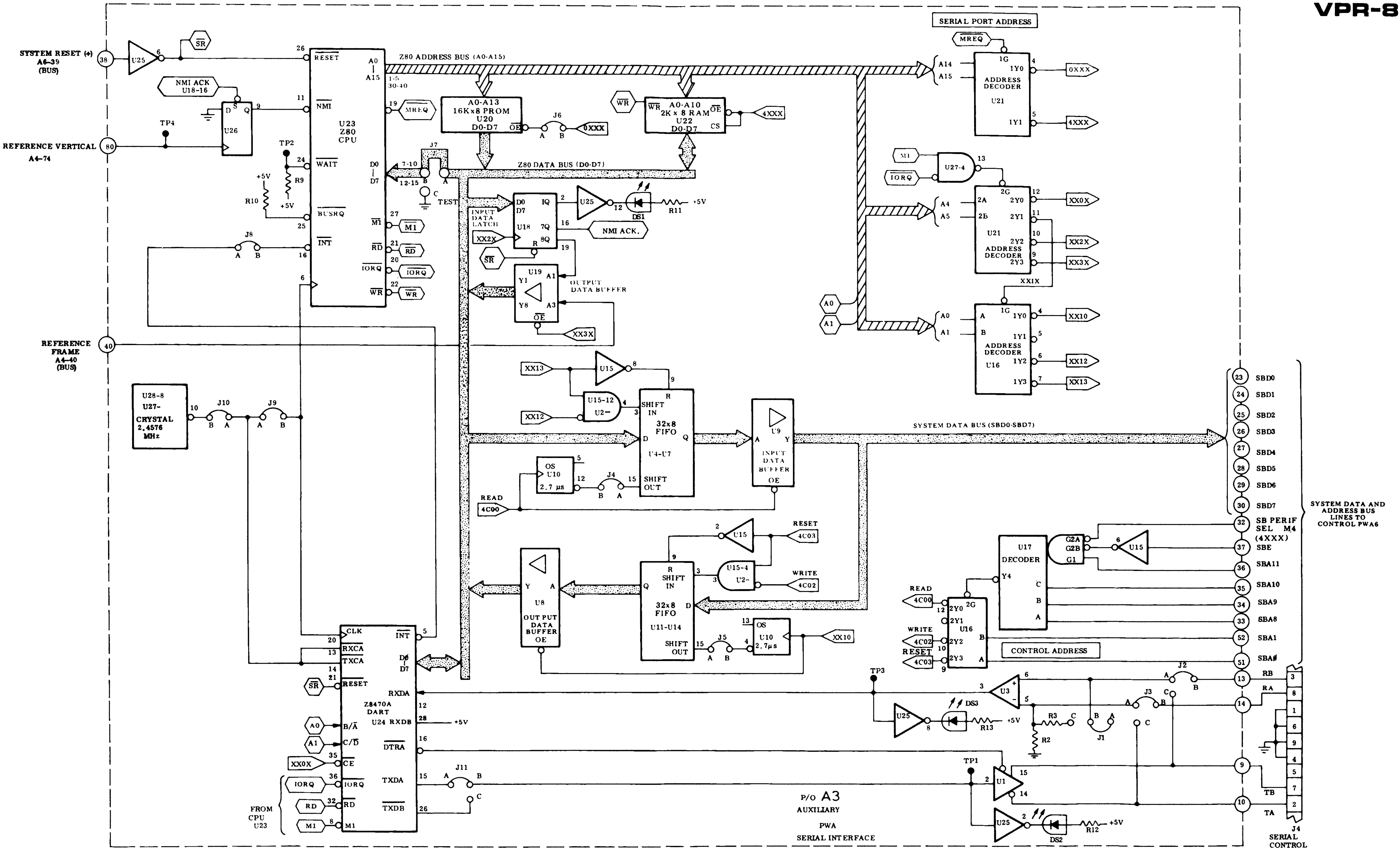


Figure 8-9.
Serial Remote PWA Block Diagram

decoder U21, which, in turn, enables the DART to put information from the Bus Controller on the Z80 data bus to the CPU.

Memory request (MREQ) is a tristate low-active output. When asserted, it indicates that the word on the Z80 address bus is valid for a memory read or write transfer. MREQ enables the memory section of dual address decoder U21. The decoder output then enables information exchange between the CPU and RAM U22 or PROM U20.

The machine cycle one (M1) output is tristate and low-active. M1 indicates that the machine (CPU) is in the op code fetch cycle of an instruction execution. M1 is also asserted with IORQ to indicate an interrupt acknowledgment.

8-21 Data Bus. The CPU 8-bit, bidirectional data port (D0—D7) is tristate and high-active. Information is exchanged on the Z80 data bus between the CPU and memory (RAM or PROM) and I/O devices (DART, output data buffers, FIFOs, or input data latch).

8-22 Address Bus. The CPU 16-bit address port (A0—A15) is tristate and high-active. The word on the Z80 address bus is validated by the CPU output of IORQ or MREQ to address decoder U21.

8-23 Memory

CPU U23 is supplied with two classes of external memory: 16K x 8-bit EPROM U20 and 2K x 8-bit static RAM U22. Information exchanges between the CPU and memory (RAM or PROM) are initiated by the assertion of MREQ to address decoder U21.

The contents of PROM U20 are accessed by addresses 0000—3FFF (hex). The only control input employed is the low-active output enable at pin 22. Assuming that the address word is stable, data can be accessed from PROM storage in 350 ns, and access time from output enable is 150 ns. The output enable is 0XXX from address decoder U21. See paragraph 8-29.

Addresses in RAM U22 range from 4000 to 47FF (hex). Two I/O controls are used for writing to or reading from RAM storage. Information can be written in RAM U22 when the WR output of the CPU is asserted (low). Information can be read out of the RAM when WR is high, and when the read output is enabled by decoded address 4XXX from U21. See paragraph 8-29.

8-24 Dual Asynchronous Receiver/Transmitter

The DART (U24) accepts serial commands and data from the Bus Controller and transmits status information when commanded. All information transfers are made using DART channel A. The use of channel B is reserved.

Each character consists of a start bit (ZERO condition), 8 information bits, followed by an odd parity bit, if required, and a stop bit (ONE condition). Each bit in a character is of equal time duration with the exception of the stop bit, which can be up to twice as long as other bits in the character.

When receiving, the DART recognizes the initial change of state from the ONE condition as the start of a data character. It then looks at the line at time intervals corresponding to the middle of each of the following information bits in order to transfer a complete data character into its internal receive shift register. The 8 information bits are then placed on the data bus for interpretation by CPU U23. The DART requests service by asserting INT (low). After the interrupt acknowledge process has occurred, the service routine reads data from the receive data register and interprets it.

The Serial Remote PWA transmits status information in a variable-length string. This string is taken in parallel from the Z80 data bus when CPU U23 asserts IORQ (low) and address decoder U21 asserts XX0X, which is the DART chip enable. The DART begins the transmission by setting the start bit low while generating the parity bit, as necessary. It then serially shifts out the string in 8-bit words (bytes) plus parity bit, and concludes the character by setting the stop bit high. If status transmission requires additional characters, the process is repeated without a break. When transmission is completed, the TxDA line out is held high (continuous stop bits).

8-25 Clock, Reset, Serial Data, and Control Inputs. DART operation is clocked by the same 2.4576-Mhz oscillator (U28) that clocks the CPU. Buffered and inverted oscillator output is applied to the CLK input for synchronization of the internal control logic. It is also applied to the channel A receiver clock input (RxCA) and the channel A transmitter clock input (TxCA). Received data is sampled on the rising edge of RxCA. The TxCA input is Schmitt-triggered. Transmitted data bits change on the falling edge of TxCA.

The DART is reset, in parallel with the CPU, by inverted and buffered system reset input. When in reset condition, the transmitter (TxDA) and receiver (RxDA) are both disabled, modem control (DTRA) is forced high, and interrupt (INT) generation is disabled.

The channel A receive data serial input port (RxDA) is high-active. The two-wire input from the Bus Controller is converted to single-ended by line receiver U3-3.

The channel A or B select input (B/A: B = high, A = low) defines which channel is accessed during a data transfer between CPU U23 and DART U24. In this application, channel B is not used.

The control or data select input specifies the type of information (C/D: control = high, data = low) transferred on the Z80 data bus between CPU U23 and DART U24.

The chip enable (CE) input is low-active, and is address XX0X from decoder U21.

Input/output request (IORQ) is a low-active input from CPU U23. IORQ is used in conjunction with B/A, C/D, CE, and RD to transfer commands and data between CPU U23 and DART U24.

Read cycle (RD) is a low-active input from CPU U23. It is active when the CPU is reading information from the DART. If RD and M1 are both active, the CPU is fetching an instruction from memory.

Machine cycle one (M1) is a low-active input from CPU U23. It is used with RD (above) and IORQ. When M1 and IORQ are both asserted, DART U24 accepts this as interrupt (INT) acknowledgment.

8-26 **Serial Data and Interrupt Outputs.** The channel A transmit data serial output port (TxDA) is high-active. The TxDA output is converted to two-wire output by line driver U1-14/15.

The channel A data terminal ready (DTRA) output is low-active. The DTRA output is applied to enabling input of line driver U1-14/15.

Interrupt (INT) is an open-drain, low-active output. DART U24 pulls INT low when requesting an interrupt of CPU U23.

8-27 **Data Bus.** The DART 8-bit, bidirectional data port (D0—D7) is tristate and high-active. Information is exchanged on the Z80 data bus between the DART and CPU U23.

8-28 Data and Address Buses

There are two data buses on the Serial Remote PWA: the Z80 data bus, and a small portion of the system data bus. This is also true for the address bus structure. Addresses from CPU U23 are carried on the Z80 address bus to peripherals. Part of the system address/control bus is applied to secondary decoder U17 and third level decoder U16.

The Z80 8-bit data bus is the bidirectional path for information exchanges between CPU U23 and DART U24, PROM U20, RAM U22, read FIFO U4—U7, output data buffers U19 and U8, and input data latch U18.

The 8-bit system data bus interfaces with the Serial Remote PWA logic at input data buffer U9 and write FIFO U11—U14.

The Z80 address bus is the path for address information from CPU U23 to DART U24, RAM U22, PROM U20, and decoders U21 and U16.

The system address/control bus interface is discussed in paragraph 8-31.

8-29 Address Decoding

Chips U21 and U16 each contain two 2 x 4 address decoders. The 1Y0—1Y3 outputs of U21 (decoded bits A14 and A15 on the Z80 address bus) are enabled by MREQ from the CPU. The 2Y0—2Y3 outputs of U21 (decoded bits A4 and A5 on the Z80 address bus) are enabled by IORQ from the CPU. The 1Y0—1Y3 outputs of U16 (decoded bits A0 and A1 on the Z80 address bus) are enabled by decoded address XX1X from U21. Table 8-4 lists the functions of these decoded addresses.

Table 8-4. Serial Remote PWA Decoded Addresses

Address	Source	Remarks
0XXX	U21-4	Output enable to PROM U20
4XXX	U21-5	Chip select and output enable to RAM U22
XX0X	U21-12	Chip enable to DART U14
XX1X	U21-11	Enables one-half of decoder U16 (XX10, XX12, and XX13)
XX2X	U21-10	Clock to input data latch U18
XX3X	U21-9	Enables output data buffer U19
XX10	U16-4	Enables output data buffer U8 and triggers one-shot U10-4
XX12	U16-6 (U2-4)	Shift (in) clock to read FIFO U4–U7
XX13	U16-7	Reset and shift (in) clock to read FIFO U4–U7

The 2Y0—2Y3 outputs of U16 (decoded bits SBA0 and SBA1 on the system address bus) are enabled by decoded address 4CXX from U17. The 4CXX decoded addresses are explained in detail in paragraph 8-31.

8-30 Control and Timing

8-31 Control System Interface. Whereas communication between Control and Parallel Remote PWAs is carried on special purpose remote data and address buses, the control system CPU accesses the Serial Remote PWA as a peripheral. Accordingly, information transfers between the Serial Remote PWA and the control system CPU are made via system data and address/control buses in the motherboard.

When information is transferred, decoded address M4 (PERIF SELECT) enables bidirectional machine data buffer 6U28. This connects the Control PWA data bus to the system data bus. Direction of transfer is controlled by the logic level of the R/W output of the control system CPU. (Refer back to Figure 6-2 in Section 6.) At the same time, an address word composed of bits SBA0, SBA1, SBA8—SBA11, enabling strobe SBE, and SB PERIF SEL is placed on the system address/control bus through permanently enabled machine address buffer 6U29.

As shown in Figure 8-9, SB PERIF SEL (low), SBA11 (high), and SBE (high) enable secondary address decoder U17. SB PERIF SEL is decoded address 4XXX in hexadecimal (hex) notation. Address bits SBA8—SBA10 are decoded by U17. When the latter three bits form a hex 4, the Y4 output of decoder U17 (4CXX) enables third level decoder U16. Decoder U16 looks at address bits SBA0 and SBA1 and decodes one of three primary instructions from the control system CPU to the Serial Remote PWA logic: read, write, or reset. These instructions are listed in Table 8-5.

Table 8-5. Control Interface Addresses

Decoded Address	Mnemonic	Source	Remarks
4CXX	--	U17-11	Enables address decoder U16.
4C00	READ	U16-12	Enables input data buffer U9 and shifts SBD0–SBD7 from Z80 data bus to system data bus.
4C02	WRITE	U16-10	Shifts SBD0–SBD7 from system data bus into FIFO registers U11, U12, U13, and U14.
4C03	RESET	U16-9	Resets FIFO registers U11, U12, U13, and U14.

When system reset is asserted by the control system CPU, the low output of inverter U25-6 resets serial remote CPU U23, DART U24, and input data latch U18.

8-32 Timing. The reference pulse generator on the AST Servo PWA (Figure 5-9 in Section 5) supplies two timing inputs to the Serial Remote PWA: reference vertical and reference frame.

The reference vertical input causes a regular nonmaskable interrupt (NMI). The reference vertical input clocks flip-flop U26-9 to reset state, and the low flip-flop Q output applies NMI to CPU U23. The flip-flop is returned to the set state by the NMI ACK output of input data latch U18.

The reference frame input is applied to the A3 input of output data buffer U19. When U19 is enabled by the XX3X output of decoder U21, CPU U23 looks at the logic level of the reference frame data bit (Y3 output), thereby identifying the current field period.

Figure 8-10 shows timing of communication between the Serial Remote PWA and the control system CPU, and between the Serial Remote PWA and the Bus Controller.

Communication with the control system CPU occurs within the first 3 ms of each field period. The direction of communication alternates with each reference vertical (NMI) input. Communication to the control system CPU occurs when NMI is accompanied by reference frame at the Y3 output of output data buffer U19.

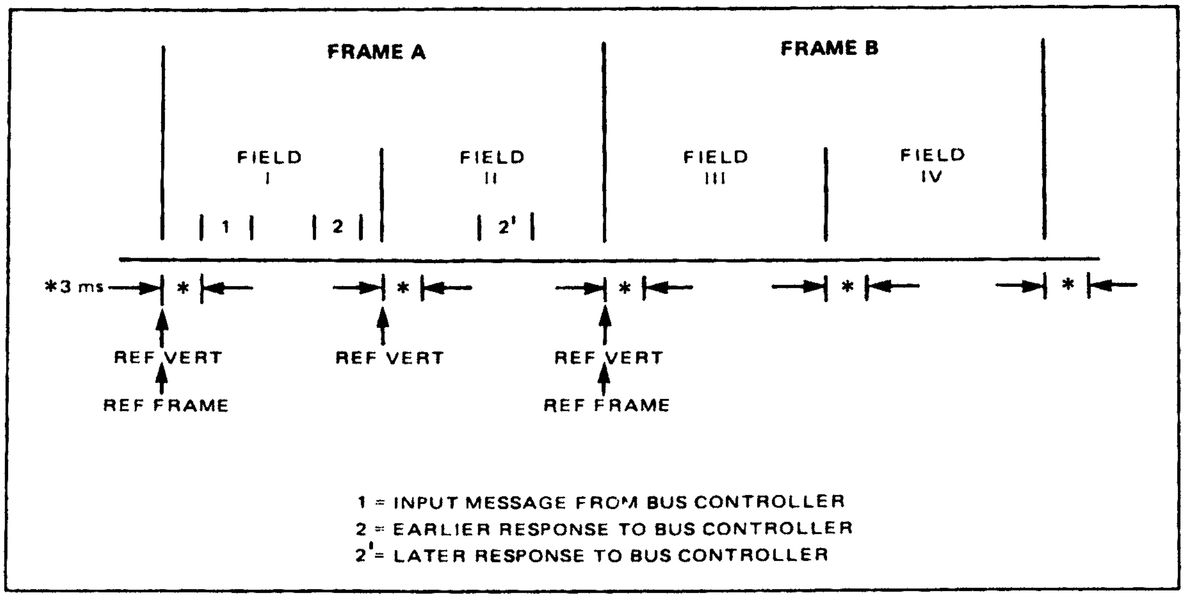

FRAME A
FRAME B
FIELD I
FIELD II
FIELD III
FIELD IV
1
2
2'
*3 ms
*
REF VERT
REF FRAME
1 = INPUT MESSAGE FROM BUS CONTROLLER
2 = EARLIER RESPONSE TO BUS CONTROLLER
2' = LATER RESPONSE TO BUS CONTROLLER

Figure 8-10. Communication Timing

Communication from the control system CPU takes place when reference frame is not present with NMI. Actual time required for communication is about 64 μs during the 3-ms period. This is the time it takes to read from (or write into) the 32-byte FIFOs.

Input from the Bus Controller can occur at any time during the odd-numbered field. If it is received during the first 3 ms of a frame, CPU U23 will not recognize INT from DART U24 and will not look at the input message until expiration of the 3-ms period, which is dedicated to internal housekeeping. If received within the 3-ms period, two bytes from the Bus Controller can be held in buffer registers within DART U24 until CPU U23 begins service of the interrupt.

The earliest start of serial communications begins with the leading edge of interval 1 (Figure 8-10). Interval 1 is the period in which the message from the bus controller is received by DART U24. The length of interval 1 depends on the length of the input message from the Bus Controller. CPU U23 computes requested information in the period between intervals 1 and 2. Duration of this period is also flexible, depending upon bulk and complexity of the requested information. If the input message from the Bus Controller is short and the requested information is brief, response to the Bus Controller is transmitted within the same odd-numbered field period. This is shown in Figure 8-10 as interval 2.

If, however, the input message and/or the requested information is lengthy, response to the Bus Controller may not take place until some time in the even-numbered field period. This is represented in Figure 8-10 as interval 2'.

Duration of intervals 1,2, and 2' is flexible, and the delay from the trailing edge of interval 1 until interval 2 (or 2') varies depending on length and content of the input message. In all cases, the Serial Remote PWA replies to the Bus Controller as quickly as possible. The Serial Remote PWA will normally always complete the reply to the Bus Controller before the next frame period. Thus, communication with the Bus Controller is not truly asynchronous. Each message must have frame reference, which is essential to making frame-accurate edits.

8-33 Jumpers

The Serial Remote PWA is equipped with jumpers as aids to testing and troubleshooting. Functions of J1 through J11 are listed in Table 8-6. Jumper locations are shown in Figure 8-24.

Table 8-6. Serial Remote PWA Jumpers

Jumper	Position	Function
J1	A-B	Normal.
	B-C	Places a bias on channel A serial data input (RxDA). (This jumper is for manufacturing test only.)
J2	A-B	Normal.
	A-C	Routes TB line of channel A serial data output at line driver U1-15 back into the DART at line receiver U3-6 (RB line). Jumper J3 must also be moved to A-C position.
J3	A-B	Normal.
	A-C	Routes TA line of channel A serial data output at line driver U1-14 back into the DART at line receiver U3-5 (RA line). Jumper J2 must also be moved to A-C position.
J4	A-B	Normal.
	Removed	Disconnects shift out clock to read FIFO U4–U7.
J5	A-B	Normal.
	Removed	Disconnects shift out clock to write FIFO U11–U14.
J6	A-B	Normal.
	Removed	Disconnects output enable to PROM U20.
J7	A-B NORM	Normal.
	A-C TEST	Forces continual NO-OP instruction for test of Z80 address bus.

(Continued next page)

Table 8-6. Serial Remote PWA Jumpers (Continued)

Jumper	Position	Function
J8	A-B	Normal.
	Removed	Disconnects CPU interrupt (INT) input from DART: INT input forced high.
J9	A-B	Normal.
	Removed	Disconnects clock (CLK) input from CPU.
J10	A-B	Normal.
	Removed	Disconnects clock (CLK) input from CPU and DART.
J11	A-B	Normal
	B-C	Disconnects channel A serial data output (TxDA) and connects channel B serial data output (TxDB) to line driver U1-14/-15.

8-34 Definition of Terms

Note

No attempt is made here to include all, or even most of the details contained in proposed SMPTE Recommended Practice RP 113. The following information, which is paraphrased from RP 113, is included in this manual only to clarify the balance of the theory of operation information.

Bus Controller:	Each serial data communications system contains one bus controller which supervises all tributaries in the system. Supervision is exercised through supervisory protocol defined in RP 113.
Byte:	Consists of 8 bits of information. Bits used to effect transmission such as byte START, PARITY, or END are not part of the byte.
Tributary:	Transfers messages to and from controlled equipment via the interface system. (In this manual, the Serial Remote PWA is considered to meet this definition.)
Word:	Consists of a byte and associated bits used to effect transmission such as START, PARITY, or END.

8-35 **Operational States.** The Serial Remote PWA operates in one of five major operational states: idle, active, poll, select, or group select.

IDLE:	The Serial Remote PWA does not communicate in any form. This state is exited only in response to BREAK from the Bus Controller. (See paragraph 8-36.)
ACTIVE:	The prerequisite state for transition to other operational states. The Serial Remote PWA enters this state whenever BREAK is received.
POLL:	The Serial Remote PWA will transmit a single status byte to the Bus Controller.
SELECT:	A single tributary (device in the serial data communications network) enters a communications mode with the Bus Controller.
GROUP SELECT:	All tributaries (devices) or a selected group of tributaries (devices) enter a communications mode with the Bus Controller.

8-36 **Supervisory Messages.** These messages supervise the channel and direct the flow of device messages. There are four supervisory messages: break, poll address, select address, and group select address.

BREAK:	BREAK drives all tributaries (devices) to the active state. The BREAK message is composed of spacing for 17 to 20 bit periods, followed by a minimum of 2 bit periods of marking.
ADDR-POLL:	Poll address message drives addressed device to the poll state.
ADDR-SELECT:	Select address message drives addressed device to the select state.
GROUP ADDR-SEL:	Group select address message drives a group of devices to the group select state.

8-37 **Supervisory Characters.** Supervisory characters identify communications sequences and provide status information. Supervisory characters are single bytes within the range of 00—7H (hex) as shown in Table 8-7.

8-38 Initialization Routine

System reset is asserted by the control system CPU while it is performing its own initialization routine. When control system initialization has been successfully completed, system reset is removed. The Serial Remote PWA CPU is then allowed to wake up and begin its own initialization. The initialization program includes resetting RAM U22, setting up DART U24, and establishing initial values.

Table 8-7. Supervisory Characters

Supervisory Character	Mnemonic	Name
01	GRP	Group assign
02	STX	Start of message
03	ESC	Escape
04	ACK	Acknowledge
05	NAK	Not acknowledge
06	BSY	Busy
07	RST	Reset
08	SVC	Service request from controlled equipment

CPU U23 uses a high-level program language which assumes that ZEROs are written in all addresses in RAM U22 at the outset of operation. Therefore, the initialization program first clears contents of all RAM addresses to zero.

DART U24, as a programmable device, must know what type of messages it will be receiving. Therefore, there are several control words which must be sent by CPU U23 to the DART before it will function as required in the Serial Remote PWA.

The CPU then sets one-time initial values in DART U24 and RAM U22.

8-39 Background Routine

When the VPR-80 is in cue mode at the direction of CPU U23, the cue point is stored in RAM U22. This is the only background activity other than housekeeping in the CPU. Everything else is part of foreground activity.

8-40 Foreground Routines

The control system CPU checks communications with the Serial Remote PWA on every vertical interval. This periodic check of communication is a foreground routine.

Inasmuch as all communication activity is synchronized to interrupts (NMI generated by reference vertical and INT generated by DART U24), exchanges with the VPR-80 control system and with the Bus Controller are considered as foreground routines.

8-41 **Exchanges with Control System.** The communication check with the Control PWA is initiated by the control system CPU.

The control system sends a discrete checksum data word to the Serial Remote PWA via the system data bus and a series of WRITE commands on the system address/control bus. The checksum data word is shifted through write FIFO U11—U14 and presented to CPU U23 for recognition. Assuming that U23 recognizes the word, it then writes the same checksum word at the input of read FIFO U4—U7. The word is then shifted out on a series of read commands from the control system and presented to the control system CPU for comparison with the checksum word sent on the previous write cycle. If the same checksum word is not recognized by the control system CPU, fault indication **106-08** is brought up for display. This communication check is repeated on every vertical interval. Refer to paragraph 6-36.

The three commands from the VPR-80 control system are read, reset, and write. Decoding of these commands is explained in paragraph 8-31.

When READ (4C00) is asserted, the decoder output at U16-12 triggers one-shot U10-12 and enables input data buffer U9. The one-shot output shifts contents of read FIFO U4—U7, and the byte at the exit stage of the FIFO is placed on the system data bus. READ command is sent 32 times within one field period. Thus, the entire contents of 32 x 8 read FIFO U4—U7 are shifted out to the system data bus. Reading the contents of FIFO U4—U7 is entirely under control of the control system CPU.

Before the control system can write new information in write FIFO U11—U14, the FIFO must be reset. When the control system asserts RESET (4C03), output of inverter U15-2 resets all stages of write FIFO U11—U14. The FIFO is then ready to receive data from the control system.

When WRITE (4C02) is asserted, decoder output at U16-10 shifts contents of write FIFO U11—U14. The WRITE command is also sent by the control system 32 times within alternate field periods. Thus, the control system fills all stages of the 32 x 8 write FIFO with new bytes of information from the VPR-80. At this point in the write operation, CPU U23 takes over.

The output of address XX1X at U21-11 enables decoder U16. The output of address XX10 at U16-4 triggers one-shot U10-4 and enables output data buffer U8. The one-shot output shifts the contents of write FIFO U11—U14, and the byte at the exit stage of the FIFO is placed on the Z80 data bus. Address XX10 is asserted 32 times, thus presenting the entire contents of the write FIFO to CPU U23.

8-42 **Exchanges with Bus Controller.** At the outset of operation, serial communication between the Serial Remote PWA and the Bus Controller is verified.

The Serial Remote PWA wakes up in the idle state. In this state no serial communication is possible, but the Serial Remote PWA will respond to a two-byte address (VTR identification word) from the Bus Controller. The address, established by the operator (see paragraph 8-16), identifies the VPR-80 on the serial communication bus. The decimal number entered by the operator is converted to a two-byte address. The Bus Controller transmits the most significant byte first.

When the Serial Remote PWA receives the first byte of the address, it takes one step away from idle state and waits for the second byte. If the second byte does not complete the preset identification word, or does not arrive within three frame periods, the Serial Remote PWA reverts to the idle state. If the second byte does complete the preset identification word, the Serial Remote PWA transits to the select state. It will stay in select state, and the serial address verification need not be repeated as long as power is on, unless there is a data communication error. If there is an error, the Serial Remote PWA reverts to the idle state, and the serial communication identification word must be reverified.

The next supervisory character sent by the Bus Controller will be ESC, and the Serial Remote PWA will respond with ACK. At this point serial communication has been established.

Supervisory messages to the Serial Remote PWA are of two types: those which direct the VPR-80 to do something (commands), and those which request the VPR-80 to reply with some specific information (status requests).

The VPR-80 responds to a command with ACK if the command is received properly, and then proceeds to execute the command. If the command is not received properly, the VPR-80 responds with NAK and transits to the idle state.

If there is a communication error in a status request, the VPR-80 responds with NAK and transits to the idle state. The VPR-80 responds to a properly received status request with STX, followed by a byte count of the requested message(s) (not counting STX or the byte count of the checksum at the end), followed by an echo of the status request, followed by the requested data, and terminated with the checksum byte. The byte count includes the echo.

The checksum is the TWOs complement of the sum (without carry) of the data, including byte count and echo bytes. Each response is prefaced with the command echo.

Once serial communications have been established, commands from the Bus Controller to the VPR-80 are in the following form:

STX
Byte count of the message
Message (variable length)
Checksum

Multiple commands or subcommands can be sent in one message as follows:

STX
Byte count of the entire message
Command 1
Command 2
Command N
Checksum

Green LED indicators DS2 and DS3 (see Figure 8-24) blink to indicate activity on the TxDA and RxDA lines, respectively. These indicators are not placarded and are not intended to convey any other specific information.

8-43 PWA Configurations

If the VPR-80 has not been previously equipped with an accessory Time-Code System (TCS) PWA in PWA slot 3, the Serial Remote PWA (mounted on a metal shield plate) is connector-mounted directly in the slot 3 motherboard connector. If the VPR-80 is equipped with a TCS PWA in slot 3, the Serial Remote PWA (without shield plate) is connector-mounted on top of the TCS PWA.

When the Serial Remote PWA is to be mounted directly in the slot 3 motherboard connector, the Serial Remote PWA is attached to a metal shield (Ampex Part No. 1450909) as shown in Figure 8-11. Side edges of the Serial Remote PWA and guide plates on the shield slip into slot 3 guides. Extraction handles on upper corners of the shield allow the Serial Remote PWA to be removed in the same manner as the other PWAs.

The TCS PWA is also mounted (with a shield) in slot 3. When the Serial Remote PWA is to be added to a VPR-80 with TCS PWA previously installed, the Serial Remote PWA (without shield) is connector-mounted on top of the TCS PWA as shown in Figure 8-12. The Serial Remote PWA interfaces directly with the Control PWA via printed wiring on the TCS PWA. Extraction handles on the shield allow the Serial Remote and TCS PWAs to be removed as one.

8-44 TIME-CODE SYSTEM PWA

The Time-Code System (TCS) PWA generates longitudinal time code in accordance with either of the following television industry standards.

- SMPTE Proposed Recommended Practice RP 93-1980, "Requirements for Recording American National Standard Time and Control Code on 1-in. Types B and C Helical Scan Video Tape Recorders"
- EBU Technical Bulletin 3097-E, "EBU time-and-control codes for television tape recordings (625-line television systems)"

The following discussions assume the reader's familiarity with the applicable standard which governs TC format and operational practices.

The VPR-80 does not have the capability of generating or reading vertical interval time code. Therefore, the term "time code" in this manual should be taken to mean longitudinal time code.

Time code (TC) is a digital signal containing 80 bits per television frame, and is recorded in bi-phase mark (Manchester I) code format on the audio channel 3 longitudinal track. The code uniquely defines, or addresses, every frame on the tape in hours, minutes, seconds, and frames. The signal originates from a time-code generator (TCG) and can be distributed to other VTRs and editing devices.

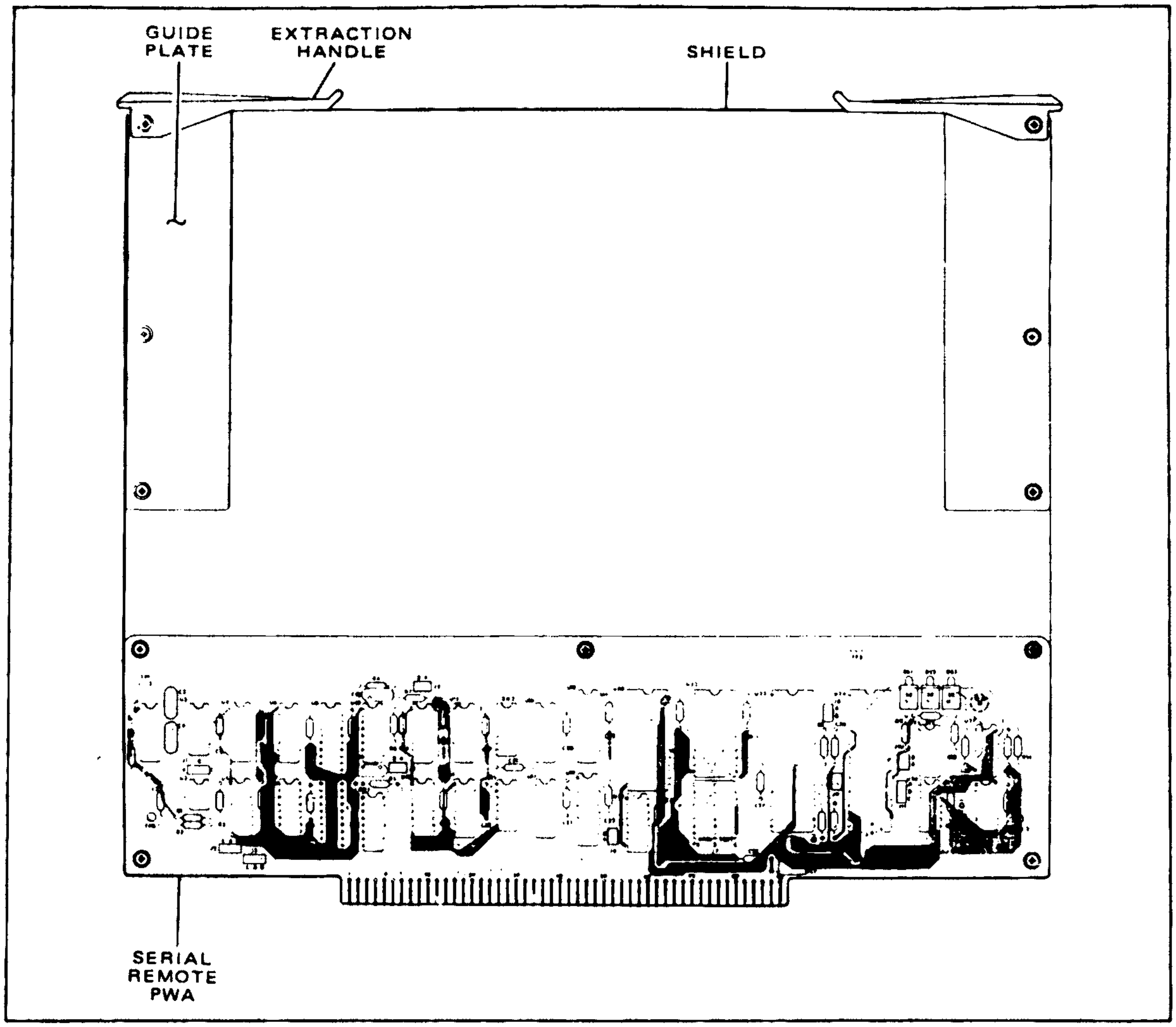


Figure 8-11. Serial Remote PWA with Shield

The serial TC output of the TCG is routed to the Audio PWA for recording in the audio channel 3 track. In play modes, the demodulated TC signal is routed from the Audio PWA to the TCS PWA where the time-code reader (TCR) assembles the time-code words and accesses corresponding blocks of alphanumeric characters held in character generator PROM storage. The TCS CPU inserts the character generator (CG) video in the monitor video signal output which is routed through the Reference PWA to the picture monitor.

The TCS PWA can also accept serial TC from an external TCG via the Audio PWA. The internal TCG can then be slaved to external TC information.

8-45 Installation

If the VPR-80 has not been previously equipped with an accessory Serial Remote PWA, the Time-Code System (TCS) PWA is simply connector-mounted in the slot 3

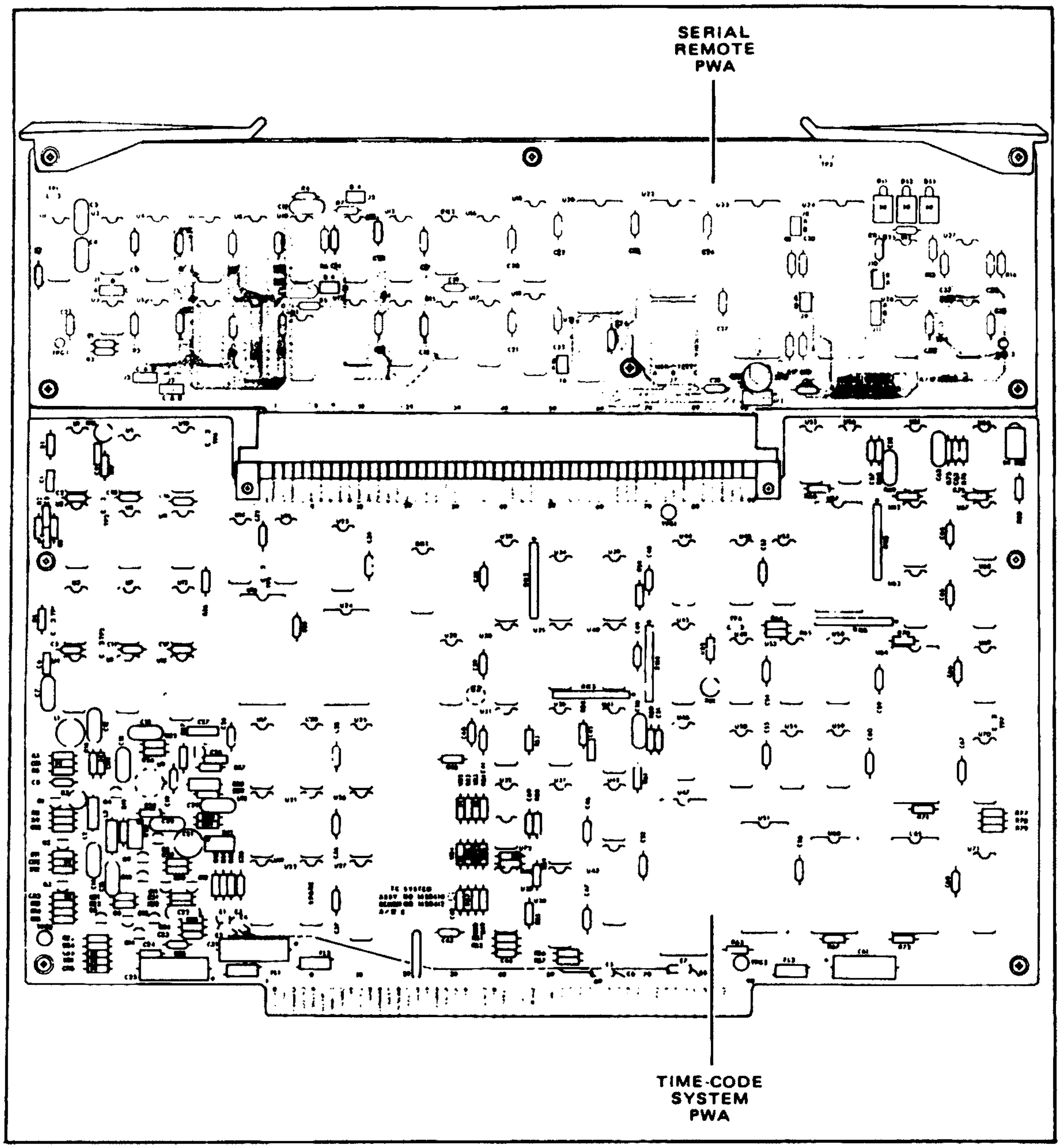


Figure 8-12. Serial Remote PWA Mounted on Time-Code System PWA

motherboard connector. When the TCS PWA is to be installed in a VPR-80 equipped with a Serial Remote PWA, the Serial Remote PWA must first be removed from the VPR-80 and then removed from its shield plate. The TCS and Serial Remote PWAs are then attached to the plate and mounted in the slot 3 motherboard connector as one assembly.

When the TCS PWA is added to a VPR-80 which is not mounted in a monitor console, the following connections must be added:

- MONITOR VIDEO OUT of TBC to AUX (J8) of VPR-80.
- MONITOR VIDEO OUT of VPR-80 to VIDEO IN of picture monitor.

When the TCS PWA is added to a VPR-80 which is mounted in a monitor console, the following connection changes must be made:

- Connect MONITOR VIDEO OUT of TBC to AUX (J8) of VPR-80.
- Remove connection between TBC VIDEO OUTPUT and VTR OUTPUT (P8) on the monitor switcher I/O connector panel.
- Connect MONITOR VIDEO OUT (J13) of VPR-80 to DEMOD VID (P7) of monitor switcher I/O connector panel.

The source of external TC and user information (when used) is connected at the AUDIO 3 IN connector (J3) on the VPR-80 I/O connector panel.

8-46 Installation without Serial Remote PWA

When the TCS PWA is to be mounted in the slot 3 motherboard connector, it is attached to a metal shield (Ampex Part No. 1450909) as shown in Figure 8-13. Side edges of the TCS PWA slip into slot 3 guides. Extraction handles on upper corners of the shield allow the TCS PWA to be removed in the same manner as other PWAs.

8-47 Installation with Serial Remote PWA

The Serial Remote PWA is also mounted (with a shield) in slot 3 as shown in Figure 8-11. When the TCS PWA is to be added to a VPR-80 with a Serial Remote PWA previously installed, the Serial Remote PWA must first be removed from the VPR-80. The TCS PWA is installed, and the Serial Remote PWA is reinstalled, in the VPR-80 as follows:

STEP 1 Remove five screws and washers which secure the Serial Remote PWA to the shield and detach the Serial Remote PWA. Refer to Figure 8-11.

STEP 2 Remove six screws and washers securing the two guide plates and extraction handles to the shield. Guide plates can be discarded.

STEP 3 Using the same hardware, attach the TCS PWA to the shield with four screws and four washers as shown in Figure 8-13.

STEP 4 Insert PWA-edge connector of the Serial Remote PWA into the female connector on the top edge of the TCS PWA.

STEP 5 Attach Serial Remote PWA and the two extraction handles to the plate with four screws and four washers as shown in Figure 8-12.

When the TCS PWA, Serial Remote PWA, and shield plate have been assembled as outlined above, assembly is connector-mounted in the motherboard slot 3 connector. Edges of the TCS and Serial Remote PWAs slip into slot 3 guides. The Serial Remote PWA interfaces directly with the Control PWA via printed wiring on

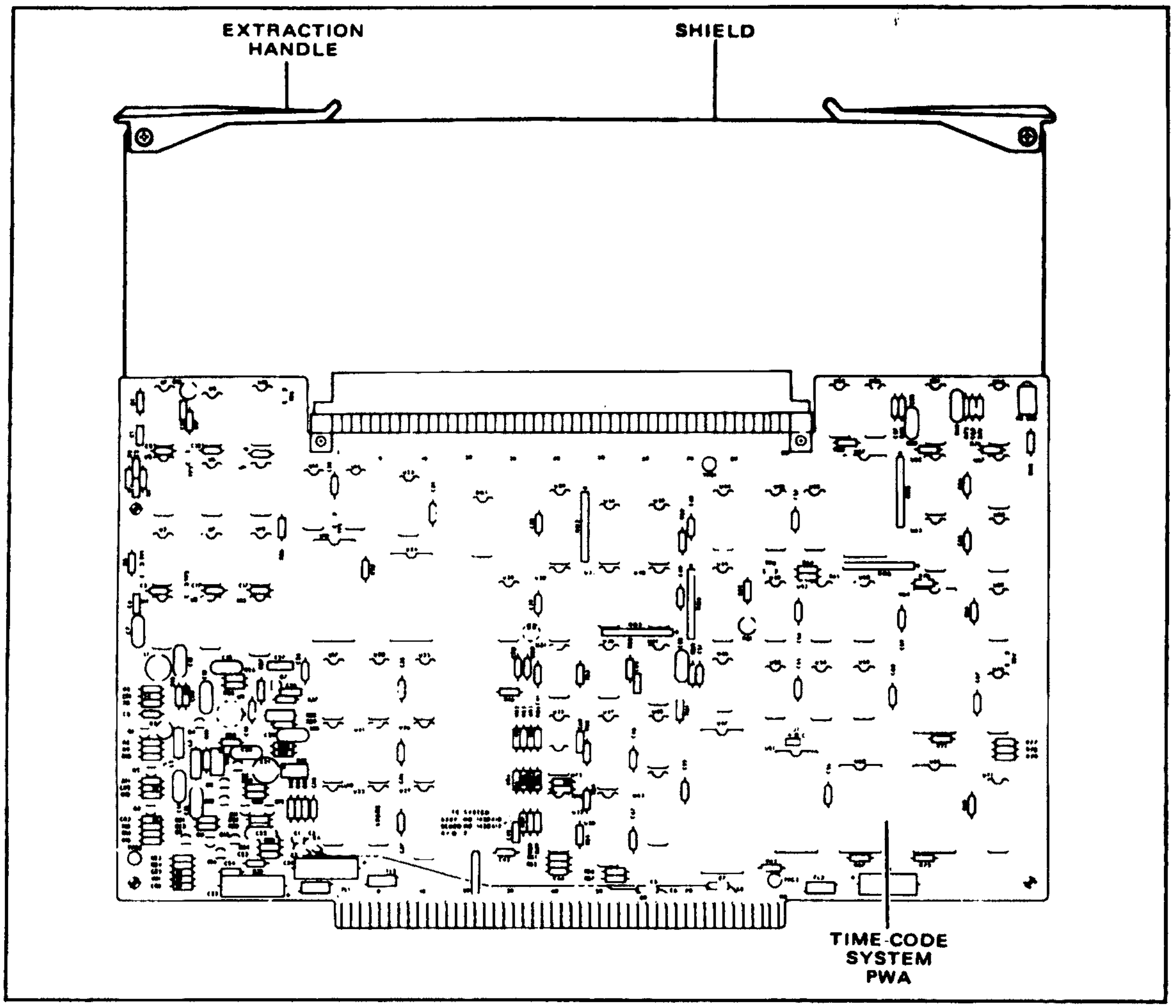


Figure 8-13. Time-Code System PWA with Shield

the TCS PWA. Extraction handles on the shield allow Serial Remote and TCS PWAs to be removed as one assembly.

8-48 Setup Modes

Several VPR-80 setup modes are at the user's disposal, whereby operation of the TCS PWA can be altered to suit individual requirements and editing situations. Setup instructions are given in the following paragraphs. Setup modes for the TCS PWA are listed below.

• Setup 20	Preset TC Information
• Setup 21	Preset User Information
• Setup 22	Select Source of TC Information
• Setup 23	Select TCG Mode of Operation
• Setup 24	Select Full Frame or Drop Frame Operation

• Setup 25	Select Binary or ASCII User Bits
• Setup 30	Select CG Information Display
• Setup 31	Select Character Size
• Setup 32	Select Black or White Background
• Setup 33	Adjust Character Display Position

In addition, system setup mode 4 allows selection of either tape-time or time-code display on the VPR-80 primary control panel.

Select time code for display on the control panel as follows:

STEP 1 Press SET UP.

STEP 2 Enter 4 on the keypad, and press ENTER. Control panel display will show **4-1** if tape time has been previously selected, or it will show **4-2** if time code has been previously selected.

STEP 3 If the display shows **4-1**, enter 2 on the keypad and press ENTER. Display will show **2**.

STEP 4 Press ENTER. Control panel display will change to **4-2**.

STEP 5 If other setup procedures are to be done, press STOP to terminate display selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-49 Preset Time-Code Information

Preset new time-code information in the TCG as follows:

STEP 1 Press SET UP.

STEP 2 Enter 20 on the keypad. Control panel display shows **20**.

STEP 3 Press ENTER. Control panel display changes to **00:00:00:00**.

STEP 4 Using the keypad, enter time information in the following sequence:

TENS OF HOURS
UNITS OF HOURS
TENS OF MINUTES
UNITS OF MINUTES
TENS OF SECONDS
UNITS OF SECONDS
TENS OF FRAMES
UNITS OF FRAMES

The control panel display follows keypad input from right to left. Use arrow (backspace) key to correct errors in manual entry.

STEP 5 Press keypad ENTER switch. If TCG is selected for display (see paragraph 8-63—setup mode 30), the CG display on the picture monitor will show selected preset time.

STEP 6 If other setup procedures are to be done, press STOP to terminate TC information preset procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-50 Preset User Information

There are eight 4-bit binary groups in the 80-bit TC word which are dedicated to user information. As shown in Figure 8-14, binary groups (BG) are paired, and each of the four pairs can be used for an ASCII* character of user information. Selection of ASCII characters which can be preset in the TCG is limited to those shown in boldface type in Table 8-8.

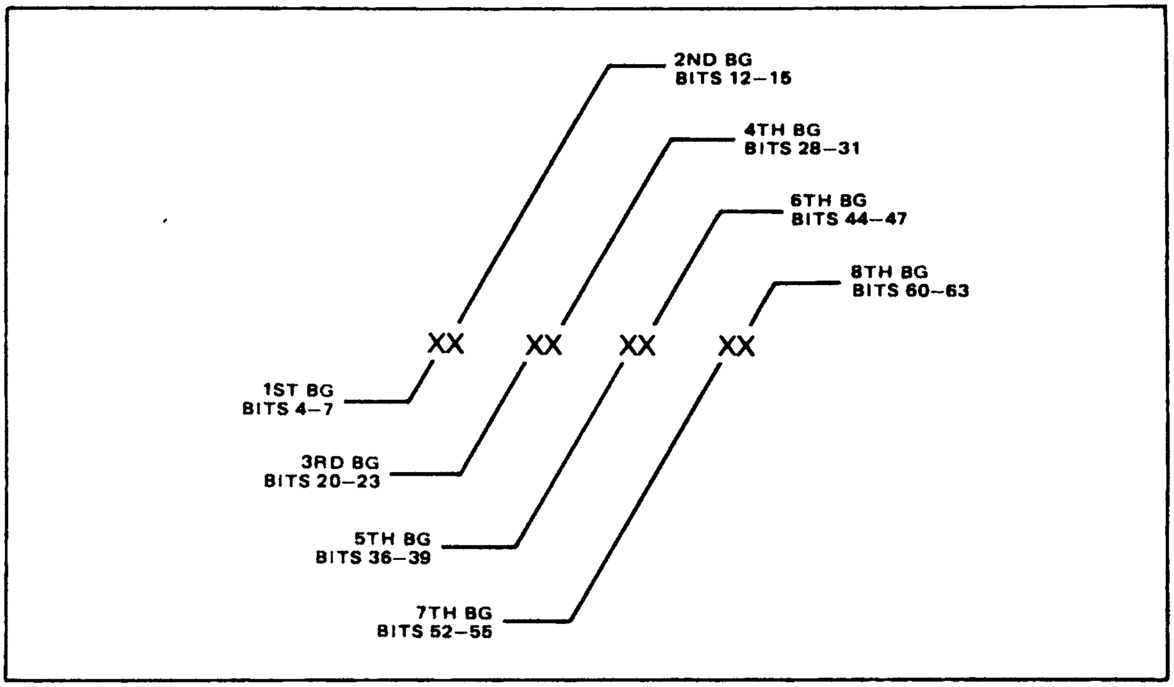


Figure 8-14. User Information—Binary Groups

Keypad entries must be made and entered in control system logic within 5 seconds. (Control system logic erases keypad entries if ENTER switch is not pressed within 5 seconds.) Therefore, before step 5 of the following procedure is attempted it is suggested that a list be made of keypad entries required to access selected ASCII characters of user information.

Preset user information in the TC word as follows:

---

* American Standard Code for Information Interchange

Table 8-8. ASCII Characters—Manual Entry

LSD \ MSD	3	4	5
0	0		P
1	1	A	Q
2	2	B	R
3	3	C	S
4	4	D	T
5	5	E	U
6	6	F	V
7	7	G	W
8	8	H	X
9	9	I	Y

BLANK

EXAMPLE:

KEYPAD ENTRIES SHOWN ON CONTROL PANEL DISPLAY ➧	5	6	5	0	5	2	3	8
CORRESPONDING CHARACTERS SHOWN ON PICTURE MONITOR ➧	V		P		R		8	

Two keypad entries are required for each ASCII character. See Table 8-8. On the keypad, enter the more significant digit (MSD) first, and then the less significant digit (LSD). For example:

To enter ASCII character "V", enter 5 and then 6.
To enter ASCII character "P", enter 5 and then 0.
To enter ASCII character "R", enter 5 and then 2.
To enter ASCII character "8", enter 3 and then 8.

Make a list of keypad entries required to preset your user information beforehand. This will avoid the frustration of having the control panel display self-erase while you are choosing required keypad entries from Table 8-8.

STEP 1 Ascertain that user information code selection setup is set for ASCII code. See paragraph 8-61.

STEP 2 Press SET UP.

STEP 3 Enter 21 on the keypad. Control panel display shows **21.**

STEP 4 Press ENTER. Control panel display changes to all zeros without colons (**00000000**).

STEP 5 Enter 2-digit desigation for each of the ASCII characters chosen from Table 8-8. Control panel display follows keypad input from right to left. Use arrow (backspace) key to correct errors in manual entry.

STEP 6 Press ENTER. If USG is selected for display (see paragraph 8-63—setup mode 30), CG display on the picture monitor will show preset user information.

Notes

If MSD entries other than 3, 4, or 5 are made, the corresponding CG display on the picture monitor will be extraneous (and meaningless) fragments of characters.

User information characters entered in steps 5 and 6 are shown on the left-hand side of the CG display on the picture monitor. User information which is thus replaced is shown on the right-hand side.

STEP 7 If other setup procedures are to be done, press STOP to terminate user information preset procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-51 Time-Code Source Selection

Setup mode 22 allows selection of either internal or external TC and user information to be recorded.

8-52 Internal Time-Code. Setup mode 22-1 selects internal TCG as the source of TC information and local user information (as selected in paragraph 8-50) to be recorded.

Select internal TC and internal user information as follows:

STEP 1 Press SET UP.

STEP 2 Enter 22 on the keypad. Control panel display will show **22-X.**

STEP 3 If control panel display does not show **22-1,** enter 1 on the keypad.

STEP 4 Press ENTER. Display will change to **22-1.**

STEP 5 If other setup procedures are to be done, press STOP to terminate internal TC selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-53 **External Time-Code.** Setup mode 22-2 selects an external TCR as source of TC information and external user information to be recorded.

Select external TC and external user information as follows:

STEP 1 Press SET UP.

STEP 2 Enter 22 on the keypad. Control panel display will show **22-X.**

STEP 3 If control panel display does not show **22-2,** enter 2 on the keypad.

STEP 4 Press ENTER. Display will change to **22-2.**

STEP 5 If other setup procedures are to be done, press STOP to terminate external TC and user information selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-54 **Jam Mode.** Setup mode 22-3 is used to select jam mode. Jam mode provides a contiguous TC recording when making edits. In jam mode the TCR reads off-tape TC in audio track 3 up to the edit entrance point. At the entrance point, the last off-tape TC word is automatically preset in the TCG. The TCG then generates TC through the edit interval which is contiguous (sequential) with the recorded TC preceding the edit. In jam mode, user information from the internal TCG is recorded throughout.

Select jam mode as follows:

STEP 1 Press SET UP.

STEP 2 Enter 22 on the keypad. Control panel display will show **22-X.**

STEP 3 If control panel display does not show **22-3,** enter 3 on the keypad.

STEP 4 Press ENTER. Display will change to **22-3.**

STEP 5 If other setup procedures are to be done, press STOP switch to terminate jam mode selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-55 **Slave Mode.** Setup mode 22-4 is used to select slave mode. When in slave mode, the internal TCG is slaved to the source of external TC. User information in the recorded TC word, however, is preset internal user information. Refer to paragraph 8-50.

Select slave mode as follows:

STEP 1 Press SET UP.

STEP 2 Enter 22 on the keypad. Control panel display will show **22-X.**

STEP 3 If control panel display does not show **22-4,** enter 4 on the keypad.

STEP 4 Press ENTER. Display will change to **22-4.**

STEP 5 If other setup procedures are to be done, press STOP to terminate slave mode selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-56 Time-Code Generator Mode

Setup mode 23 allows selection of TCG mode: run, hold, or sequence mode.

8-57 Run Mode. Setup mode 23-1 is used to select run mode. In run mode, internal TCG continuously generates sequential TC words. Therefore, recorded TC will be discontinuous between times that audio channel 3 exits and reenters record mode. Run mode is effective only if internal TC generation is selected. Refer to paragraph 8-52.

Select run mode as follows:

STEP 1 Press SET UP.

STEP 2 Enter 23 on the keypad. Control panel display will show **23-X.**

STEP 3 If control panel display does not show **23-1,** enter 1 on the keypad.

STEP 4 Press ENTER. Display will change to **23-1.**

STEP 5 If other setup procedures are to be done, press STOP to terminate run mode selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-58 Hold Mode. Setup mode 23-2 is used to select hold mode. In hold mode, preset TC in the internal TCG is held (frozen) until audio channel 3 enters record mode. When audio 3 recording begins, the TCG runs continuously (reverts to run mode—refer to paragraph 8-57).

Select hold mode as follows:

STEP 1 Press SET UP.

STEP 2 Enter 23 on the keypad. Control panel display will show **23-X.**

STEP 3 If control panel display does not show **23-2,** enter 2 on the keypad.

STEP 4 Press ENTER. Display will change to **23-2.**

STEP 5 If other setup procedures are to be done, press STOP to terminate hold mode selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-59 Sequence Mode. Setup mode 23-3 is used to select sequence mode. In sequence mode, the TCG is halted until audio channel 3 enters record mode. At that time the TCG starts to generate sequential TC. When record mode is exited, the TCG is halted. When recording of audio channel 3 is resumed there will be a slight discontinuity in the TC (unlike jam mode—paragraph 8-54), but TC recording will be essentially sequential.

Select sequence mode as follows:

STEP 1 Press SET UP.

STEP 2 Enter 23 on the keypad. Control panel display will show **23-X**.

STEP 3 If control panel display does not show **22-3**, enter 3 on the keypad.

STEP 4 Press ENTER. Display will change to **23-3**.

STEP 5 If other setup procedures are to be done, press STOP to terminate sequence mode selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-60 Frame Count Selection

Setup mode 24 is provided for 525-line/60-Hz video systems. This setup mode allows selection of either full-frame or drop-frame operation of the TCG.

Note

Keep in mind that this setup mode modifies operation of the TCG only. Operation of the TCR is unaffected. The TCR will read whatever is recorded on tape, full-frame or drop-frame TC.

Select TCG full-frame or drop-frame operation as follows:

STEP 1 Press SET UP.

STEP 2 Enter 24 on the keypad and press ENTER. Control panel display will show **24-1** if full-frame operation has been previously selected, or it will show **24-2** if drop-frame operation has been previously selected.

STEP 3 Enter 1 on the keypad to select full-frame operation, or enter 2 to select drop-frame operation.

STEP 4 Press ENTER. Display will change accordingly.

Note

When drop-frame operation of the TCG is selected, colons which separate the hour, minute, second, and frame values on the picture monitor are changed to semicolons.

STEP 5 If other setup procedures are to be done, press STOP to terminate frame count selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-61 User Information Code Selection

User information in the TC word can be generated in a limited number of ASCII* characters. Setup mode 25 is used for selection of either binary or ASCII code; however, to date, generation of user information in binary code has not been implemented.

Make sure that setup mode 25 is set for ASCII code as follows:

STEP 1 Press SET UP.

STEP 2 Enter 25 on the keypad and press ENTER. Control panel display will show **25-1** if binary code has been previously selected, or it will show **25-2** if ASCII code has been previously selected.

STEP 3 If display shows **25-1**, enter 2 to select ASCII code.

STEP 4 Press ENTER. Display will change to **25-2**.

STEP 5 If other setup procedures are to be done, press STOP to terminate user information code selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-62 Character Generator Display Selection

The character generator (CG) video output is routed to the Reference PWA where it is inserted in the video output to the picture monitor. The picture monitor can be commanded to display tape timer time, TC from either the TCG or TCR, or user information from either TCG or TCR. The picture monitor can also be commanded to display combinations of the above types of information, including time display with edit entrance and exit points. The display of CG output can also be simply turned off.

8-63 **Information to be Displayed.** Setup mode 30 is used to select information to be displayed. The following mnemonics are used in the picture monitor display to identify information.

TTM Tape time (from the tape timer on the Control PWA)

---

* American Standard Code for Information Interchange. Refer to paragraph 8-50.

TCR	TC from the TCR
USR	User information from the TCR
TCG	TC from the TCG (including external TCG when in slave mode)
USG	User information from the TCG
ENT	Edit entrance point
EXT	Edit exit point

Colons that punctuate the TTM, TCR, TCG, ENT, and EXT values are replaced by semicolons when drop-frame count is used. Refer to paragraph 8-60.

Select information to be displayed on the picture monitor as follows:

STEP 1 Press SET UP.

STEP 2 Enter 30 on the keypad and press ENTER. Display on the control panel will show **30-X**. The dash number indicates type of information to be displayed.

STEP 3 Select information display as follows:

- To turn off the CG display on the picture monitor, enter 0 on the keypad and press ENTER. Display on the control panel will show **30-0**, and the CG display on the picture monitor, if any, will cease when ENTER is pressed.
- To display time from tape timer, enter 1 on the keypad and press ENTER. Display on the control panel will show **30-1**, and the CG display on the picture monitor will appear as follows:

  TTMXX:XX:XX:XX

- To display TC from the TCR, enter 2 on the keypad and press ENTER. Display on the control panel will show **30-2**, and the CG display on the picture monitor will appear as follows:

  TCRXX:XX:XX:XX

- To display user information from the TCR, enter 3 on the keypad and press ENTER. Display on the control panel will show **30-3**, and the CG display on the picture monitor will appear as follows:

  USRXXXX XXXX*

- To display TC from the TCG, enter 4 on the keypad and press ENTER. Display on the control panel will show **30-4**, and the CG display on the picture monitor will appear as follows:

  TCGXX:XX:XX:XX

---

*Current user information on the left, followed by a blank space, and then most recently replaced user information on the right.

- To display user information from the TCG, enter 5 on the keypad and press ENTER. Display on the control panel will show **30-5**, and the CG display on the picture monitor will appear as follows:

  USGXXXX XXXX*

- To display a combination of time and edit entrance and exit points, enter 6 on the keypad and press ENTER. Display on the control panel will show **30-6**.

  If tape time has been previously selected for display (system setup mode 4—paragraph 8-48), the CG display on the picture monitor will appear as follows:

  either** **TTMXX:XX:XX:XX**
  ENTXX:XX:XX:XX

  or*** **TTMXX:XX:XX:XX**
  EXTXX:XX:XX:XX

  If TC has been previously selected for display (system setup mode 4—paragraph 8-48), the CG display on the picture monitor will appear as follows:

  either** **TCRXX:XX:XX:XX**
  ENTXX:XX:XX:XX

  or*** **TCRXX:XX:XX:XX**
  EXTXX:XX:XX:XX

- To display TC and user information from the TCR, enter 7 on the keypad and press ENTER. Display on the control panel will show **30-7**, and the CG display on the picture monitor will appear as follows:

  TCRXX:XX:XX:XX
  USRXX:XX:XX:XX

- To display TC and user information from the TCG, enter 8 on the keypad and press ENTER. Display on the control panel will show **30-8**, and the CG display on the picture monitor will appear as follows:

  TCGXX:XX:XX:XX
  USGXX:XX:XX:XX

- To display TC from the TCR and time from the tape timer, enter 9 on the keypad and press ENTER. Display on the control panel will show **30-9**, and the CG display on the picture monitor will appear as follows:

---

* Current user information on the left, followed by a blank space, and then most recently replaced user information on the right.

** Edit entrance point displayed if *not within* edit interval.

*** Edit exit point displayed if *within* edit interval.

TCRXX:XX:XX:XX
TTMXX:XX:XX:XX

STEP 4 If other setup procedures are to be done, press STOP to terminate information display selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-64 Character Size. The CG output can be displayed in either of two sizes on the picture monitor. Setup mode 31 is used to select larger or smaller size characters.

Make selection between larger and smaller size characters as follows:

STEP 1 Press SET UP.

STEP 2 Enter 31 on the keypad and press ENTER. Display will show **31-1** if large characters have been previously selected, or **31-2** if small characters have been previously selected.

STEP 3 Enter 1 on the keypad to select large characters, or enter 2 to select small characters.

STEP 4 Press ENTER. Display will change accordingly.

STEP 5 If other setup procedures are to be done, press STOP to terminate character size selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-65 Background. The CG output can be displayed on the picture monitor as either white characters on a black background or black characters on a white background. Setup mode 32 allows selection of black or white background.

Make selection between black and white background as follows:

STEP 1 Press SET UP.

STEP 2 Enter 32 on the keypad and press ENTER. Display will show **32-1** if black background has been previously selected, or it will show **32-2** if white background has been previously selected.

STEP 3 Enter 1 on the keypad to select black background or enter 2 to select white background.

STEP 4 Press ENTER. Display will change accordingly.

STEP 5 If other setup procedures are to be done, press STOP to terminate background selection procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-66 Character Position. Position of the CG display on the picture monitor screen can be adjusted vertically or horizontally. Setup mode 33 allows position adjustment of the CG output display.

Adjust position of the CG output display as follows.

STEP 1 Press SET UP.

STEP 2 Enter 33 on keypad, and press ENTER. Control panel display will show **33-0.**

Note

Position adjustment setup mode wakes up in standby (33-0), preventing the CG display from immediately moving to the position commanded by the tape speed control knob.

STEP 3 To adjust vertical position of the CG display on the picture monitor, enter 1 on the keypad. Display on the control panel changes to **1.**

STEP 4 Press ENTER. Control panel display changes to **33-1.**

STEP 5 Use tape speed control knob to adjust vertical position of CG display. Clockwise rotation of the knob moves CG display upward. Counterclockwise rotation of the knob moves CG display downward.

STEP 6 To adjust horizontal position of the CG display on the picture monitor, enter 2 on the keypad. Display on the control panel changes to **2.**

STEP 7 Press ENTER. Control panel display changes to **33-2.**

STEP 8 Use tape speed control knob to adjust horizontal position of CG display. Clockwise rotation of knob moves CG display to the right. Counterclockwise rotation of the knob moves CG display to the left.

STEP 9 If other setup procedures are to be done, press STOP to terminate character position adjustment procedure. Otherwise, press alternate-action SET UP switch to exit setup mode.

8-67 Theory of Operation

Time-Code System (TCS) PWA logic is composed of the CPU kernel, control system interface, time-code generator, time-code reader, and character generator. Regulated +5 Vdc and ±15 Vdc are supplied to components on the TCS PWA via motherboard power distribution (PWA connector contacts 97—100 and 1-6).

In the following discussions, reference designations of components on the Control PWA are prefixed with 6. Reference designations of components on the TCS PWA are not prefixed. It should also be noted that the terms "read," "write", "input," and "output" are used with respect to the control system CPU.

8-68 CPU Kernel

TCS PWA control logic consists of microprocessor (CPU) U47, crystal oscillator U42, time-code reader program PROM U51, program RAM U60, video RAM U65, and address decoders U62 and U66. The TCS CPU kernel is shown in Figure 8-15.

The TCS PWA microprocessor is a Zilog Z80 CPU. Internal architecture and instructions are more than adequately documented by the manufacturer, and consequently are not given in this manual. However, complete details of all Z80 I/O signal characteristics are given in Appendix A of the *VPR-80 Parts Lists and Schematics* manual. In this application, the CPU low-active bus request (BUSRQ) input is held high through R63. HALT, refresh (RFSH), and bus acknowledge (BUSAK) outputs are unused.

Green LED indicator DS1 (see Figure 8-25) blinks to indicate that the CPU program is running and that timing input supplied by reference frame is being received.

8-69 Clock, Reset, and Interrupt Inputs. Crystal oscillator U42 supplies two buffered clock outputs: 4 MHz and 8 MHz. The CPU clock is supplied by the 4-Mhz output of crystal oscillator U42. This is a single-phase clock which is also supplied to counter/timer and parallel I/O unit (CIO) U64 and to shift register U50.

When system reset is asserted by the control system CPU, the low output of inverter U31-8 resets CPU U47. It initializes the CPU and forces the CPU program counter to zero. During the time reset is asserted, data and address bus outputs go to a high-impedance state.

Interrupt (INT) input is low-active. It is asserted by CIO U64. When the CPU recognizes the interrupt at the end of the current instruction, it sends input/output request (IORQ) which enables address decoder U62. The decoder then asserts chip enable to the CIO.

Nonmaskable interrupt (NMI) input is negative edge-triggered. It is a higher priority interrupt than INT and it is always recognized at the end of the current instruction. When enabled, NMI is asserted by reference frame pulses from the AST Servo PWA.

8-70 **R/W, I/O and Memory Request, and M1 Outputs.** Read (RD) and write (WR) are tristate low-active outputs. RD is asserted when the CPU is ready to read information from RAM U60 or U65. RD enables RAM information output. RD also enables input data buffer U38.

WR is asserted when the CPU is ready to write information in RAM U60 or U65. WR enables information to be written into RAM storage. WR also enables character generator data transfer at gate U68-3 and clocks CPU commands to the output of output data latch U71.

Input/output request (IORQ) is a tristate low-active output. The CPU asserts IORQ in response to INT from CIO U64. IORQ enables address decoder U62 to apply commands to the time-code generator (TCG), time-code reader (TCR), and character generator. The I/O request enable output of gate U46-11 is delayed until expiration of M1 which is asserted with IORQ to acknowledge the interrupt.

Memory request (MREQ) is a tristate low-active output. When asserted, it indicates that the word on the Z80 address bus is valid for a memory read or write transfer. MREQ enables the output of EPROM U51 and section 1 of dual address decoder U66. Decoder output then enables information transfer from EPROM U51 to CPU U47.

The machine cycle one (M1) output is tristate and low-active. M1 indicates that the machine (CPU) is in the op code fetch cycle of an instruction execution. M1 is also asserted with IORQ to indicate an interrupt acknowledgment.

8-71 **Data Bus.** The CPU 8-bit, bidirectional data port (D0—D7) is tristate and high-active. Information is exchanged on the TCS data bus between the CPU and memory (RAM or PROM) and I/O devices (CIO, output data buffers, FIFOs, or input data latches).

8-72 **Address Bus.** The CPU 16-bit address port (A0—A15) is tristate and high-active. The word on the TCS address bus is validated by the CPU output of IORQ or MREQ to address decoders U62 or U66.

8-73 **Memory.** The TCS CPU kernel includes three memory chips: U51, U65, and U60 which are shown in Figure 8-15. EPROM U51 contains storage for 16K bytes of program instructions. Its contents are mapped between addresses 0000 and 3FFF (hex). The low-active PGM input of EPROM U51 at pin 27 is held high through jumper J1 (position A-C). If jumper J1 is moved to position A-B, logic level at pin 27 of the EPROM follows address bit A14. This jumper position was initially provided to accommodate a different type of EPROM. The jumper has no test or maintenance purposes and should be left in the A-C position.

RAM U65 provides storage for 1K bytes of TC information (video characters). Its contents are mapped between addresses 8000 and 83FF (hex). When the CPU is shifting TC information bytes and their corresponding addresses into the character generator FIFO registers, the same information is written into the same address in U65.

Position of the character display on the picture monitor is governed by addresses of the characters stored in RAM U65. When the position of the character generator display is adjusted (vertically or horizontally) on the picture monitor, characters are read out of RAM U65, new addresses are assigned, and characters are then written back into RAM storage. The RAM in the character generator (U24) cannot be accessed for this purpose. The CPU cannot read contents of the CG RAM inasmuch as it is isolated from data and address buses by one-way (write) FIFO registers. See paragraph 8-85 for details.

RAM U60 provides temporary storage for up to 2K bytes of program information storage. Its contents are mapped between addresses 8800 and 8FFF (hex).

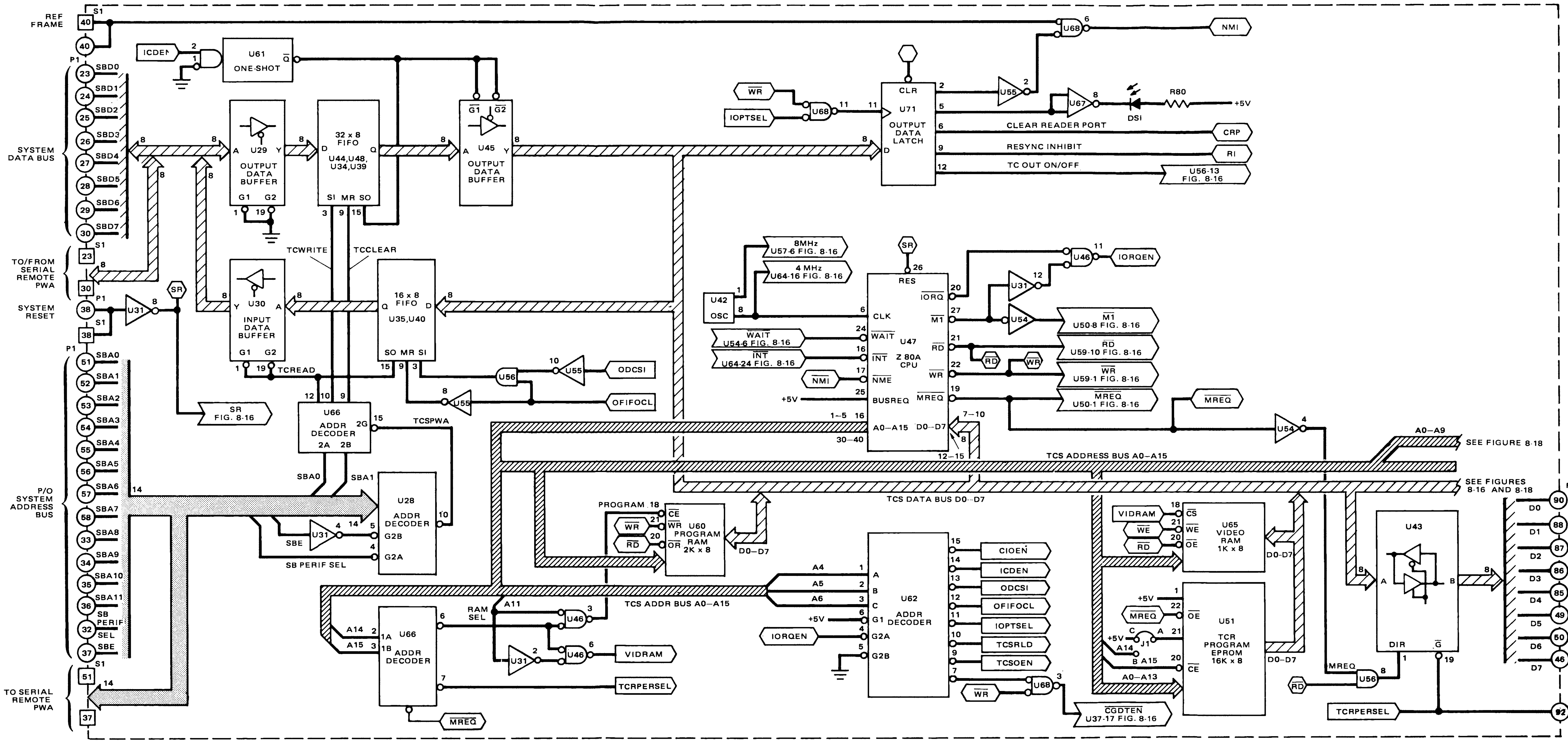


Figure 8-15.
CPU Kernel, Control Interface, and Data I/O Interface

8-74 Address Decoding. The TCS CPU kernel includes two address decoders, U66 and U62.

Decoder chip U66 contains two independent decoder circuits. Each decodes two address bits and can produce up to four outputs.

Section 1 of decoder U66 is enabled by MREQ from CPU U47. It decodes address bits A14 and A15 on the TCS address bus to produce either RAM SEL (RAM select) or TCR PERIF SEL (time-code reader peripheral select). The RAM select output at U66-6 is further broken down into enabling inputs for either program RAM U60 or video RAM U65 by gates U46-3 and U46-6 to which address bit A11 is applied.

The TCR PERIF SEL output at U66-7 enables bidirectional data buffer U43. It is also routed to PWA connector P1 contact 92. This decoded output has no function in the VPR-80.

Section 2 decodes system address bus bits SBA0 and SBA1 and produces commands from the control system CPU to the TCS PWA. It is enabled by address 4DXX from the system address bus. Refer to paragraph 8-75.

Address decoder U62 is enabled by IORQ from CPU U47. Control outputs of address decoder U62 and section 1 of decoder U66 are listed in Table 8-9.

Table 8-9. Primary Time-Code System CPU Commands

Address	Mnemonic	Source	Command
XX00	CIOEN	U62-15	**CIO enable**. Enables CIO U64.
XX10	ICDEN	U62-14	**Input command and data enable**. Enables output data buffer U45 and then clears output FIFO U34/U39/U44/U48.
XX20	ODCSI	U62-13	**Output data and command shift in**. Shifts time-code byte through input FIFO U35/U40 and input data buffer U30 (enabled by TCREAD) to system data bus.
XX30	OFIFOCL	U62-12	**Output FIFO clear**. Clear input FIFO U35/U40 (input FIFO to control system CPU)
XX40	IOPTSEL	U62-11	**I/O port select**. Clocks output data latch U71 on write cycle: enables input data buffer U38 on read cycle.

(Continued next page)

Table 8-9. Primary Time-Code System CPU Commands (Continued)

Address	Mnemonic	Source	Command
XX50	TCSRLD	U62-10	**Time-code shift register load.** Parallel loads time-code byte into serial time-code shift register U70.
XX60	TCSOEN	U62-9	**Time-code shift out enable.** Shifts time-code byte from gate array U7 into time-code reader FIFO U52/U58
XX70	CGDTEN	U62-7 (gate 68-3)	**Character generator data transfer enable.** Shifts time-code byte out of time-code reader FIFO U52/U58 and clears character generator FIFOs U17/U18/U19/U21/U26.
8XXX	RAM SEL	U66-6	**RAM select.** Applied to gates U46-3 and U46-6 for further decoding with address bit A11.
8800-8FFF	PRGRAM	U46-3	**Program RAM.** Selects program RAM U60.
8000-83FF	VIDRAM	U46-6	**Video RAM.** Selects video RAM U65.
CXXX-FXXX	TCR PERIF SEL	U66-7	**TCR PERIF SEL.** Enables bidirectional data buffer U43 and supplies controlling logic level to external device.

8-75 Control System Interface

The control system CPU accesses the TCS PWA as a peripheral. Accordingly, information transfers between the TCS PWA and the control system CPU are made via the system data and address/control buses in the motherboard.

When information is transferred, decoded address M4 (PERIF SELECT) enables bidirectional machine data buffer 6U28. This connects the Control PWA data bus to the system data bus. Direction of transfer is controlled by the logic level of the R/W output of the control system CPU. (Refer back to Figure 6-2 in Section 6.) At the same time, an address word composed of bits SBA0, SBA1, SBA8—SBA11, enabling strobe SBE, and SB PERIF SEL is placed on the system address/control bus through permanently enabled machine address buffer 6U29.

As shown in Figure 8-15, SB PERIF SEL (low), SBA11 (high), and SBE (low) enable secondary address decoder U28. SB PERIF SEL is decoded address 4XXX in hexadecimal (hex) notation. Address bits SBA8—SBA10 are decoded by U28. When the latter three bits form a hex 5, the Y5 output of decoder U28 (4DXX) enables section 2 of dual 2 x 4 decoder U66. Decoder U66 looks at address bits SBA0 and SBA1 and decodes one of three primary commands from the control system CPU to the TCS PWA logic: read, write, or clear. These instructions are listed in Table 8-10.

Table 8-10. Control Interface Commands

Address	Mnemonic	Source	Command
4DXX	TCSPWA	U28-10	**Time-Code System PWA**. Enables section 2 of decoder U66.
4D00	TCREAD	U66-12	**Time-code read**. Enables data buffer U30 and shifts one byte of data from FIFO U35/U40 to system data bus.
4D02	TCWRITE	U66-10	**Time-code write**. Shifts one byte of data from system data bus into FIFO U34/U39/U44/U48.
4D03	TCCLEAR	U66-9	**Time-code clear**. Resets FIFO U34/U39/U44/U48.

8-76 **Output from VTR to TCS.** The data path from the VTR control system to the TCS is through output data buffer U29, which is permanently enabled. Buffer outputs are applied to FIFO U34/U39/U44/U48, which can store 32 data bytes. Data is shifted into the FIFO by TCWRITE from U66-10. The FIFO is filled by 32 assertions of TCWRITE. The TCS then reads the data by asserting ICDEN. ICDEN enables output data buffer U45, thus placing the first data byte on the TCS data bus. The trailing edge of ICDEN triggers one-shot U61-4 which, in turn, clears the input FIFO on the trailing edge of its low output pulse.

8-77 **Input to VTR from TCS.** The data path from the TCS to the VTR control system is through input FIFO U35/U40 and input data buffer U30. The FIFO, which can hold 16 bytes, is cleared by OFIFOCL from decoder U62-12. Data is shifted into the FIFO by ODCSI from U62-13. The control system reads the data by asserting TCREAD at U66-12. TCREAD enables input data buffer U30, thereby placing the first data byte on the system data bus. The trailing edge of TCREAD triggers one-shot U61-12 which, in turn, shifts the next data byte to the output of FIFO U35/U40. A total of 16 assertions of TCREAD shifts the entire contents of FIFO U35/U40 to the control system CPU via the system data bus.

8-78 Time-Code Reader/Generator

The heart of TC reading and generation is counter/timer and parallel I/O unit (CIO) U64, which is shown in Figure 8-16. Specifications of the CIO chip (Zilog Z8536) are given in Appendix A of the *VPR-80 Parts Lists and Schematics* manual. The CIO is Ampex Part No. 001-894. Its achitecture is quite complex (i.e., 48 internal

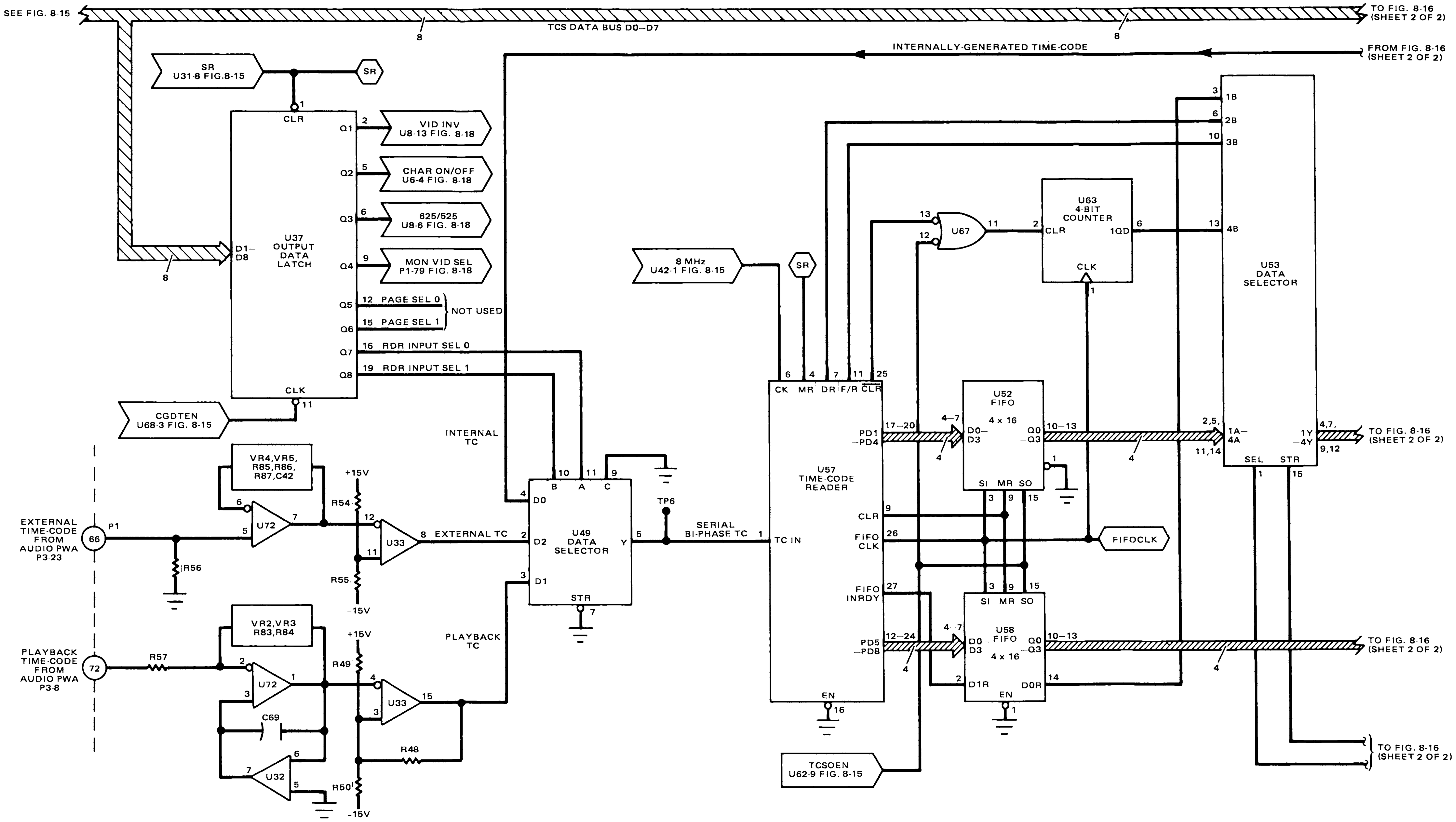


**Figure 8-16.
Time-Code Reader/Generator
(Sheet 1 of 2)**

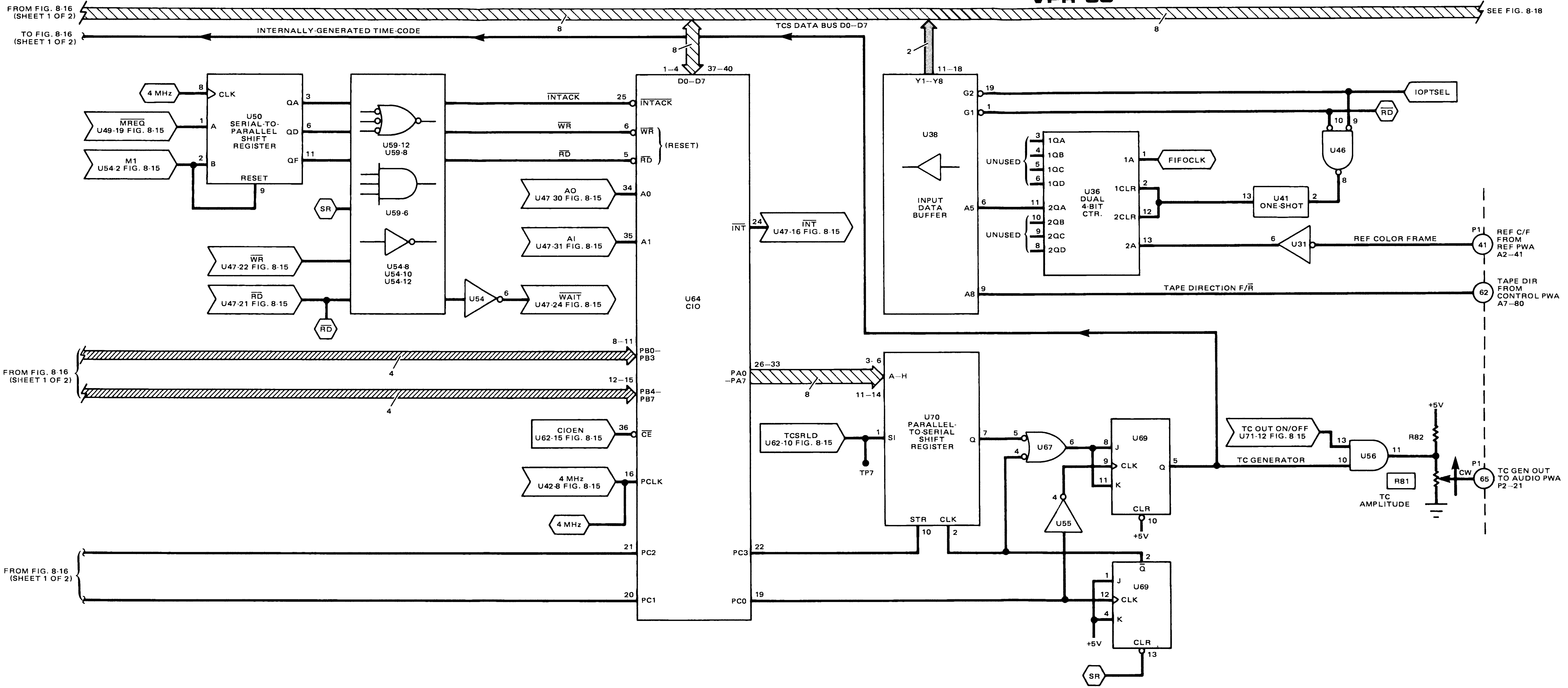


Figure 8-16.
Time-Code Reader/Generator
(Sheet 2 of 2)

registers), and it is extremely versatile. Therefore, only those characteristics, capabilities, and requirements which play a role in TC reading and generation are mentioned here.

CIO U64 contains three bidirectional I/O ports and three counter/timers, each of which is independently addressable and programmable. Ports A and B are 8 bits wide, and port C is 4 bits wide. Port A (PA0--PA7) is used as output port in TC generation. Port B (PB0--PB7) is used as input port for TC reading. Port C (PC0--PC3) is used for control outputs from CPU U47 for governing operation of the TCR and TCG.

All registers in CIO U64 (command, status, and data) are readable, and, except for status bits, writable. Each register has its own unique internal address so that any register can be accessed in two operations. All data registers can be directly accessed in a single operation. In addition, the CIO contains programmable pattern-recognition logic. This feature is used to signal the CIO when to accept TC bytes from the TCR and place them on the TCS data bus to CPU U47.

As shown in Figure 8-16, the CIO is interfaced with CPU U47 by interrupt acknowledge (INTACK) and reset generator circuits U50, U54, and U59. The reset does not have a reset input. The CIO is reset when RD and WR inputs are asserted (detected low) at the same time.

8-79 Serial Time-Code Format. The internationally specified TC format is serial bi-phase mark (Manchester I) time code. It is self-clocking, which allows decoding over a wide range of speeds. There is no dc component, and inversion of the signal is immaterial, facilitating transmission of time code to VTRs at remote locations.

In bi-phase mark time code, a transition occurs at the start of every bit cell. Direction of transition (and therefore polarity of the signal) has no significance. If the bit is a ONE, an extra transition is made in the middle of the bit cell. If the bit is a ZERO, the dc level remains steady until transition at the start of the next bit cell. The time-code waveform shown in Figure 8-17 represents 10010110 followed by four ZEROs and repetition of the 8-bit word.

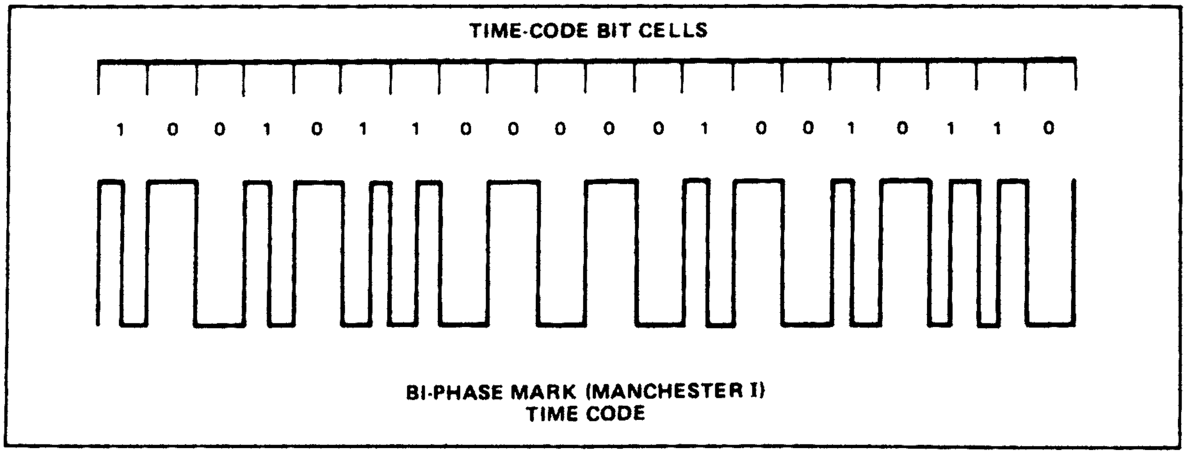


Figure 8-17. Serial Time-Code Format

8-80 Time-Code Reader. TC can be presented to the TCR from any of three sources: off-tape TC when in play modes, TC from an external TCG, or TC which is generated on the same PWA. Selector U49 (Figure 8-16) is a three-way switch for selecting the source of TC to be applied to TCR U57 and displayed on the picture monitor by the character generator.

Internally generated TC from TCG circuit U69-5 is applied to the D0 input of selector U49.

Playback TC from audio channel 3 is applied to the TCS PWA at connector P1, contact 72. The TC signal is routed to VR3, U72-1, VR2, and U32-7. These components form an adaptive slicer and pulse former which adjust the input signal from the Audio PWA to nominal dc logic levels with clean edges. The output of U72-1 is applied to Schmitt trigger circuit U33-15. The serial TC output of U33-15 is applied to the D1 input of selector U49.

Externally generated TC from audio channel 3 is applied to the TCS PWA at connector P1, contact 66. The TC signal is routed to U72-7, VR4, and VR5. These components form an adaptive slicer and pulse former which adjust the input signal from the Audio PWA to nominal dc logic levels with clean edges. The output of U72-7 is applied to Schmitt trigger circuit U33-8. The serial TC output of U33-8 is applied to the D2 input of selector U49.

Q7 and Q8 outputs of data latch U37 determine TCR input selection. Input selection logic levels are decided by the TC source setup established by the operator. Q1--Q6 outputs of data latch U37 are character generator and monitor video controls. See paragraph 8-82.

Selector output at U49-5 is serial TC at logic level. Serial TC (test point TP6) is applied to pin 1 of TCR U57. U57 is a longitudinal gate array (Ampex Part No. 1467711). Its internal operation is clocked by the 8-MHz output of oscillator U42 (Figure 8-15). U57 is essentially a parallel-to-serial converter. It syncs on the 16-bit sync word within the TC word, and then assembles TC time or user information words in byte slices. When 16-byte TCR FIFO U58/U52 asserts FIFO INRDY (high) at pin 27, U57 asserts FIFO CLK which is the FIFO shift-in clock. Parallel byte outputs of U57 are thus shifted into the TCR FIFO.

Bits PD5--PD8 at the output of U57 are shifted through FIFO chip U58 and are then presented directly to the input port (B) of CIO U64. Bits PD1--PD4 of the TC byte, however, are first routed through selector U53 before arriving at the CIO input port.

Bits PD1--PD4 at the output of FIFO U52 are presented to the four channel A inputs (1A--4A) of data selector U53. The PC1 output of CIO U64 is the channel select input to U53. The CIO PC1 output first selects channel B inputs. The CIO examines them to determine when it is time to switch to channel A inputs and shift out FIFO contents into the CIO input port. Channel B inputs are data ready (DR) and forward/reverse (F/R) from U57, data output ready (DOR) from FIFO U58, and the bit 4 output from counter U63.

Counter U63 is a 4-bit counter, and is clocked by FIFO shift-in pulses. Counter U63 is also a window generator. When the bit 4 output of U63 goes high, a window is opened (interval is begun) during which pattern recognition logic in CIO U64 looks for 1X11 at its PB0--PB3 inputs. When the CIO detects this input pattern, it generates an interrupt (INT). CPU U47 services the interrupt by asserting time-code shift out enable (TCSOEN) at decoder U662-9 (Figure 8-15), and TC bytes are shifted out of the TCR FIFO. The CIO then reads the TC bytes from TCR FIFO U52/U58 and sends them to CPU U47 via the TCS data bus.

Counter U36 is a dual 4-bit counter. Section 1 of U36 (1QA--1QD), which is clocked by FIFOCLK pulses, counts TC bytes shifted into TCR FIFO U52/U58. This function is part of a flywheel counter; however, this hardware implementation has since been taken over by software enhancement. Thus, section 1 of U36 is not actually used.

Section 2 of U36 (2QA--2QD) is clocked by inverted reference frame pulses (REF C/F) from the Reference PWA. REF C/F, counted down 2 to 1, is thereby made available to CPU U47 at the Y5 output of input data buffer U38. Tape direction logic level (high = forward, low = reverse) from the Control PWA is applied directly to input data buffer U38. CPU U47 samples the tape direction logic level once per frame.

8-81 Time-Code Generator. Output port A of CIO U64 produces parallel bytes of TC according to the selected operating mode (run, hold, sequence, jam, or slave mode). TC bytes are applied to parallel-to-serial shift register U70 which is clocked by flip-flop U69-2. Shift register U70 converts the TC bytes to serial NRZ TC at U70-7. The NRZ signal is applied to the J/K inputs of U69-2 through gate U67-6. Normal and inverted PC0 output of CIO U64 clocks flip-flops U69-2 and U69-5.

When the inverted NRZ signal at the J/K inputs of U69-5 is low, the Q output goes high on the clock pulse. When the J/K inputs of U69-5 are high, the flip-flop output toggles on the clock pulse. Flip-flop U69-2 toggles at the rate set by the PC0 output of CIO U64. Its output clocks flip-flop U69-5 through gate U67-6, and thereby provides the extra transition in the NRZ signal when the bit cell contains a ONE.

Thus, the signal at U69-5 is serial bi-phase mark TC. The TC signal output is gated at U56-11 by the logic level of TC OUT ON/OFF from output data latch U71 (Figure 8-15). The TC output of gate U56-11 is routed through R81 to the PWA output at connector contact P1-65. R81 provides TC output amplitude adjustment. The TC output at P1-65 is routed to P2-21 on the Audio PWA. The TC output at U69-5 is routed back to TCR input selector U49-5.

8-82 Character Generator

Design of a video character generator (CG) is usually afflicted with a time-share problem. The conflict is between writing PROM addresses in the RAM and reading the RAM (and thus accessing PROM contents). This conflict causes black or white flashes in the character video on the picture monitor. The design of the TCS PWA avoids this problem. FIFO registers are employed for both data and address information going to the RAM, and timing circuitry provides control over noninterfering FIFO shift-out pulses and access to the RAM and CG PROM. Figure 8-18 shows the principal CG circuits.

8-83 **Monitor/Character Video Path.** Monitor video output of the TBC is connected to the VPR-80 at J8 (AUX) on the I/O connector panel. Monitor video enters the TCS PWA at connector contact P1-91 and is routed to video amplifier Q8/Q11/Q12. Transistor Q5 is a current source at the amplifier output which is routed to the monitor/auxiliary video switching network on the Reference PWA at connector contact P1-75. Adjustment of unity gain is provided by R42, and C21 is adjusted for flat frequency response during multiburst.

When a VPR-80 is equipped with a TCS PWA, the monitor video select (MON VID SEL) logic level at PWA connector contact P1-79 is held low by CPU U47. When low, MON VID SEL switches the auxiliary output at P1-75 (monitor video with inserted character display) to the picture monitor. If the MON VID SEL logic level were high, the switching network on the Reference PWA would route demod video (without character display) to the picture monitor.

The monitor video chroma is stripped by low-pass filter L2/C18/C14. Transistors Q1/Q2/Q3 are the sync stripper. Vertical drive (V), horizontal drive (H), and feedback clamp pulses are derived from the stripped composite sync signal (TP3).

One-shot U1-12 and flip-flop U6-8 are the broad pulse detector. Vertical (V) pulses at U6-8 (TP5) drive the vertical counter. One-shot U2-13 is a 2H eliminator. Horizontal (H) pulses at U4-11 (TP2) drive the horizontal counter through horizontal position one-shot U1-4. The 3-µs output of one-shot U2-5 is the feedback clamp for the character amplifier.

Characters can be turned on and off by modifying current through CR6/Q13/Q14. Characters are substituted for monitor video when control circuit U6-5 goes low. Transistors Q13 and Q14 turn off video amplifier Q8/Q11/Q12 and turn on character amplifier Q6/Q9/Q10. Q5 is a current source for both video and character amplifiers. Back porch is sampled and held for the character insertion through FET Q7 which is driven by the 3-microsecond clamp output of U2-5. When characters are substituted for video, Q4 does the black/white switching. Black level is adjusted with R20, and white level is adjusted with R7. B/W rise and fall times are controlled by L-C network L3/C13/C15.

8-84 **Character (Font) Storage.** Character information is stored in 8K x 8 PROM U16. Large and small sizes of one font of characters are stored in 2K of the available 8K of storage. Character information is accessed by PROM address bits A0—A10 which are generated by the vertical counter (A0—A2) and read from RAM storage (A3—A10). PROM address bits A11 and A12, which would access the remaining 6K of storage, are not used.

As shown in Figure 8-19, small size characters are 16 lines high by 8 dots (pixels) wide. Therefore, 16 bytes of character information must be read from PROM U16,

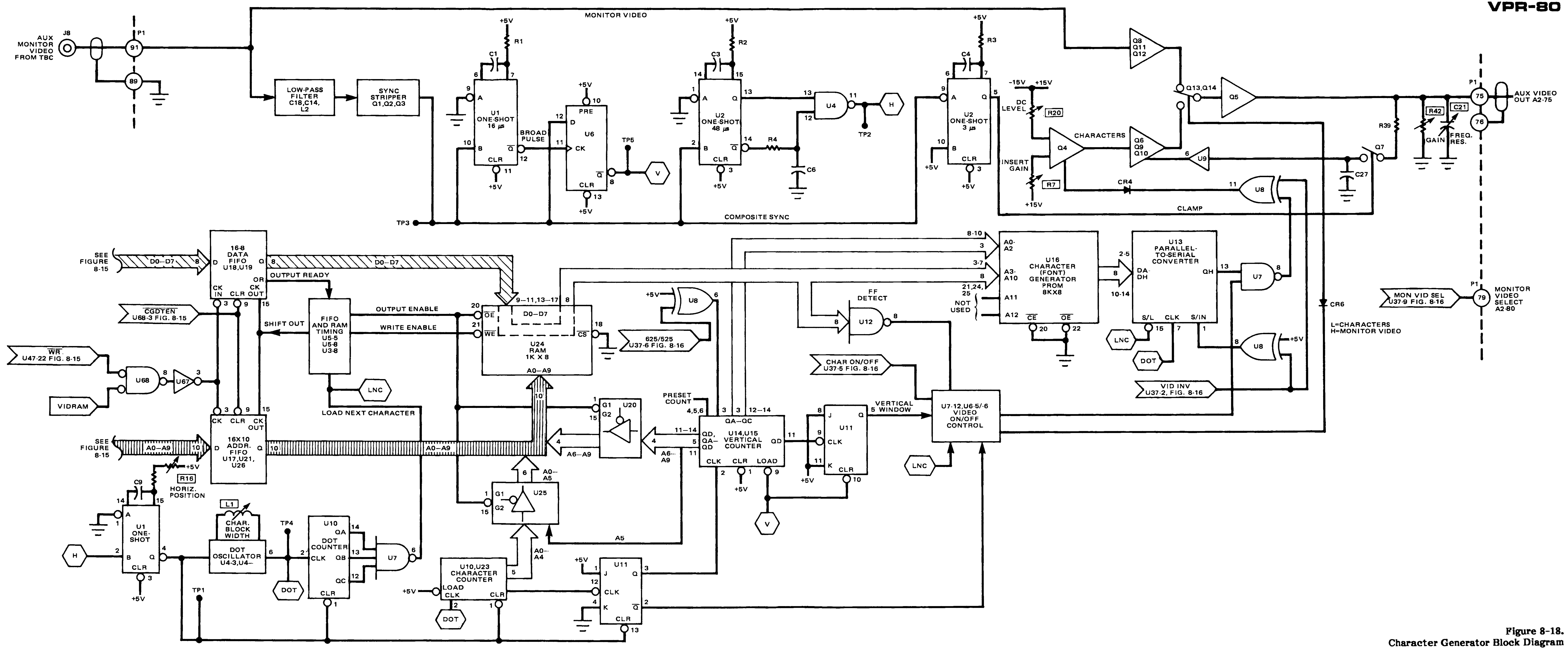


Figure 8-18.
Character Generator Block Diagram

converted from parallel to serial procession, and synchronously inserted in the monitor video output. Each 16-byte block of character information from U16 constitutes a small-size character.

Large-size characters are 32 lines high by 16 dots wide. When large characters are selected for display, four 16-byte blocks of character information are read from PROM U16. Each block contains one quarter of the whole large character information. Thus, the required monitor screen area for the character is increased by four, and each large-size character is composed of four small-size character blocks of information.

The 16-byte blocks of character information are accessed by PROM address bits A3—A10 which are stored in RAM U24. Individual bytes of character information within the block are accessed by PROM address bits A0—A2 which are generated by vertical counter U11/U14/U15. Eight bytes of information are read from PROM U16 per field.

The sequence of bytes at the PROM output proceeds first by line (controlled by vertical counter) and then by character (controlled by character counter). The sequence is explained in detail in paragraph 8-89.

8-85 **Accessing RAM Storage.** Character generator RAM U24, shown in Figure 8-18, has storage capacity of 1K bytes. TC information bytes from CPU U47 are written into RAM U24 through 16 x 8 data FIFO U18/U19. Corresponding 10-bit addresses for TC information bytes are applied to RAM U24 through 16 x 10 address FIFO U17/U21/U26. The CPU clears FIFO registers by asserting character generator data transfer enable (CGDTEN) before shifting in TC information bytes.

Since RAM U24 is connected to TCS data and address buses through FIFO registers, which are one-way devices, the CPU cannot read RAM contents. Therefore, each time data is written into RAM U24, the same data is also written into the same address in video RAM U65 (Figure 8-15). WR and VIDRAM are AND-gated by U68-8 (Figure 8-18), and the buffered and inverted AND gate output shifts TC information bytes and their corresponding RAM addresses into FIFO registers U19/U19 and U17/U21/U26. At the same time, WR and VIDRAM enable the same information to be written into the same address in RAM U65. The CPU can read this information from U65 by asserting RD and VIDRAM.

When 16 bytes and their RAM addresses have been shifted into FIFO registers, the output ready (OR) level at U19-14 goes high. TC information bytes are then quickly written into RAM U24 during the quiet part of the cycle (when not reading data out of CG PROM U16). Timing circuitry, composed of U7-6, U5-5, and U5-8, and U3-8, generates shift-out pulses to FIFO registers and write enable (WE) pulses to the RAM. OR output at U19-14 is asynchronous. OR is asserted near the center of the character generation time slot.

The load next character (LNC) output of gate U7-6 goes high at the beginning of the interval for writing to RAM U24. This level shift clocks U5-5, initiating the timing and control sequence which asserts FIFO shift-out and RAM WE pulses.

Once data has been written into RAM U24 (and into RAM U65) it will appear at a fixed location on the monitor screen. If it is desirable to move the location of the CG display, its addresses in RAM storage must be changed so that it can be read out earlier or later. This manipulation is done by reading RAM U65, assigning new addresses to the bytes, and then writing them back into RAMs U24 and U65.

When gate U7-6 detects the count of 8 in the dot counter, its output goes low. This output (LNC) clears U5-5 and U5-8 and ends the write interval to RAM U24. The WE output at U3-8 goes high, and the RAM output enable (OE) level at U5-5 is asserted (low). At the same time, the low output at U5-5 enables tristate buffers U20 and U25. Enabled buffers allow count outputs of vertical and character counters to access the RAM on read cycles.

The TC information bytes in RAM U24 are actually addresses for accessing CG PROM U16. Therefore, details of reading RAM U24 (and thus PROM U16) are included in the following paragraphs on the character counter, vertical counter, and accessing character information in PROM U16.

8-86 **Dot Oscillator and Counter.** All changes in position of the CG display on the picture monitor are handled by software-programmed response to manual adjustments. The only adjustments which are dealt with solely in the hardware domain are those of horizontal position offset and character block width. Horizontal position offset is controlled by the output pulse width of one-shot U1-4. As shown in Figure 8-18, line rate (H) pulses U4-11 trigger one-shot U1-4. The adjustment of R16 controls the delay from horizontal drive (H) when dot oscillator U4-3/U4-6 starts, when dot counter U10 is clocked, when LNC is generated, and when character information is read from PROM U16. The adjustment of R16 thus sets the farthest left-hand boundary on the picture monitor screen where the CG display can begin. See Figure 8-20. Manually entered adjustments of horizontal position, as explained in paragraph 8-66, are accomplished by the CPU and its firmware. However, for any adjustment, the left-hand boundary is fixed by setting R16.

The dot oscillator is composed of U4-3, U4-6, and L1. It is stopped and then synchronously restarted by delayed H (TP1). Its output frequency is adjusted with L1. Oscillator output frequency (5 MHz nominal) controls character block width. Oscillator output (TP4) clocks dot counter U10 and character counter U10/U11/U23.

Adjustments of R16 and L1 are slightly interactive, and are explained in paragraph 8-95.

The 3-bit dot counter is composed of QA--QC stages of U10. It is cleared by delayed H (TP1), and is clocked by the dot oscillator (TP4). Each time the count of 8 dots is reached, gate U7-6 generates load next character (LNC). LNC clears U5-5 and U5-8, thus synchronizing the FIFO shift-out and RAM write enable timing network. LNC also controls shift/load input of parallel-to-serial shift register U13. When LNC goes low at U13-15, the next character from PROM U16 is parallel loaded into shift register U13. The dot oscillator output then clocks the character information out of U13 in serial procession to video insertion circuits.

8-87 Character Counter. The 5-bit character counter is composed of the QD stage of U10 and the QA--QD stages of U23. Flip-flop U11-2/-3 is clocked on the count of 8. The counter is cleared by delayed H (U1-4), and it is clocked by the dot oscillator (U4-6). The dot oscillator also clocks character information out of parallel-to-serial converter U13. When the last bit of each video character byte has been clocked to video insertion circuits, the output of character counter U10/U23 advances one count. The count output is applied through enabled buffer U25 to the A0—A4 address inputs of RAM U24. These address bits define the character address in U16, which is being accessed from RAM U24.

When one byte (line) of character information has been read out of PROM U16 for each of the characters in the display, the QD stage of the character counter (U23-11) clocks J-K flip-flop U11-3/-2. States of this flip-flop define the horizontal window: cleared (reset) state = horizontal window open, set state = horizontal window closed. When clocked by U23-11, the cleared flip-flop changes to the set state, indicating that one line of character information has been shifted out to video insertion circuits, closing the horizontal window. Refer to Figure 8-20. The level at U11-3 goes high. This output clocks the vertical counter, U14 and U15, and the vertical count output (number of lines completed) advances by one.

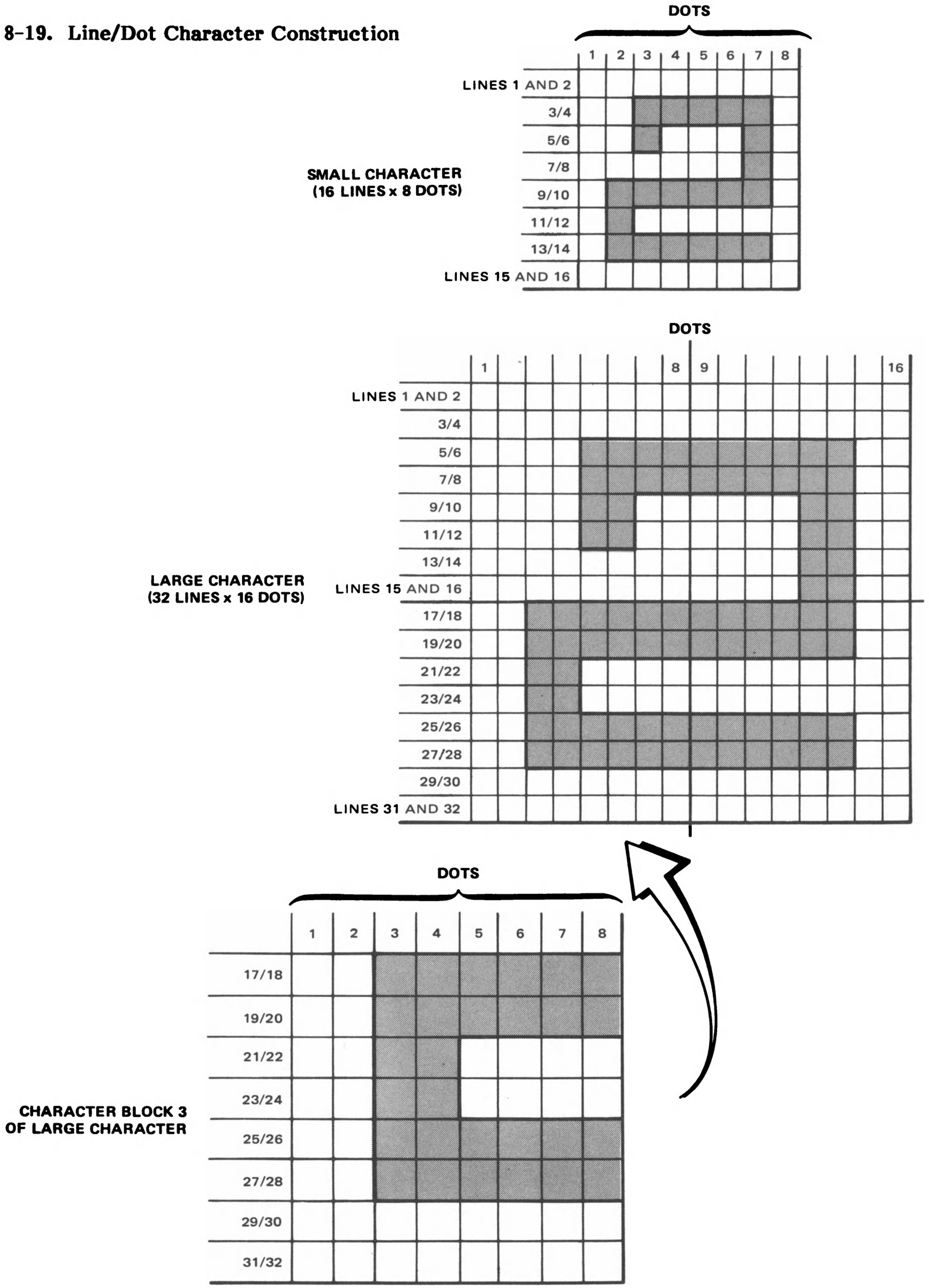
The level at U11-2 goes low when the horizontal window is closed. This output inhibits gate U7-12 in the video on/off control logic, which turns off character video, turns on monitor video, and inhibits insertion of character video at gate U7-8. Video on/off control logic is described paragraph 8-90.

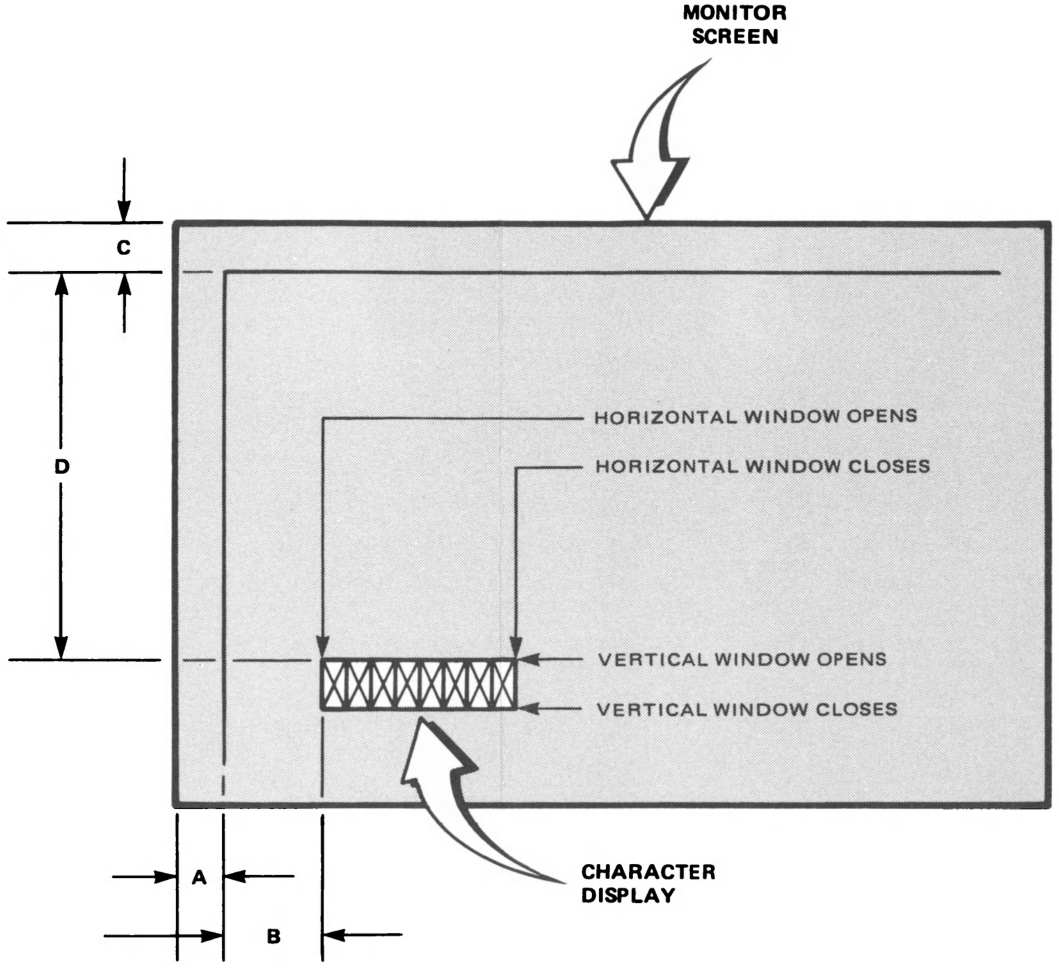
J-K flip-flop U11-3/-2 is cleared by the next delayed H signal from U1-4. The horizontal window is thus reopened when completed AND gate U7-12 output goes high. Video control logic then turns auxiliary video off, turns character video back on, and enables character video to be inserted through gate U7-8 as the next line of character video information is read from PROM U16.

8-88 Vertical Counter. Two 4-bit counters, U14 and U15, are combined to form the 8-bit vertical counter. Flip-flop U11-5 is clocked by the last stage of the counter. The vertical drive pulse (V from U6-8) loads a preset count in the counter. The preset count is 241 for 525-line video or 225 for 625-line video. The preset value depends upon the 625/525 logic level at exclusive OR gate U8-6. The negative-going edge of the vertical drive also clears U11-5. States of this flip-flop define the vertical window: cleared (reset) state = vertical window closed, set state = vertical window open. The low output at U11-5 inhibits gate U7-12 in the video control logic. The vertical window, thus closed, remains closed until the vertical counter reaches the count of 255.

The vertical counter is clocked by the count of 8 from the character counter when the horizontal window is closed. With preset value loaded by V, the vertical window remains closed until the MSB output of the vertical counter, U15-11, goes low on the count of 255. This requires 16 clock inputs for 525-line video (32 clock inputs for 625-line video). Even though the three LSB count outputs of the vertical counter are accessing A0--A2 of PROM U16, character video information from the PROM is not displayed because the low output at U11-5 (closed vertical window)

Figure 8-19. Line/Dot Character Construction





A = DELAY FIXED BY SETTING OF R16

B = DELAY VARIABLE BY SETUP MODE 33-2

C = DELAY FIXED BY PRESET OF VERTICAL COUNTER U14/U15

D = DELAY VARIABLE BY SETUP MODE 33-1

Figure 8-20. Character Display Position Variables

prevents it. The 16- (or32-) line count delay before the vertical window is opened is labeled C in Figure 8-20. Thus, a fixed delay from vertical interval is ensured before the vertical window is opened. With respect to monitor screen position, this represents the uppermost line upon which the character display can border.

When the counter reaches 255, the next count output is 000. Subsequent count outputs of the three LSB stages are applied to A0—A2 address inputs of PROM U16. The count output of the five MSB stages is applied through enabled buffers U20 and U25 to the A5—A9 address inputs of RAM U24. Therefore, the RAM is accessed by line count from the vertical counter and by character count from the character counter. The PROM addresses thus read from RAM storage are routed to the A3—A10 address inputs of PROM U16.

Outputs of the vertical counter first sequentially access all the odd-numbered lines (field 1) in each character, and then, after the second vertical interval (assertion of V), access all the even-numbered lines (field 2).

8-89 **Accessing Character Information.** The sequence of character information read from PROM U16 is as follows. Refer to Figure 8-18.

After the preset delay, explained in paragraph 8-88, the three parallel address outputs of the vertical counter access line 1 of field 1 at PROM U16 address inputs A0—A2. Four buffered parallel address outputs of the vertical counter and six buffered parallel address outputs of the character counter access character information in RAM U24 which is applied to the A3—A10 address inputs of PROM U16. Thus, the first byte (top line) of information is accessed for the first character.

The parallel count output (RAM address) of the character counter then advances through the second character to the last character in the display. Thus, the first byte (top line) in each character block is read from PROM U16 by sequentially advancing PROM address bits A3--A10. At the end of the line the horizontal window is closed and the vertical counter is clocked. The horizontal window is reopened when the next delayed H-pulse clears the character counter. (Horizontal window is explained in paragraph 8-87.)

The vertical counter then advances by one count (line), and the second line address for field 1 is presented to A0—A2 address inputs of PROM U16. Character information bytes in each block are then sequentially accessed from RAM U24 by the character counter. RAM outputs advance PROM address bits A3—A10 for each character to be displayed. This sequence continues until the vertical counter clocks U11-5 at the end of the eighth line of field 1, closing the vertical window. (Vertical window is explained in paragraph 8-88.) The vertical counter is then preset by V, and after the next 16 (or 32) counts, sequentially accesses character information for the 8 lines in field 2.

If small-size characters are selected, all the character information required for one frame will have been accessed when the last bit of line 8 information is accessed for the last (right-hand) character to be displayed. If large-size characters are selected, only character information for the top half of all characters in the display will have been accessed at the count of 8 from the vertical counter. The vertical counter must cycle through the count of 8 again to complete accessing character information for the bottom half of large-size characters.

Character information bytes read out of PROM U16 are applied in parallel to shift register U13. Load next character (LNC) from gate U7-6, which is produced by the dot oscillator and is synchronized to delayed H, parallel-loads each byte into U13. U13 is clocked by the dot oscillator, and bits of the character information bytes are applied to gate U7-8 in serial procession.

8-90 **Video On/Off Control.** Video on/off control logic is composed of gates U7-12, U7-8, U12-8, and flip-flop U6-5/-6, shown in Figure 8-18. Control logic ensures that four conditions are satisfied before allowing character video to be inserted in the monitor video output:

- Horizontal window is open,
- Vertical window is open,
- Byte read from RAM U24 is not all ONEs (FF), and
- Character video on/off control from CPU is on.

When the first three of the above conditions are met, all three inputs to AND gate U7-12 are high. Low gate output is applied to the D input of U6-5/-6. When U6-5/-6 is clocked by the load-next-character (LNC) pulse from gate U7-6, logic level at U6-5 is low, and U6-6 is high. When the last of the above conditions is met, the preset input to U6-5/-6 is high (not asserted). Thus, when U6-5/-6 is in the reset state, the low output at U6-5 turns character video circuits on and turns off monitor video circuits at Q13/Q14. At the same time, high output at U6-6 keeps gate U7-8 enabled, allowing insertion of character video in monitor video output.

If horizontal window (paragraph 8-87) or vertical window (paragraph 8-88) is closed, or if the byte (PROM address) read from RAM U24 is FF (hex), output of gate U7-12 is high. When U6-5/-6 is clocked by the next LNC pulse from gate U7-6, the level at U6-5 goes high also. The high output at U6-5 turns off character video and turns on monitor video at Q13/Q14. At the same time, low output at U6-6 inhibits gate U7-8, thereby preventing insertion of character video in monitor video output.

If CPU U47 sets the CHAR ON/OFF output at output data latch U37-5 (Figure 8-16) low, flip-flop U6-5/-6 is preset, and display of character video is inhibited as explained above.

When all four conditions for allowing character video to be displayed are again satisfied, the next LNC pulse from U7-6 will clock U6-5/-6 back to the reset state, and display of character video is again enabled.

8-91 **Black/White Inversion.** Black/white polarity of character video is established by setup mode 32 (paragraph 8-65) which allows the operator to choose a black background with white characters, or vice versa. The video inversion (VID INV) logic level from output data latch U37-2 (Figure 8-16) is thus set by the operator.

When black/white polarity is to be inverted, two logic inversions are necessary. Refer to Figure 8-18. First, serial character video bits at exclusive OR gate U8-11 must be inverted. Second, logic level at the serial input of the shift register (U13-1) must be inverted. The VID INV logic level is applied to exclusive OR gates U8-11 and U8-8 to accomplish required inversions.

8-92 Adjustments

The following characteristics of the video character generator and serial TC can be adjusted as necessary.

- Video gain and frequency response (paragraph 8-93)
- Black/white levels (paragraph 8-94)
- Block width and horizontal position (paragraph 8-95)
- Time-code output amplitude (paragraph 8-96).

In all adjustment preocedures it is assumed that the TCS PWA is mounted on an extender to provide access to adjustment controls and test points. The adjustment controls referenced in the following procedures are shown in Figure 8-25 at the end of this section of the manual. It is further assumed that adjustment procedures will be performed in the sequential order listed above.

8-93 Video Gain and Frequency Response

Check and adjust video gain and frequency response as follows:

STEP 1 Set up test equipment in accordance with Figure 8-21.

STEP 2 Set differential comparator for differential measurement with 5-MHz bandwidth.

STEP 3 Set output of insertion test signal generator for peak white level multiburst.

STEP 4 Turn on VPR-80 power.

STEP 5 Press EE: EE indicator should be lighted.

STEP 6 Adjust R42 (Figure 8-25) for a 1-volt ±10 mVp-p signal at VPR-80 MONITOR VIDEO OUT connector (J13).

STEP 7 Set differential comparator for nondifferential presentation at full bandwidth.

STEP 8 Adjust C21 for flattest frequency reponse to multiburst input.

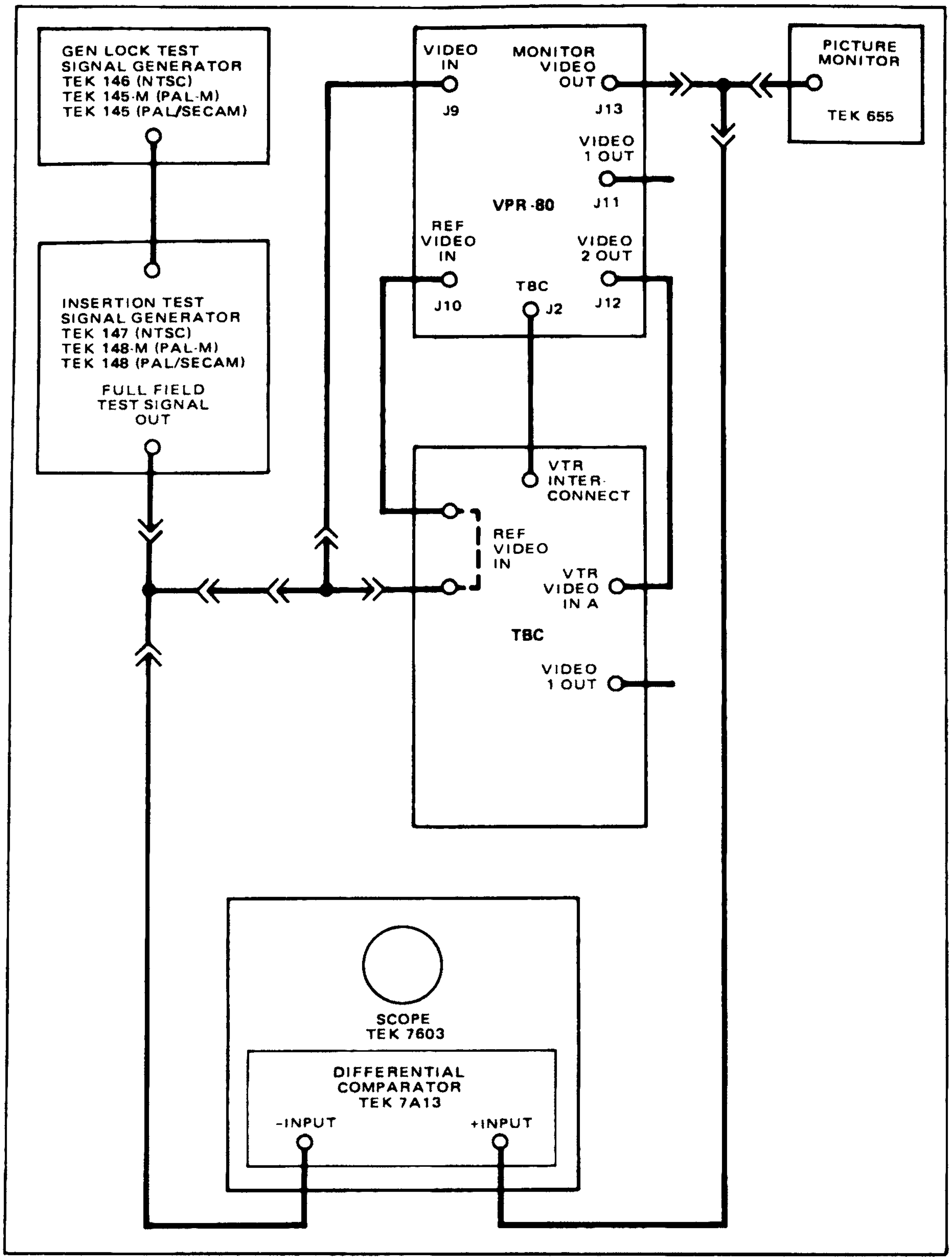


Figure 8-21. Video Gain and Frequency Response Adjustment Setup

8-94 Black/White Levels

Check and adjust black and white levels of character video as follows:

STEP 1 Verify that test equipment is set up in accordance with Figure 8-21.

STEP 2 Set output of insertion test signal generator for 50% peak white flat field.

STEP 3 Press ZERO.

STEP 4 Using setup mode 30-1, select tape timer for display. Refer to paragraph 8-63.

STEP 5 Using setup mode 32-2, select white background for character display. Refer to paragraph 8-65. Picture monitor displays a 50% peak white flat field, and the character display shows **TTM 00:00:00:00** (black characters on a white background).

STEP 6 Adjust R20 (black level) so that inserted black characters are 10% peak white level.

STEP 7 Adjust R7 (white level) so that inserted white background of character display is 90% peak white level.

8-95 Block Width and Horizontal Position

Block width adjustment control L1 and horizontal position adjustment control R16 are slightly interactive. Therefore, it is advisable to adjust these parameters at the same time. In addition, there appear to be unstable areas in the adjustment of R16. These unstable areas (evidenced by disturbances in the character video) are actually caused by the dot oscillator. Interactive adjustment of L1 eliminates these effects.

Adjust block width and horizontal position as follows:

STEP 1 Using setup mode 31-2, select small character display. Refer to paragraph 8-64.

STEP 2 Using setup mode 33-2, enable adjustment of character display horizontal position. Refer to paragraph 8-66.

STEP 3 Rotate tape speed control (shuttle) knob full ccw. Character display moves to left-hand side of picture monitor screen.

STEP 4 If necessary, adjust L1 to see that a full set of characters is displayed on picture monitor screen.

STEP 5 Adjust R16 as necessary to position character on left-hand side of character display in active video area of the picture monitor.

STEP 6 Adjust L1 to get a full display of character video across the screen.

STEP 7 Make sure that R16 has not been set to an unstable area in its adjustment range. If it has, repeat steps 5 and 6, as necessary, until there are no disturbances in the character video.

8-96 Time-Code Output Amplitude

Check and adjust TC output amplitude as follows:

STEP 1 Using setup mode 22-1, select internal TCG as source of information for character display. Refer to paragraph 8-52.

STEP 2 Using setup mode 23-1, select run mode of operation. Refer to paragraph 8-57.

STEP 3 Press EE switch: EE indicator should be lighted.

STEP 4 Observing AUDIO 3 meter on VPR-80 primary control panel, adjust R81 for an indication of +3 VU.

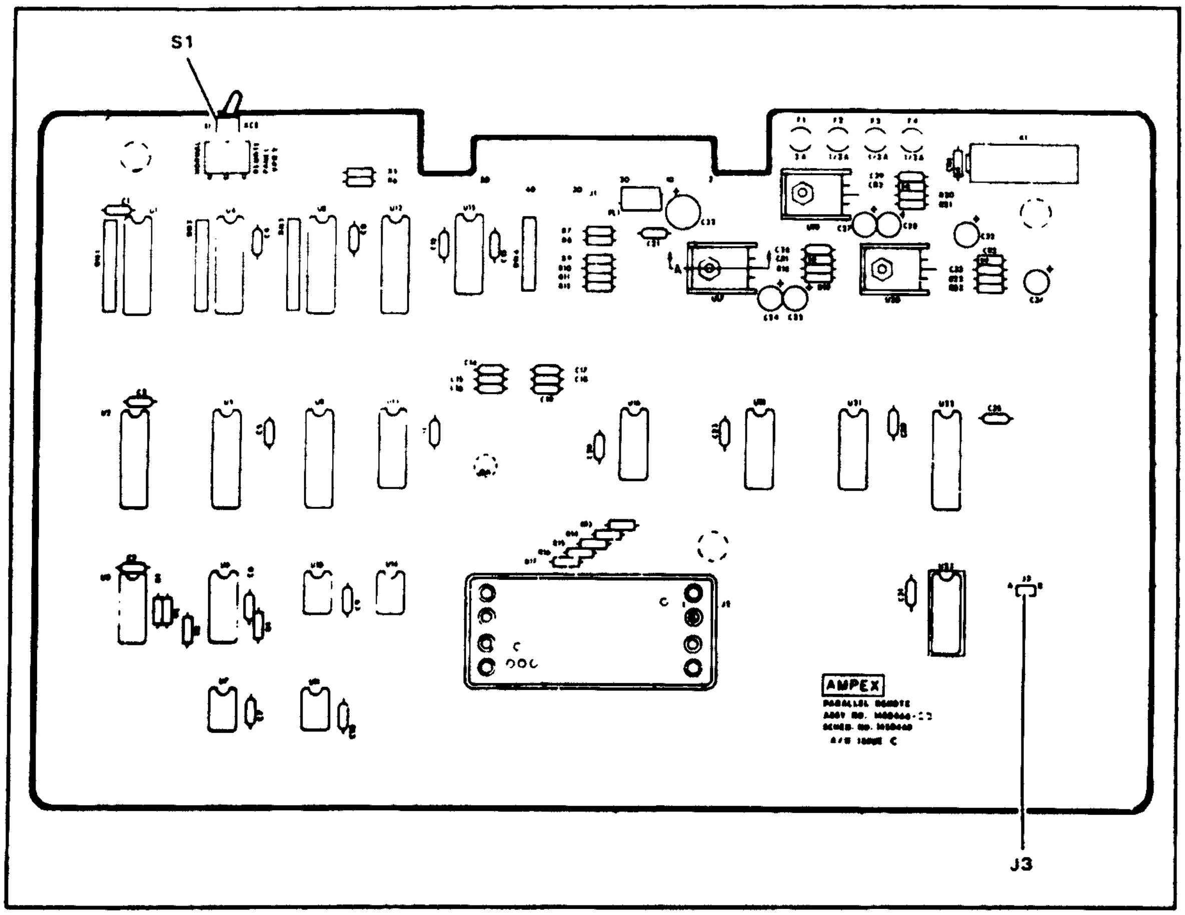


Figure 8-22. Parallel Remote PWA Mode Switch and Jumper

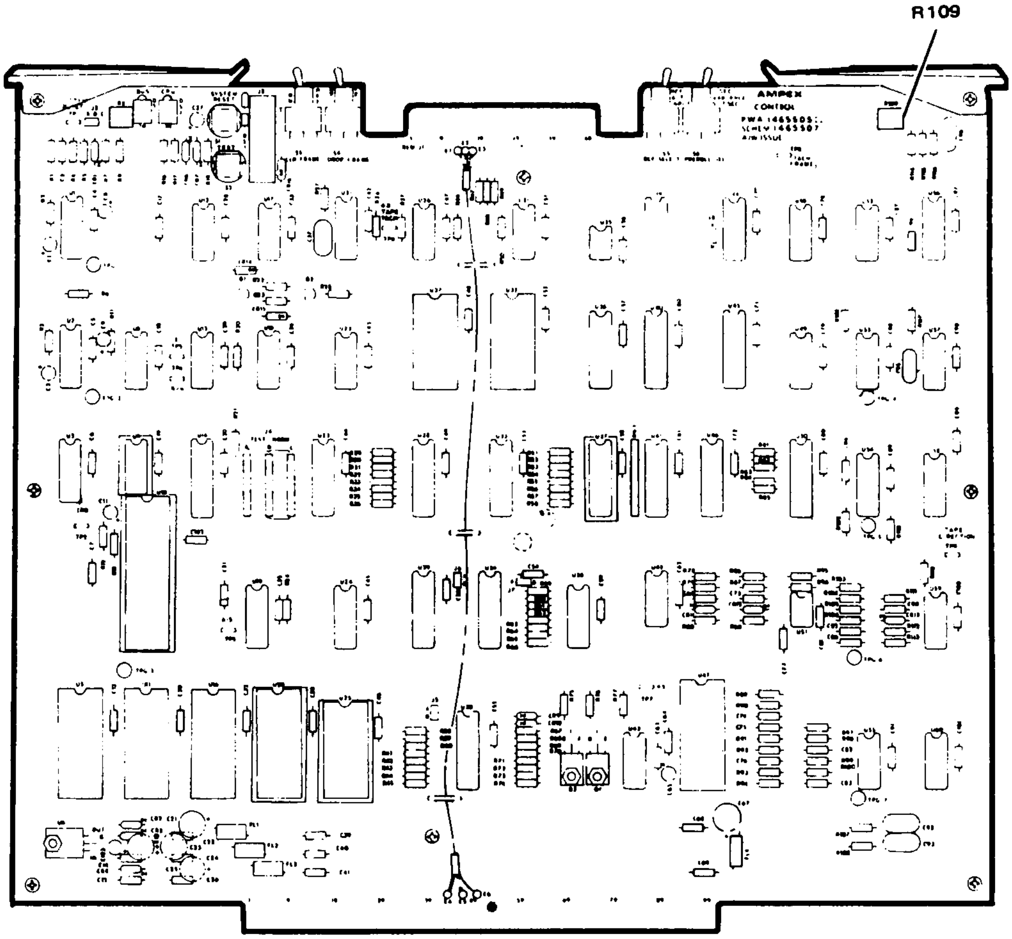


Figure 8-23. Control PWA Remote Shuttle Control Calibration

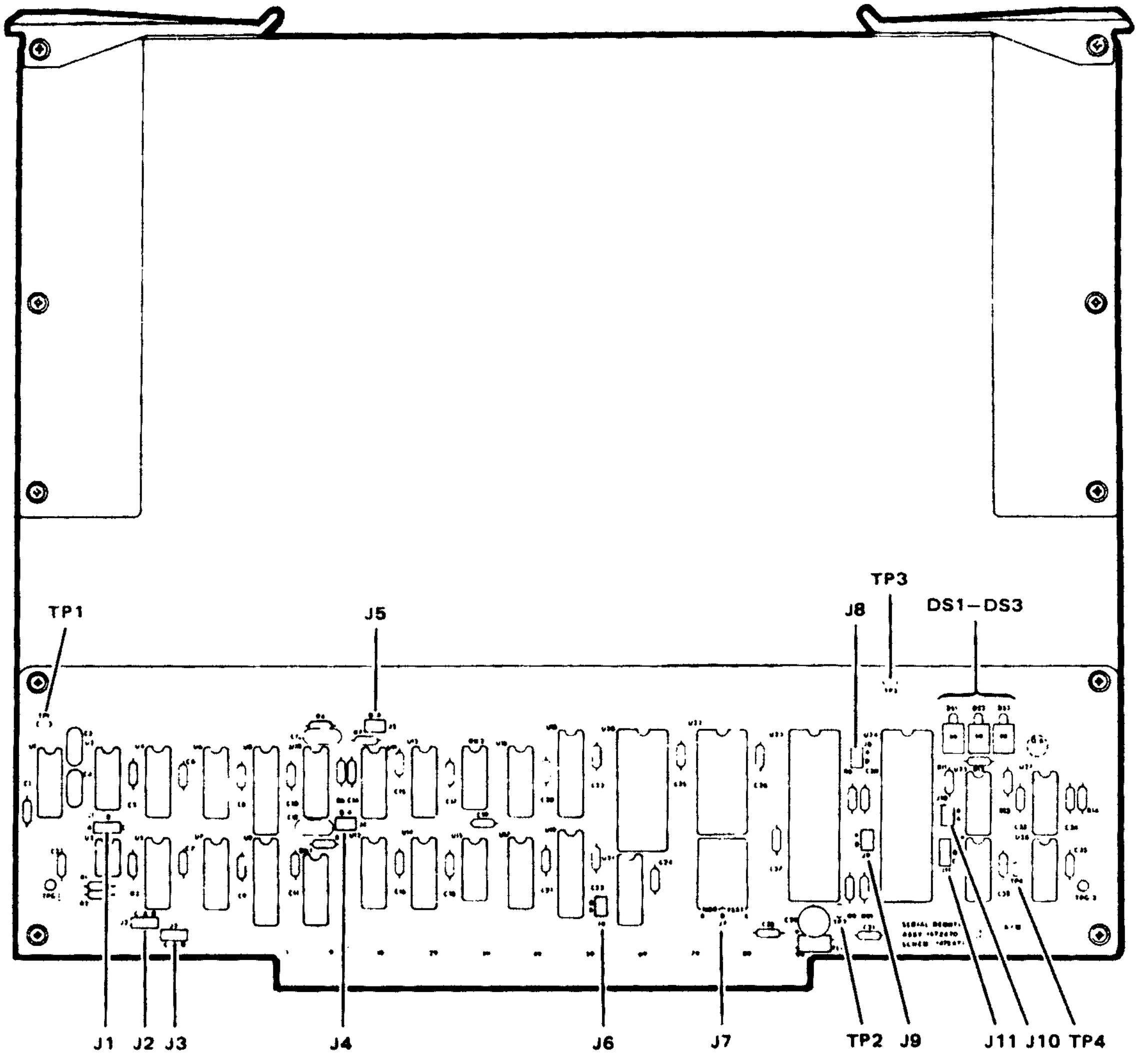


Figure 8-24. Serial Remote PWA
Test Points, Jumpers, and Indicators

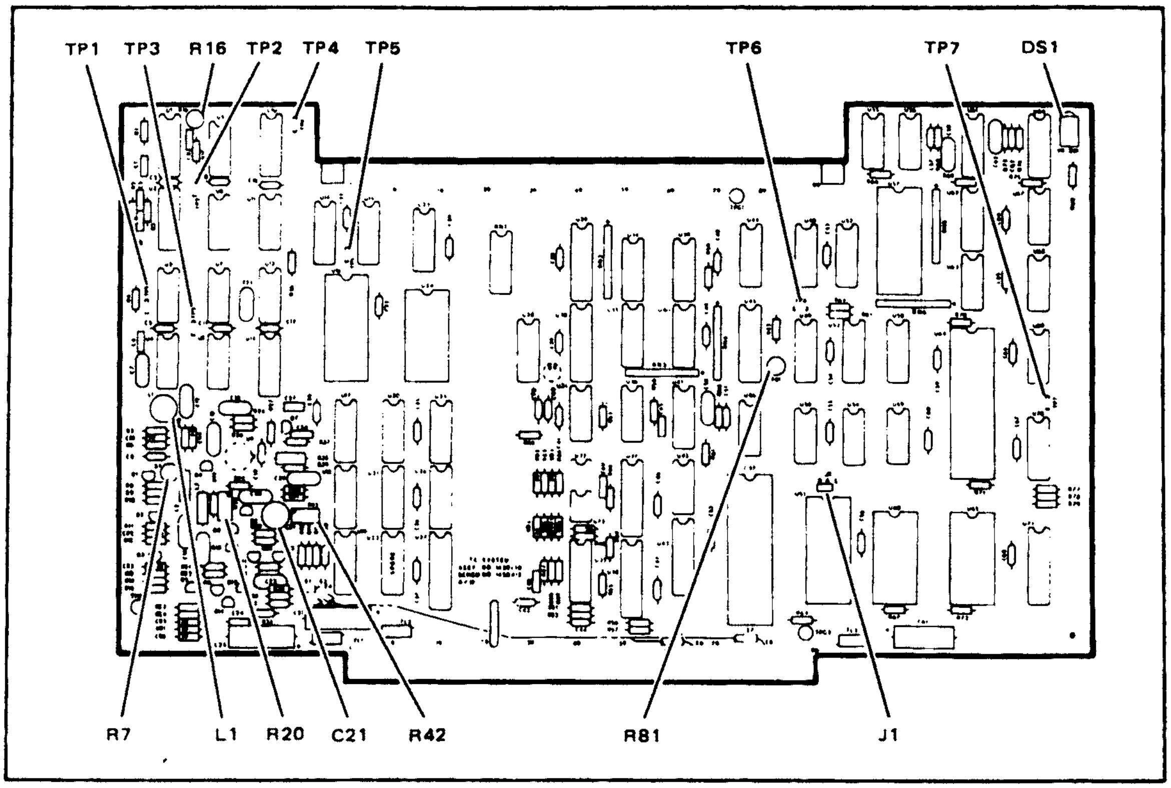


Figure 8-25. Time-Code System PWA Test Points, Jumpers, Indicators, and Adjustments

PART II
SECTION 9
DIAGNOSTICS

9-1 INTRODUCTION

The VPR-80 diagnostic program is specifically designed to assist both operator and service technician. The diagnostic program consists of six routines, including two background diagnostic routines that take place during initialization and operation, and four fault isolation routines, initialized by the operator or service technician. Diagnostic routines are easy to use and permit considerable flexibility in service and maintenance.

9-2 SCOPE OF THIS SECTION

This section covers VPR-80 diagnostic routines with instructions for exercising each routine and interpreting fault codes. Additionally, this section gives instructions for using the diagnostic probe to detect problems on key printed wiring assemblies (PWAs).

Operators and technicians should be familiar with the contents of the *VPR-80 Installation and Operation* manual, as well as other sections of this manual which give more detailed information for hardware troubleshooting by technical personnel.

9-3 VPR-80 DIAGNOSTICS AND EQUIPMENT

The six VPR-80 diagnostic programs are included in the operating system software, hardware, and accessories. To use the diagnostics, the following items are required:

- Diagnostic Probe Kit P/N 1450981
- Extender Board Assembly P/N 1450320
- NOP Processor PWA (Servo PWA CPU kernel) P/N 1430334

9-4 DIAGNOSTICS ORGANIZATION

VPR-80 diagnostics are organized into six parts, as shown in Figure 9-1.

The six diagnostics routines and their functions are:

- **Initialization Diagnostics.** When power is first applied, the control microprocessor performs an initialization check. After the control microprocessor completes its initialization, the servo microprocessor also performs an initialization check. When these checks are complete and no faults exist, the STOP button on the front panel will light. The VPR-80 is

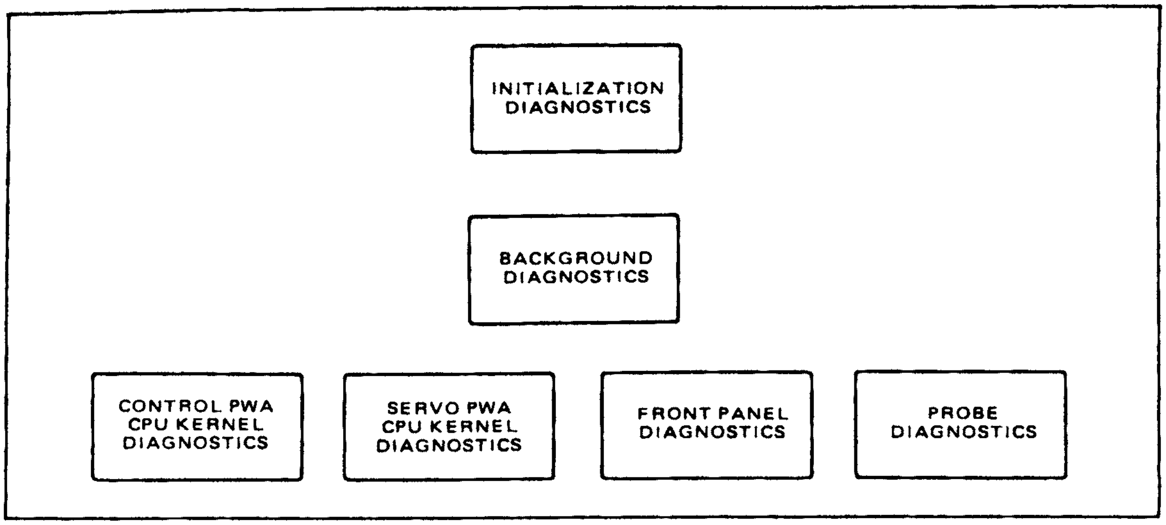

INITIALIZATION DIAGNOSTICS
BACKGROUND DIAGNOSTICS
CONTROL PWA CPU KERNEL DIAGNOSTICS
SERVO PWA CPU KERNEL DIAGNOSTICS
FRONT PANEL DIAGNOSTICS
PROBE DIAGNOSTICS

Figure 9-1. VPR-80 Diagnostics Organization

now in STOP-LOCAL-EE, with READY off (scanner not turning), and is ready for normal operation. If any part of initialization fails, the front panel STOP button will not light and/or a fault code will be displayed on the tape timer display. Also, if a fault exists a red bus fault LED on the edge of the Control PWA will light.

- **Background Diagnostics.** During normal operation a background diagnostic routine continually checks various operations. If a fault occurs during normal operation, the FAULT or SYSTEM lamp on the front panel will flash. The operator can press the FAULT or SYSTEM switch and a code indicating the fault will be displayed. In case of multiple faults, a stack of up to four fault codes is created. With each press of the switch the code for the next most recent fault to occur will be displayed.

- **Control PWA CPU Kernel Diagnostics.** A test jumper (J4) on the control PWA initiates a check of the Control PWA CPU kernel. When jumper J4 is moved to the test (A-B) position, it holds the data bus in the state 00000001. This is the machine code for a NOP (do nothing) instruction. This condition causes the control CPU to step through its address space one address at a time. The address bus will look like the output of a 16-bit counter.

- **Servo PWA CPU Kernel Diagnostics.** The Servo PWA CPU kernel can be checked by removing some components (see Figure 9-6) and installing a NOP processor (P/N 090-245) in place of the servo microprocessor. With the NOP processor installed, servo address lines will count from 0000 (hex) to FFFF (hex).

- **Control Panel Diagnostics.** Part of the diagnostic software run by the operator or service technician, this diagnostic routine checks functions of control panel switches and indicators, and displays codes indicating their status.

- **Probe Diagnostics.** Uses a diagnostic probe for fault isolation of VPR-80 circuit nodes. In general, holding the probe on a specified circuit node allows the control processor to send a signal to that node via the bus, and to confirm that the signal is correctly received by reading the probe. Alternatively, the control processor can inject a signal by driving the probe tip, and then confirm the circuit's integrity by reading the bus.

9-5 DIAGNOSTIC PROCEDURES

The following paragraphs detail diagnostic routines and procedures for using diagnostics to isolate faults. Each diagnostic routine is completely self-contained and is not dependent upon any other part of the diagnostics. Each routine is described individually with flowcharts of the routine or procedure where the routine is not automatic. Diagnostic routines are not necessarily designed to completely isolate a fault; rather, they are intended to perform confidence checks and isolate the fault to a particular PWA circuit. Table 9-1 (at the end of this section) lists fault codes and the circuit where the fault is most likely to have occurred. Within each flowchart, references are made to other sections of this manual for troubleshooting procedures to use once a fault is isolated. A section is also included for fault isolation should the VPR-80 fail to initialize and no fault code is displayed.

9-6 Initialization Diagnostics

A system reset condition begins when the VPR-80 is turned on or when the red system reset button on the Control PWA is pressed. The Control PWA microprocessor holds the system reset line while it performs its initialization checks. When the control microprocessor completes its initialization, the system reset line is lifted, allowing the servo microprocessor to perform its initialization. During initialization the microprocessors check the following:

Control PWA Checks

Internal RAM
External RAM
Timers
Interrupts
System Reset

Servo Communications
Battery Back-up Data
PROM Checksum

Servo PWA Checks

Internal RAM
External RAM
PROM Checksum
Control Communications

Figure 9-2 is a flowchart showing the sequence of events during initialization. Three kinds of problems can occur during initialization:

- VPR-80 failure without fault code display,
- Catastrophic fault that causes initialization abort, with fault code display, and
- Noncatastrophic fault that permits initialization, with fault code display.

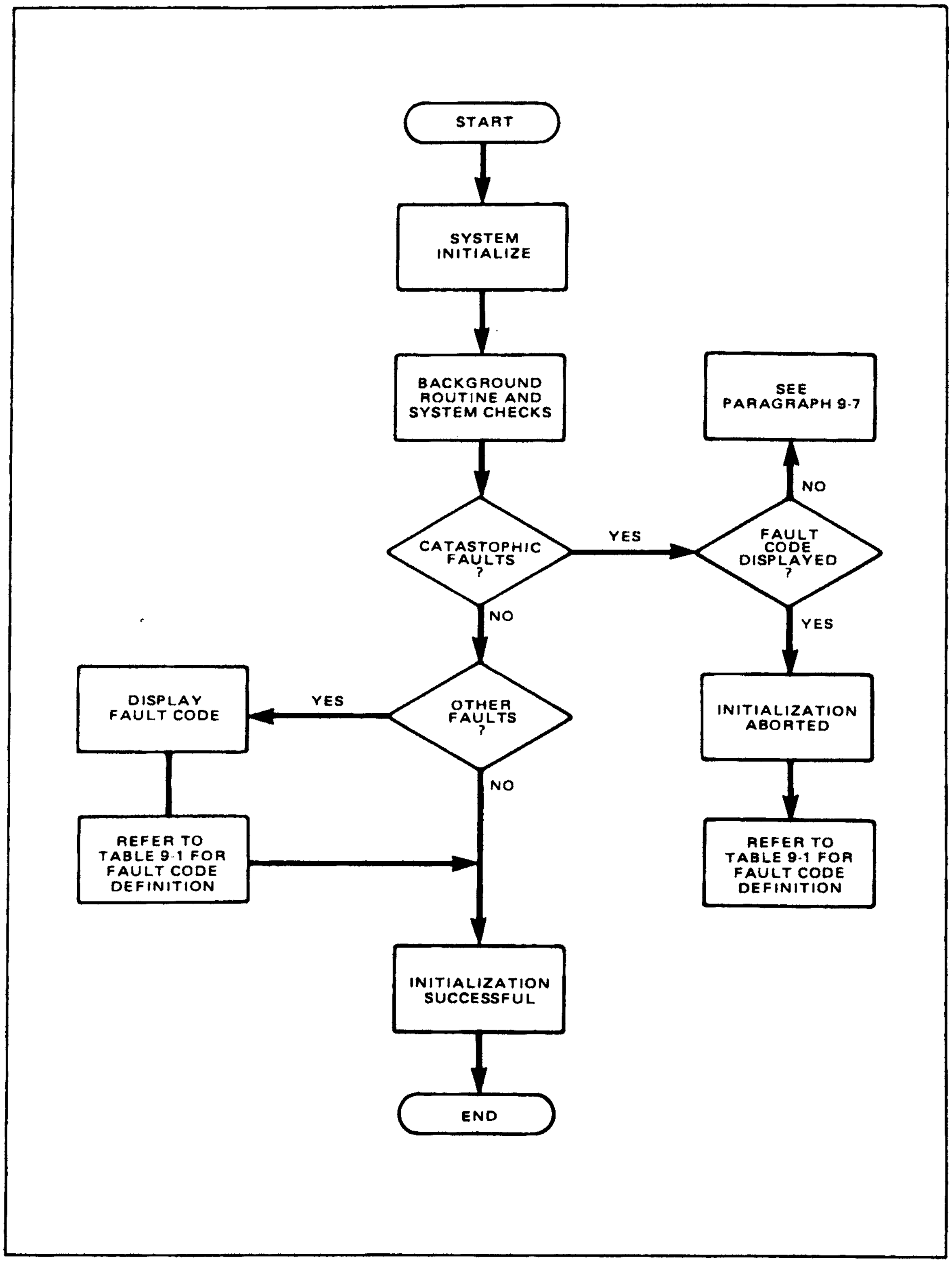


Figure 9-2. Initialization Diagnostics Flowchart

Paragraph 9-7 and Figure 9-3 provide troubleshooting tips should the VPR-80 fail to initialize without fault code display. If a catastrophic fault occurs that causes initialization to be aborted and a fault code is displayed, you should begin either by following the appropriate diagnostic routine, or by using the fault code to determine the potential circuit problem and then troubleshooting using appropriate procedures in this manual. If the VPR-80 initializes, and a fault code is displayed, you should begin either by following the appropriate diagnostic routine, or by using the fault code to determine the potential circuit and again troubleshooting using appropriate procedures in this manual.

9-7 Initialization Fail Fault Isolation

In the event the VPR-80 fails to initialize without any fault code being displayed, Figure 9-3 gives fault isolation procedures for probable causes.

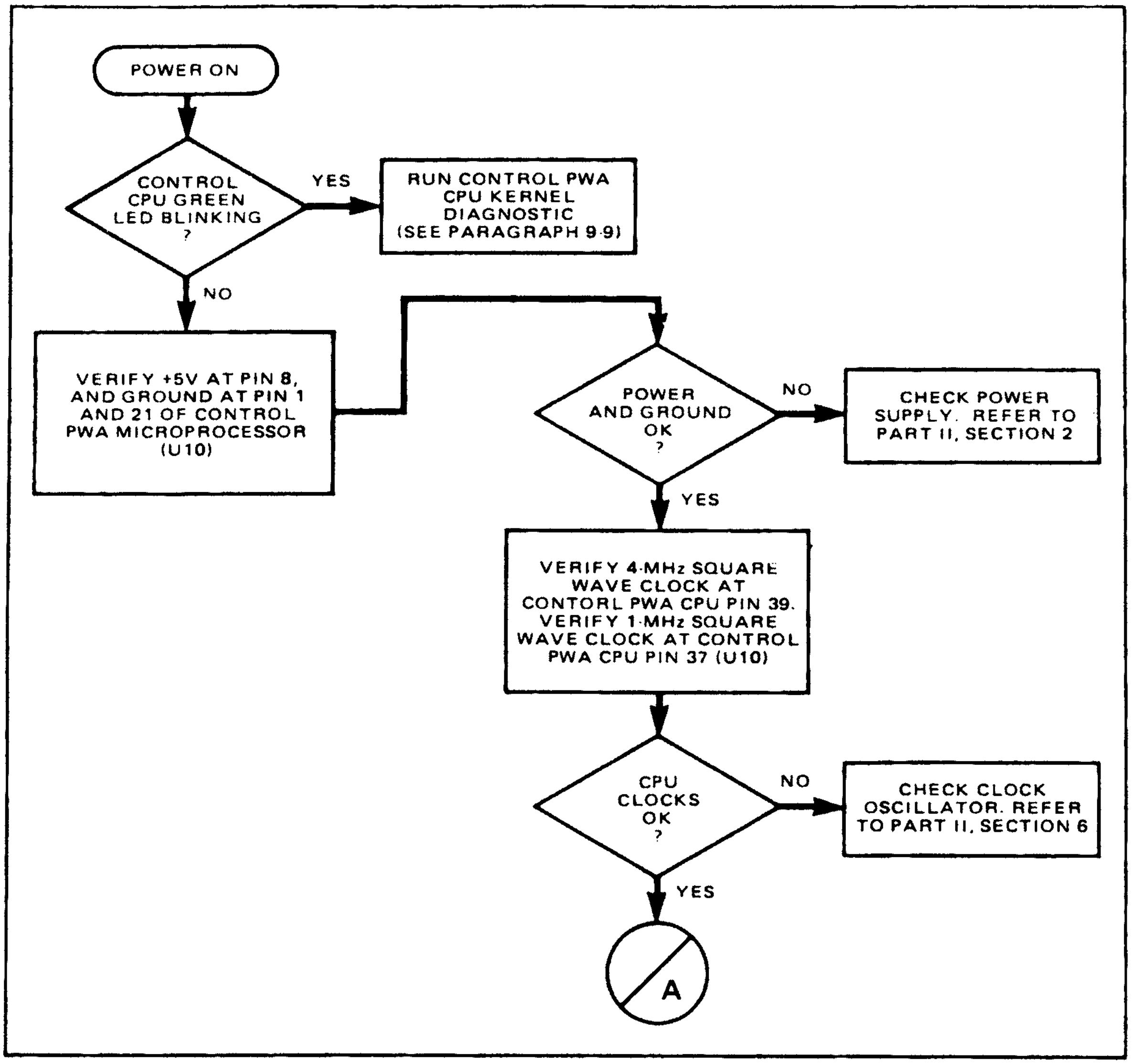

POWER ON
CONTROL CPU GREEN LED BLINKING ?
YES
RUN CONTROL PWA CPU KERNEL DIAGNOSTIC (SEE PARAGRAPH 9-9)
NO
VERIFY +5V AT PIN 8, AND GROUND AT PIN 1 AND 21 OF CONTROL PWA MICROPROCESSOR (U10)
POWER AND GROUND OK ?
NO
CHECK POWER SUPPLY. REFER TO PART II, SECTION 2
YES
VERIFY 4-MHz SQUARE WAVE CLOCK AT CONTORL PWA CPU PIN 39. VERIFY 1-MHz SQUARE WAVE CLOCK AT CONTROL PWA CPU PIN 37 (U10)
CPU CLOCKS OK ?
NO
CHECK CLOCK OSCILLATOR. REFER TO PART II, SECTION 6
YES
A

Figure 9-3. Initialization Fail Fault Isolation (Sheet 1 of 2)

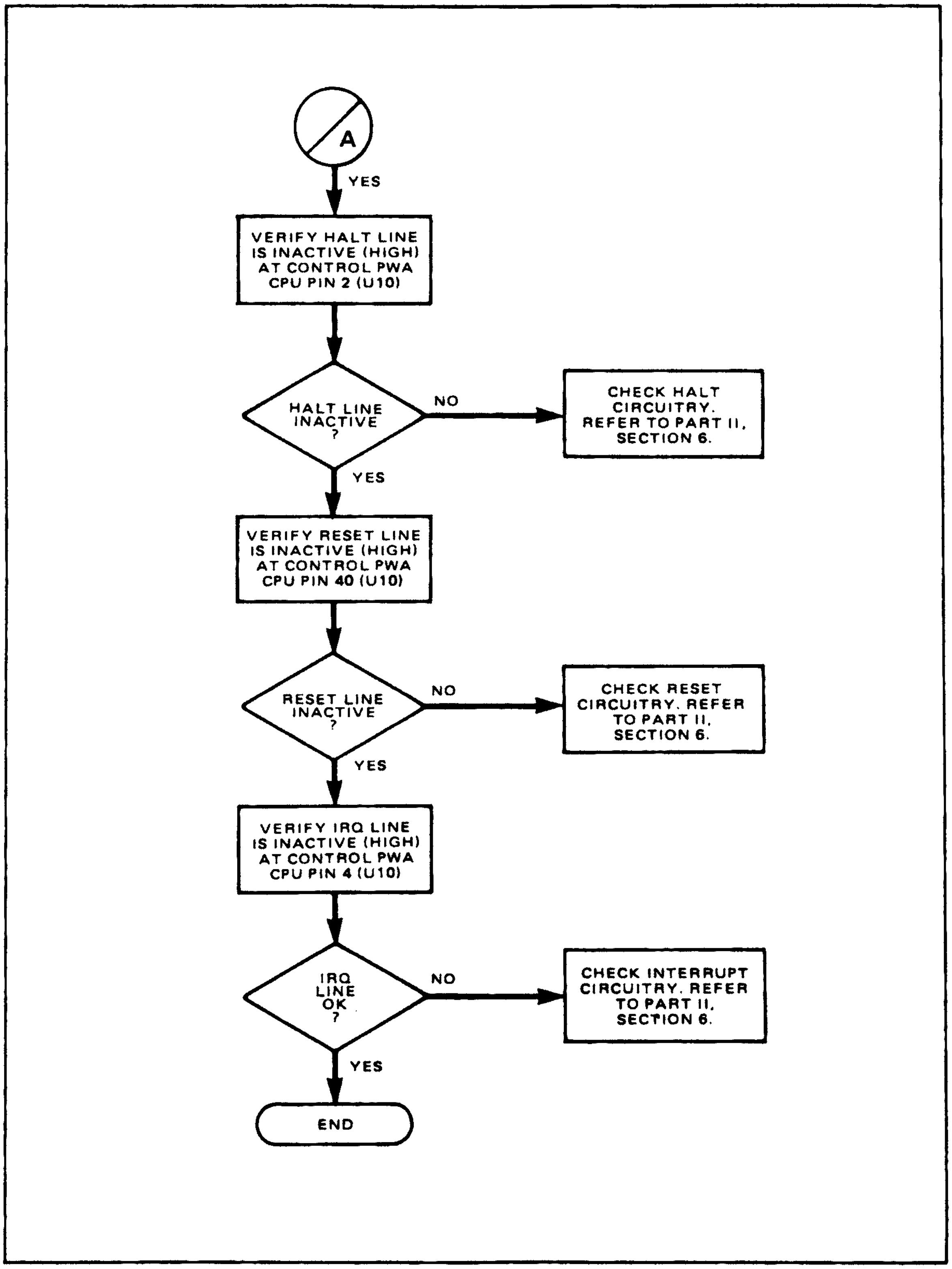

A
YES
VERIFY HALT LINE IS INACTIVE (HIGH) AT CONTROL PWA CPU PIN 2 (U10)
HALT LINE INACTIVE ?
NO
CHECK HALT CIRCUITRY. REFER TO PART II, SECTION 6.
YES
VERIFY RESET LINE IS INACTIVE (HIGH) AT CONTROL PWA CPU PIN 40 (U10)
RESET LINE INACTIVE ?
NO
CHECK RESET CIRCUITRY. REFER TO PART II, SECTION 6.
YES
VERIFY IRQ LINE IS INACTIVE (HIGH) AT CONTROL PWA CPU PIN 4 (U10)
IRQ LINE OK ?
NO
CHECK INTERRUPT CIRCUITRY. REFER TO PART II, SECTION 6.
YES
END

Figure 9-3. Initialization Fail Fault Isolation (Sheet 2 of 2)

9-8 Background Diagnostics

During normal VPR-80 operation, a diagnostic routine continually performs background checks of primary functions. If a fault occurs during normal operation, the FAULT or SYSTEM lamp on the control panel will flash. The operator can press the FAULT or SYSTEM switch, and a code indicating the fault will be displayed. In case of multiple faults, a stack of up to four fault codes is created. With each press of the switch the code for the next most-recent-fault-to-occur will be displayed. Figure 9-4 shows basic operation of background diagnostics, with reference for corrective action in case of a fault. The following functions are continually being checked:

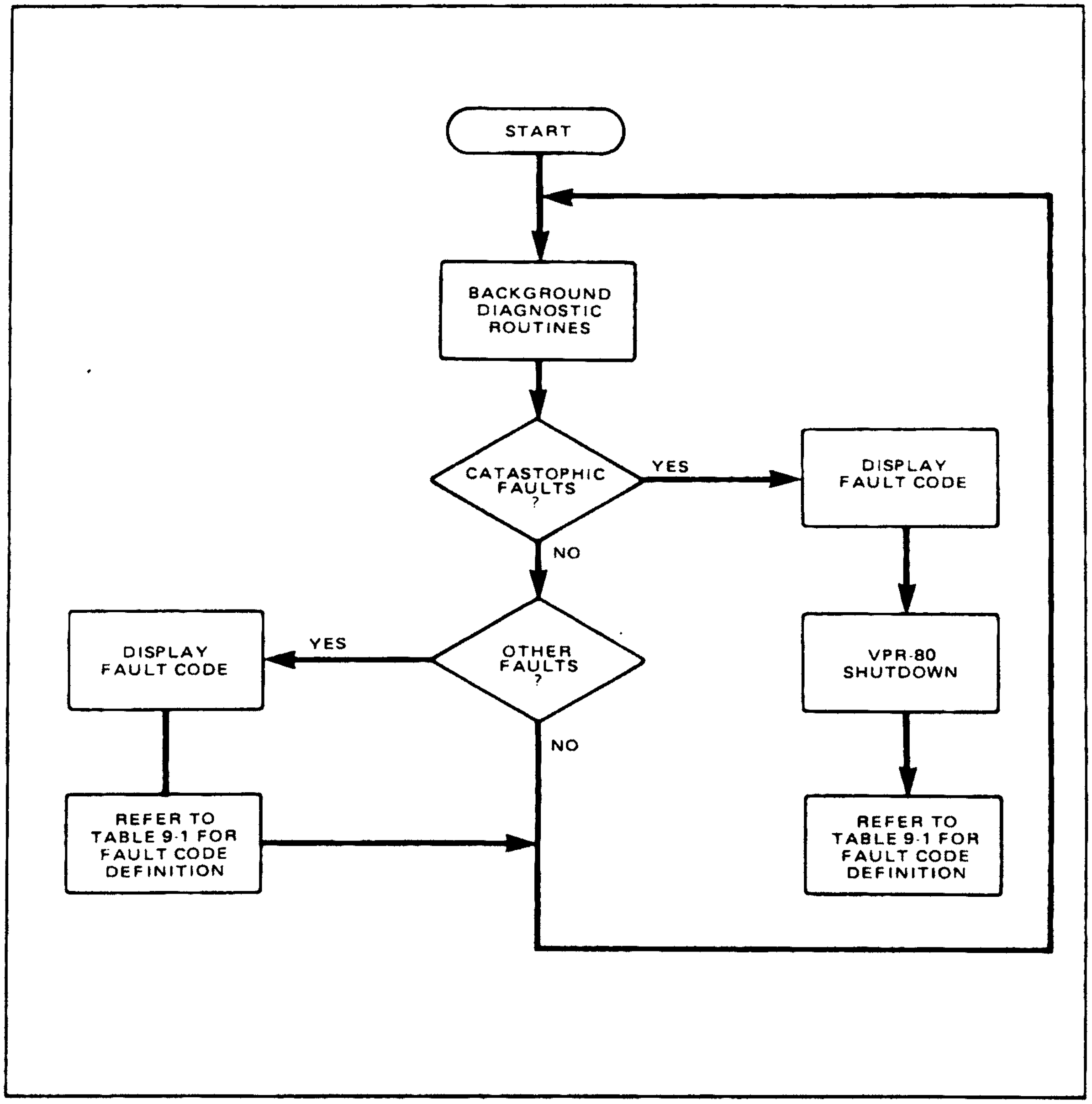

START
BACKGROUND DIAGNOSTIC ROUTINES
CATASTOPHIC FAULTS ?
YES
NO
DISPLAY FAULT CODE
VPR-80 SHUTDOWN
REFER TO TABLE 9-1 FOR FAULT CODE DEFINITION
OTHER FAULTS ?
YES
NO
DISPLAY FAULT CODE
REFER TO TABLE 9-1 FOR FAULT CODE DEFINITION

Figure 9-4. Background Diagnostics Flowchart

Control Main Program Background

Presence of:

Reference Frame
Reference Vertical
Reference Input
Video Input
RF
Control Track

Communication with:

Servo PWA
Parallel Remote PWA
Reference PWA
Serial Remote PWA
Time-Code Reader/Generator
Character Generator PWA
Secondary Control Panel PWA
Primary Control Panel PWA

Power Supply Background

+250V in range
+11V below minimum
Line voltage high or low
+15V high, low or below minimum
-15V high, low or below minimum
Power supply temperature

Servo Main Program Background

Position of Tension Arm
Scanner Lock
Control Track Lock
AST Lock
Scanner Stall
Control Communications
Presence of Scanner Tachometer Pulses
Edit Phase within Range
Color Framing

9-9 Control PWA CPU Kernel Diagnostics

When moved to the test (B-C) position, diagnostic jumper J4 on the Control PWA holds the data bus in the state 00000001. This is the machine code for a NOP (do nothing) instruction. This condition should cause the control processor to step through its address space, one address at a time. The address bus should look like the output of a 16-bit counter, with the lowest-order address line (A0) at U10 pin 9 being a square wave at 500 kHz. Each succeeding address line (pins 10-25) should be a square wave at one-half the frequency of the preceding line. Check address decoders on the Control PWA using the flowchart in Figure 9-5 and the following procedure.

STEP 1 Set an oscilloscope to trigger on U19 pin 3 going low. Outputs of U19 (pins 15-9 and 7) should go low one after another, with pin 15 going first.

STEP 2 Set scope to trigger on U19 pin 14 going low. Outputs of U38 (pins 15-9 and 7) and U24 (pins 15-9 and 7) should go low one after another, with pin 15 going low first.

STEP 3 If address lines are not counting in this way, a short on the address bus is possible. Remove address decoders (U19, U24, and U38) and check address lines again. If address lines are counting properly, decoders, or the bus on the other side of them, are the likely source of the problem.

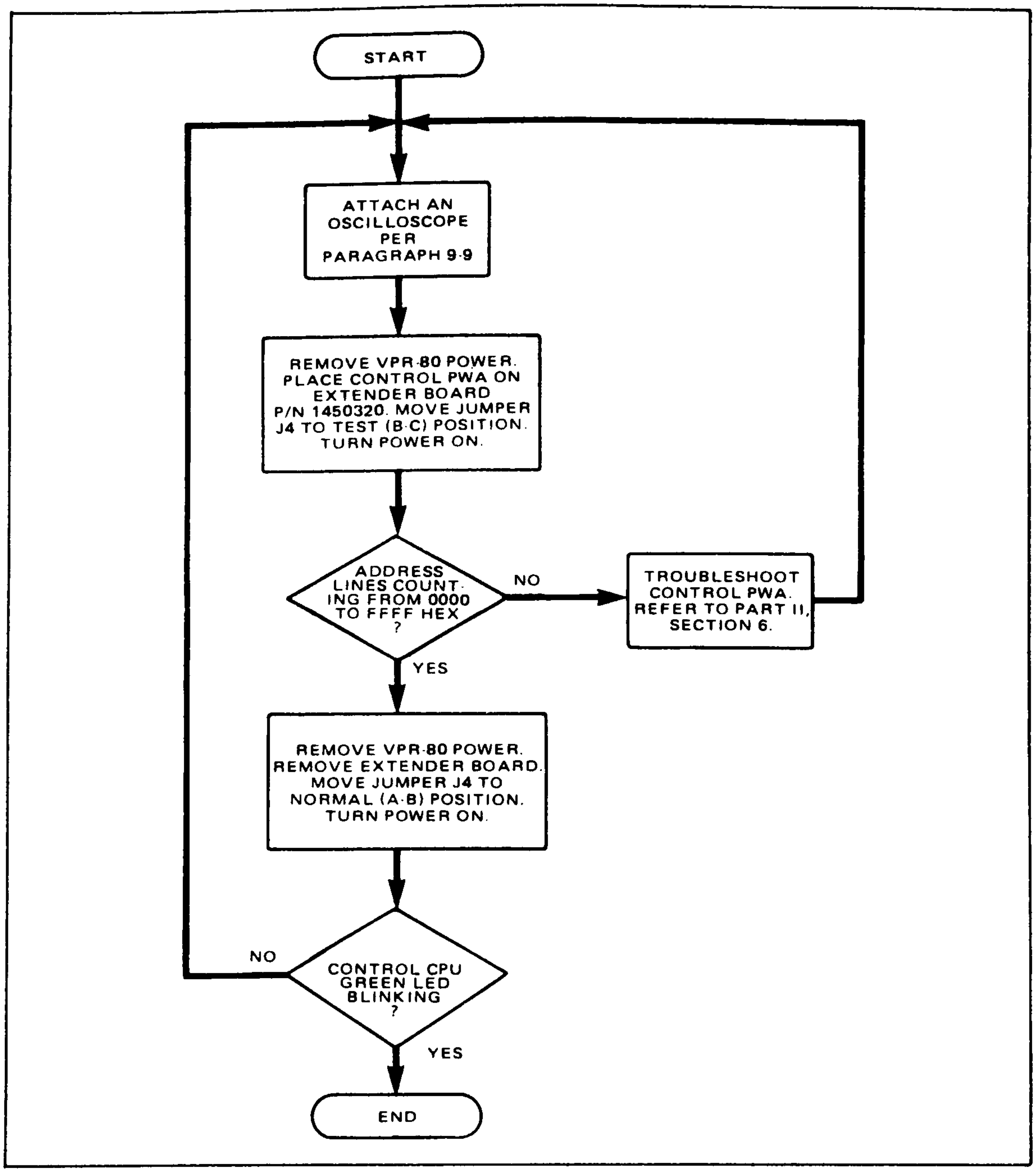

START
ATTACH AN OSCILLOSCOPE PER PARAGRAPH 9-9
REMOVE VPR-80 POWER. PLACE CONTROL PWA ON EXTENDER BOARD P/N 1450320. MOVE JUMPER J4 TO TEST (B-C) POSITION. TURN POWER ON.
ADDRESS LINES COUNTING FROM 0000 TO FFFF HEX ?
NO
TROUBLESHOOT CONTROL PWA. REFER TO PART II, SECTION 6.
YES
REMOVE VPR-80 POWER. REMOVE EXTENDER BOARD. MOVE JUMPER J4 TO NORMAL (A-B) POSITION. TURN POWER ON.
NO
CONTROL CPU GREEN LED BLINKING ?
YES
END

Figure 9-5. Control PWA CPU Kernel Diagnostics

STEP 4 If removing address decoders does not relieve the problem, a short may exist on the address bus between the processor and decoders.

If, after checking all items above, the processor still does not run, a short may exist somewhere on the local data bus. Removing data bus buffers from their sockets isolates the local data bus from the processor.

9-10 Servo PWA CPU Kernel Diagnostics

If a fault occurs that indicates the servo, serial interface, or time-code reader/generator are not functioning properly, the Servo PWA CPU kernel should be checked. The Servo PWA CPU can be checked by removing some components (Figure 9-6) and installing a NOP processor (P/N 090-245) in place of the servo microprocessor. With the NOP processor installed, servo address lines will count from 000 to FFFF hex. Figure 9-6 is a flowchart with basic procedures for performing Servo PWA CPU diagnostics. If servo address lines are not counting as indicated, check for shorts, and check address decoders for that line. Address decoders on the Servo PWA are U25, U45, U38, and U51. The address decoder for the AST PWA is (Servo) U39.

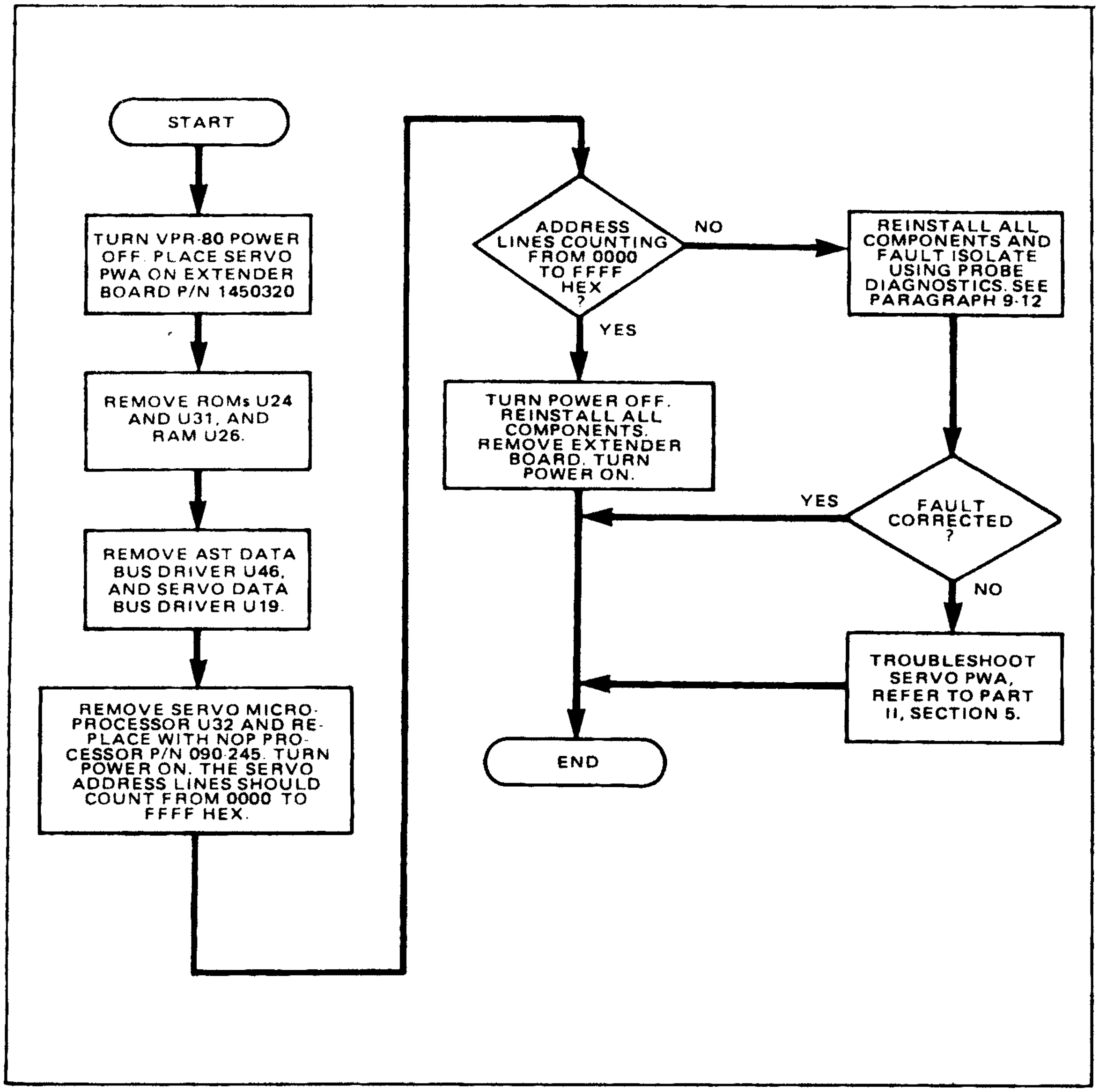

START
TURN VPR-80 POWER OFF. PLACE SERVO PWA ON EXTENDER BOARD P/N 1450320
REMOVE ROMs U24 AND U31, AND RAM U26.
REMOVE AST DATA BUS DRIVER U46, AND SERVO DATA BUS DRIVER U19.
REMOVE SERVO MICRO-PROCESSOR U32 AND RE-PLACE WITH NOP PRO-CESSOR P/N 090-245. TURN POWER ON. THE SERVO ADDRESS LINES SHOULD COUNT FROM 0000 TO FFFF HEX.
ADDRESS LINES COUNTING FROM 0000 TO FFFF HEX ?
NO
YES
REINSTALL ALL COMPONENTS AND FAULT ISOLATE USING PROBE DIAGNOSTICS. SEE PARAGRAPH 9-12
TURN POWER OFF. REINSTALL ALL COMPONENTS. REMOVE EXTENDER BOARD. TURN POWER ON.
FAULT CORRECTED ?
YES
NO
TROUBLESHOOT SERVO PWA, REFER TO PART II, SECTION 5.
END

Figure 9-6. Servo PWA CPU Kernel Diagnostics

9-11 Front Panel Diagnostics

Front panel diagnostics is a non-real-time program that runs outside normal VPR-80 operation. It is initialized by pressing the test switch on the Control PWA—the black switch on the upper edge of the Control PWA, adjacent to the system reset switch.

Note

> **The VPR-80 will not enter the front panel diagnostics program from any mode other than STOP-UNREADY-LOCAL. Before concluding that the test switch is broken, make sure machine is in this state.**

Front panel diagnostics checks associated circuitry by sending a stimulus to the switch and waiting for the operator to press the switch; the diagnostics then reads that response. The program loops on the current test until the operator sequences to the next one, allowing use of enable lines in the area being tested to be used as trigger signals for oscilloscopes or logic analyzers. The service technician can also use probe diagnostics (see paragraph 9-12) to check many of the circuits for front panel switches.

Procedures for running front panel diagnostics are shown in Figure 9-7. For each test the tape timer displays the switch code in the form SS-1 and SS-2, where SS is the code number. The program also displays codes indicating probable faults. Codes are as follows:

Switch	Legend	Switch	Legend
1	Shutle	18	Ready-9
2	Cue	19	Master lockout-8
3	Stop	20	Video lockout-7
4	Variable Play	21	Edit optimize
5	Play	22	System
6	Record	23	Fault
7	Exit	24	Setup
8	Entr	25	Chroma/eg norm/invert
9	Remote 2- greater than--	26	Color frame norm/invert
10	Assemble-0	27	Audio 3 speaker/phones
11	Audio 3 lockout-Enter	28	Audio 2 speaker/phones
12	Remote 1-3	29	Audio 1 speaker/phones
13	Insert-2	30	TSO advance
14	Audio 2 lockout-1	31	TSO retard
15	EE-6	32	-
16	Auto-5	33	+
17	Audio 1 lockout-4		

Code	Meaning
1	Switch closed
2	Switch opened after closing
3	Switch stuck shut
4	No switch closed
5	Multiple or incorrect switch pressed

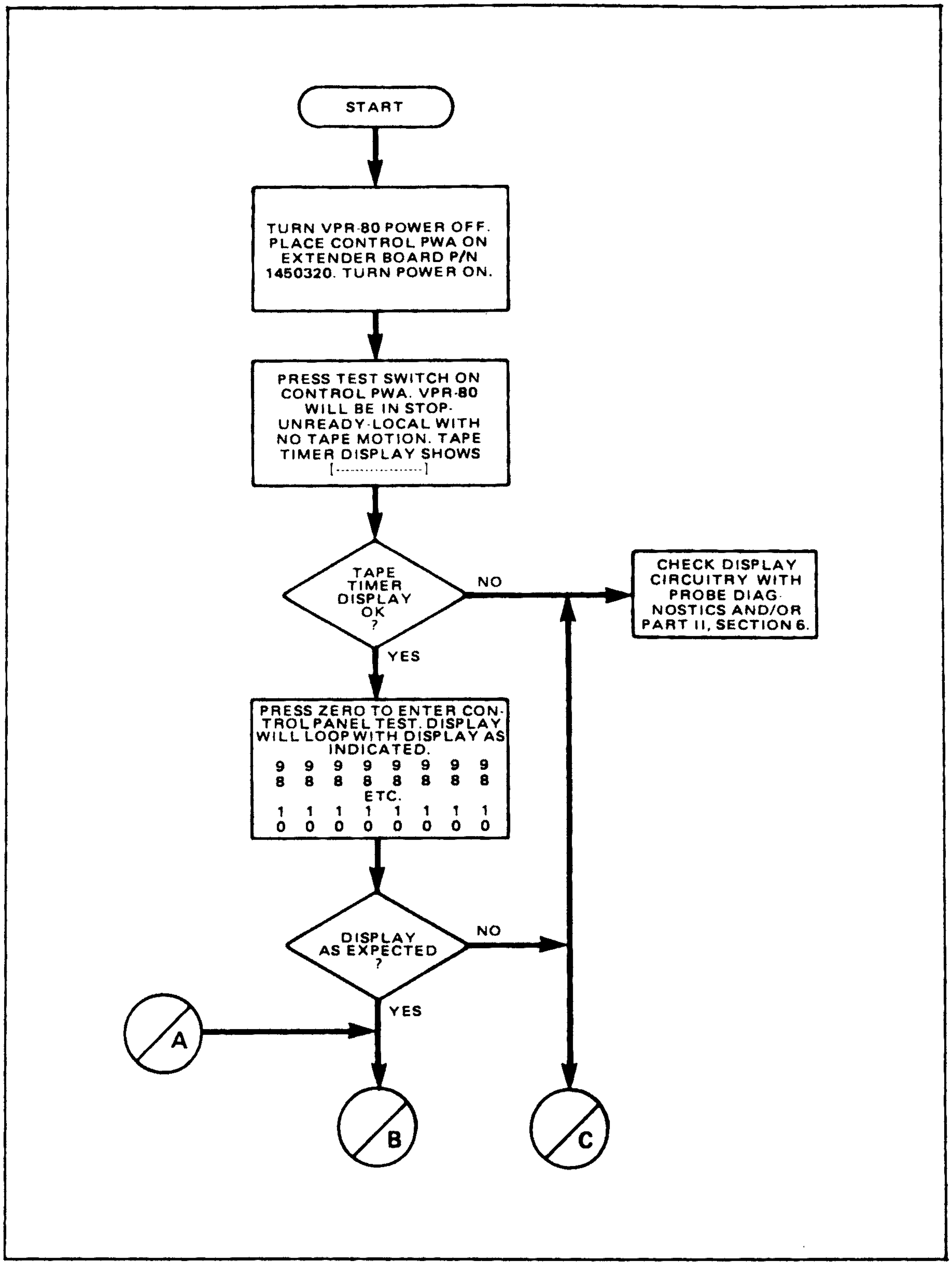

START
TURN VPR-80 POWER OFF. PLACE CONTROL PWA ON EXTENDER BOARD P/N 1450320. TURN POWER ON.
PRESS TEST SWITCH ON CONTROL PWA. VPR-80 WILL BE IN STOP-UNREADY-LOCAL WITH NO TAPE MOTION. TAPE TIMER DISPLAY SHOWS [--------------------]
TAPE TIMER DISPLAY OK ?
NO
CHECK DISPLAY CIRCUITRY WITH PROBE DIAGNOSTICS AND/OR PART II, SECTION 6.
YES
PRESS ZERO TO ENTER CONTROL PANEL TEST. DISPLAY WILL LOOP WITH DISPLAY AS INDICATED.
9 9 9 9 9 9 9 9
8 8 8 8 8 8 8 8
ETC.
1 1 1 1 1 1 1 1
0 0 0 0 0 0 0 0
DISPLAY AS EXPECTED ?
NO
YES
A
B
C

Figure 9-7. Control Panel Diagnostics (Sheet 1 of 2)

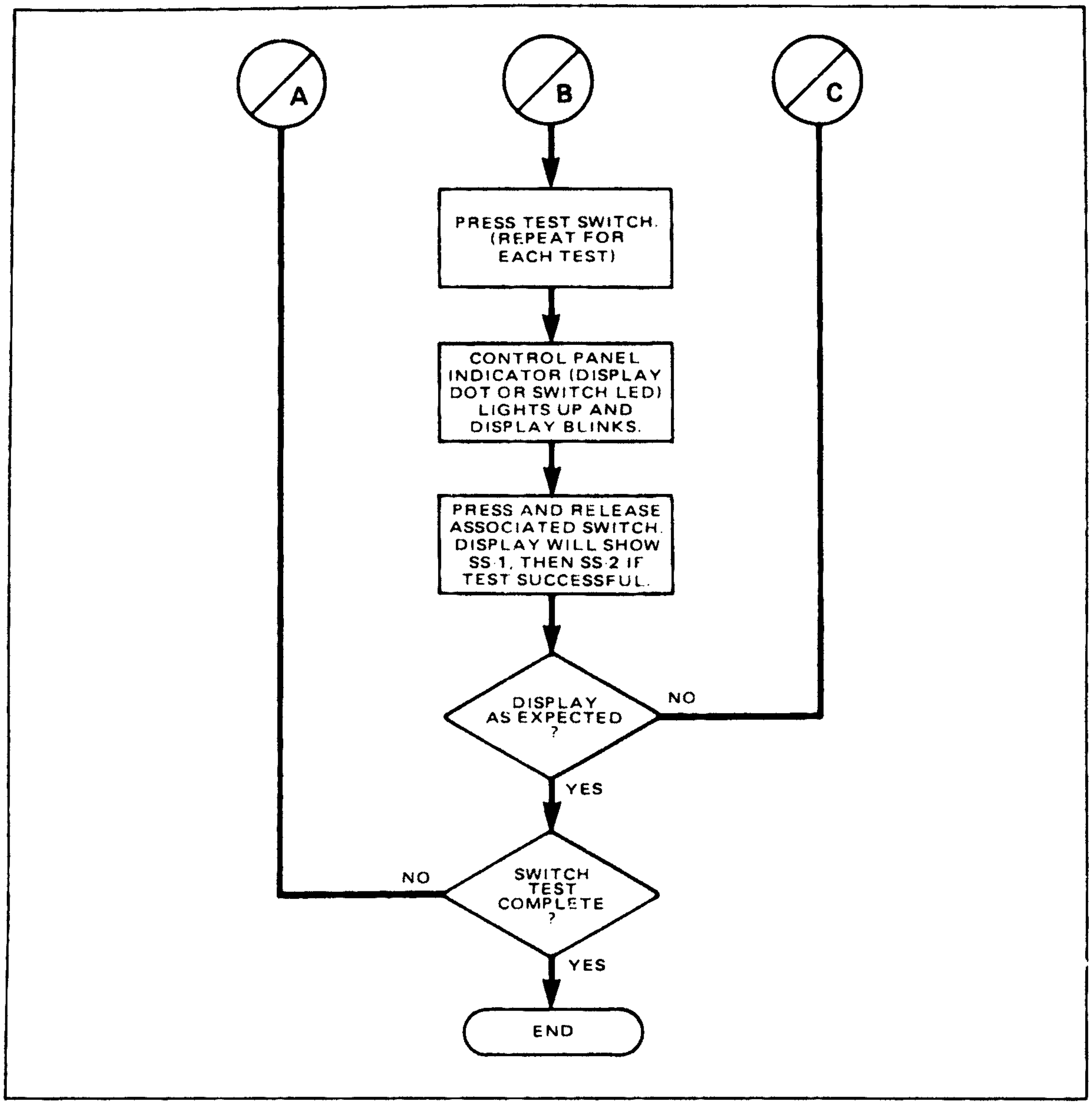

A
B
C
PRESS TEST SWITCH. (REPEAT FOR EACH TEST)
CONTROL PANEL INDICATOR (DISPLAY DOT OR SWITCH LED) LIGHTS UP AND DISPLAY BLINKS.
PRESS AND RELEASE ASSOCIATED SWITCH. DISPLAY WILL SHOW SS-1, THEN SS-2 IF TEST SUCCESSFUL.
DISPLAY AS EXPECTED ?
NO
YES
SWITCH TEST COMPLETE ?
NO
YES
END

Figure 9-7. Control Panel Diagnostics (Sheet 2 of 2)

9-12 Probe Diagnostics

Probe diagnostics is also a non-real-time program which runs outside normal VPR-80 operation. It is initialized by pressing the test switch on the Control PWA.

Note

The VPR-80 will not enter the probe diagnostics program from any mode other than STOP-UNREADY-LOCAL. If probe diagnostics fails to run, make sure machine is in this state before concluding there is another problem.

Probe diagnostics can check major portions of VPR-80 circuitry by sending a signal and reading back the result. Each subassembly in the VPR-80 is assigned a three-digit code for use by the operator in identifying the subassembly to be checked. A list of subassembly codes can be found on the inside front flip-cover of the machine. A copy is included here for your convenience. Also, each IC has a one- or two-digit code for identification. The IC code is the schematic IC number found in the *VPR-80 Parts Lists and Schematics* manual (Catalog No. 1809548).

Code	Assembly	Code	Assembly
100	AST	106	Serial Remote
101	AST Driver	107	TC Reader/Generator
102	Control	108	Power Supply
103	Servo	109	Secondary Control Panel
104	Reference	110	Primary Control Panel
105	Parallel Remote	111	Audio

Procedures for running front panel diagnostics are shown in Figure 9-8. Basically, the procedure is to attach the probe, verify probe operation, and then key in the subassembly and IC number. As an example, to test IC cc of subassembly aaa, either key in aaa then key in cc, or key in aaacc (all together). If the IC number is a single digit, enter aaa then c or aaac. If an invalid subassembly or IC number is entered, the program will promp the operator for another entry by displaying dashes in the subassembly or IC position in the tape timer display. For example: to test U36 on the Control PWA, key in 102, and then press ENTER on the keypad. The tape timer display will read 102--, prompting for a chip number. To enter the chip number, key in 36, and then press ENTER. Display will read **102-36,** and then change to **36-2,** indicating pin 2 of U36 is the first pin to test. If U36 is not eligible for testing, the system will stay at 102--. If the probe had not been tested previously, after entering 36, the display will show **102-P2,** indicating a probe test must be performed.

When the diagnostic program displays IC and pin number, simply touch the probe tip to the displayed pin number and press the probe switch. The diagnostics program will display the IC number and pin number, followed by one then two if the pin tests ok. The diagnostics will then display the next pin number to test on that IC. After an IC has been tested, the tape timer dispay will show dashes again, indicating that it is waiting for a new subassembly and IC number.

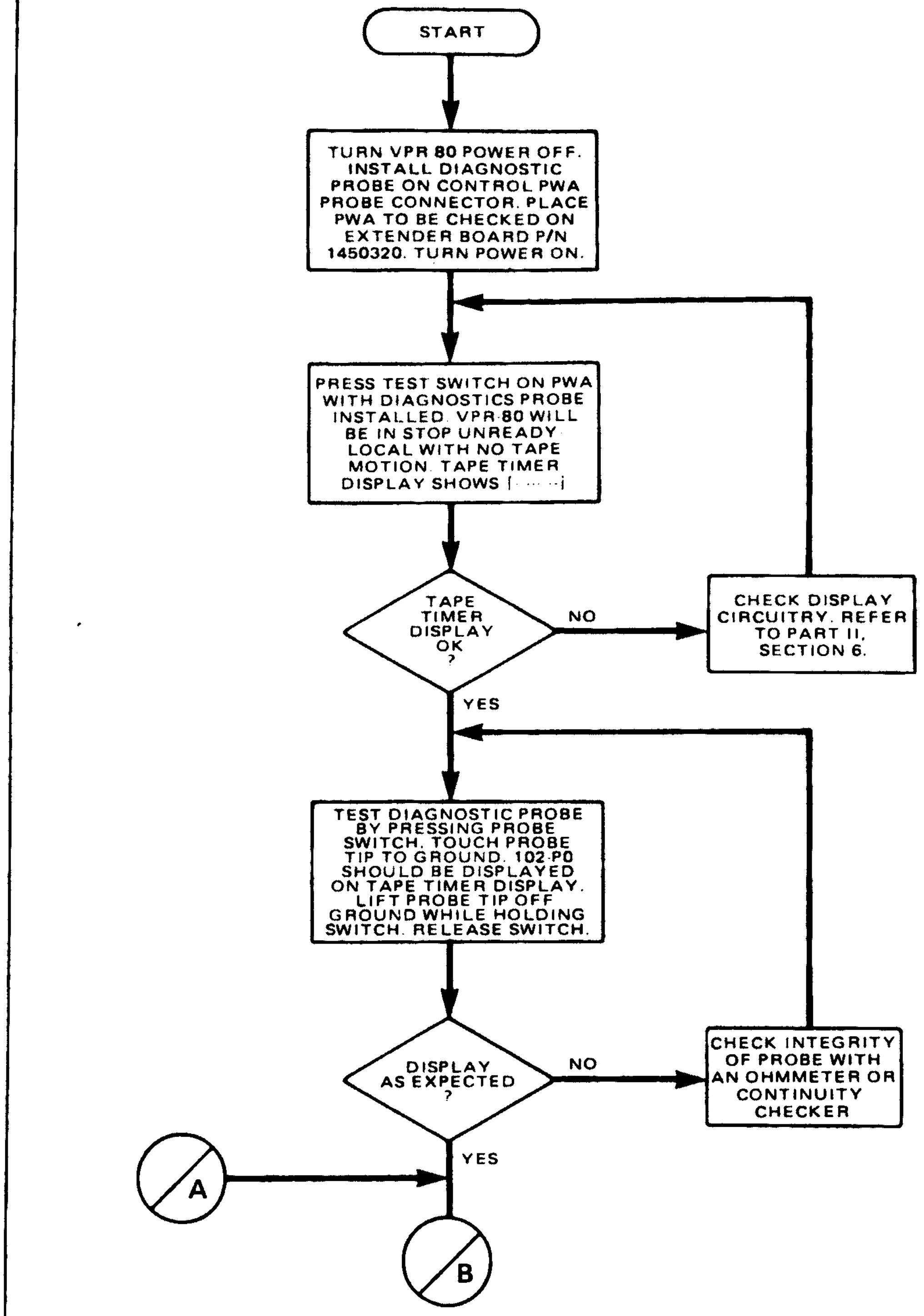

START
TURN VPR 80 POWER OFF. INSTALL DIAGNOSTIC PROBE ON CONTROL PWA PROBE CONNECTOR. PLACE PWA TO BE CHECKED ON EXTENDER BOARD P/N 1450320. TURN POWER ON.
PRESS TEST SWITCH ON PWA WITH DIAGNOSTICS PROBE INSTALLED. VPR-80 WILL BE IN STOP UNREADY LOCAL WITH NO TAPE MOTION. TAPE TIMER DISPLAY SHOWS [- --- --]
TAPE TIMER DISPLAY OK ?
NO
CHECK DISPLAY CIRCUITRY. REFER TO PART II, SECTION 6.
YES
TEST DIAGNOSTIC PROBE BY PRESSING PROBE SWITCH. TOUCH PROBE TIP TO GROUND. 102-P0 SHOULD BE DISPLAYED ON TAPE TIMER DISPLAY. LIFT PROBE TIP OFF GROUND WHILE HOLDING SWITCH. RELEASE SWITCH.
DISPLAY AS EXPECTED ?
NO
CHECK INTEGRITY OF PROBE WITH AN OHMMETER OR CONTINUITY CHECKER
YES
A
B

Figure 9-8. Probe Diagnostics Flowchart (Sheet 1 of 2)

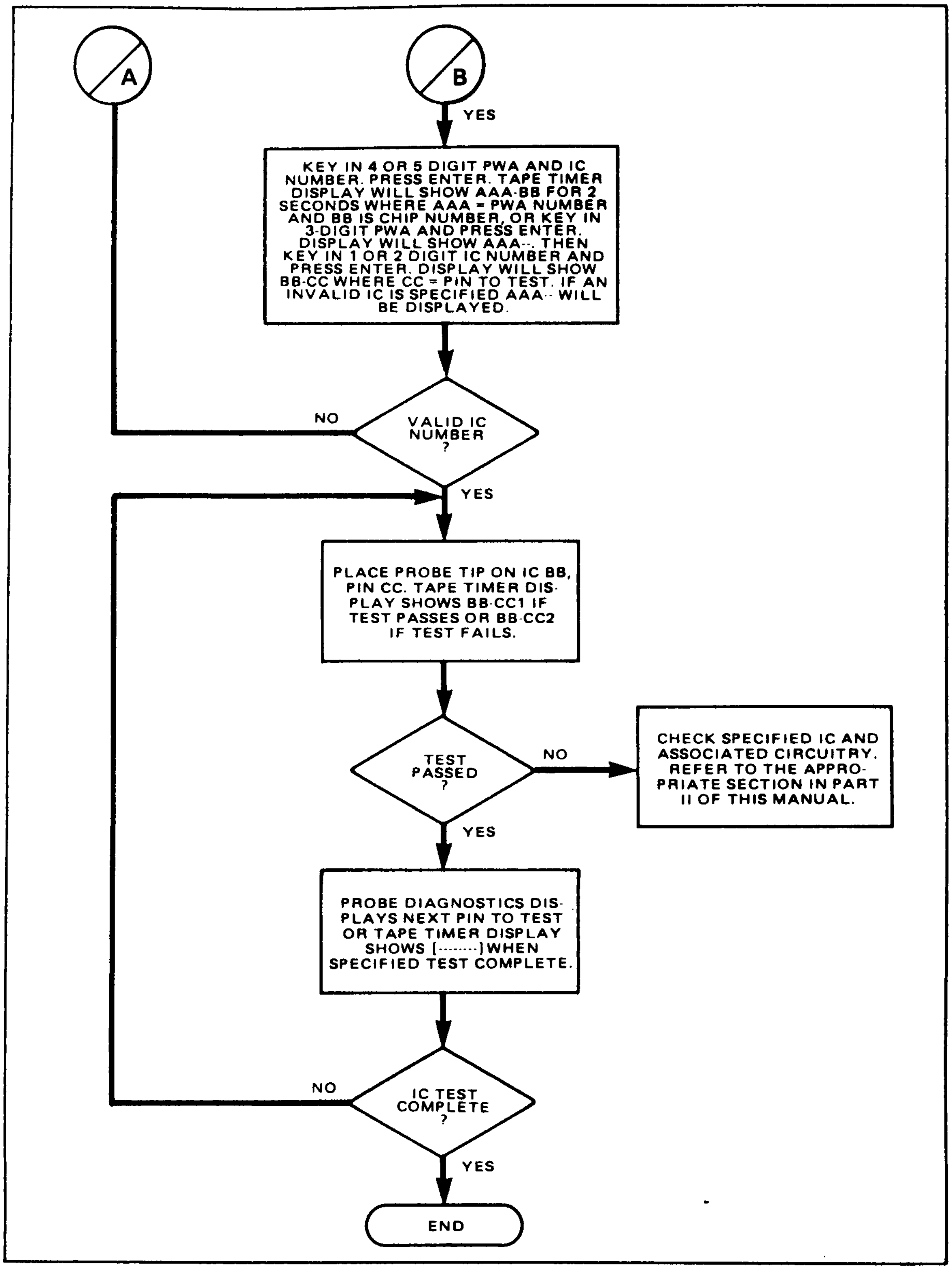

A
B
YES
KEY IN 4 OR 5 DIGIT PWA AND IC NUMBER. PRESS ENTER. TAPE TIMER DISPLAY WILL SHOW AAA-BB FOR 2 SECONDS WHERE AAA = PWA NUMBER AND BB IS CHIP NUMBER, OR KEY IN 3-DIGIT PWA AND PRESS ENTER. DISPLAY WILL SHOW AAA--. THEN KEY IN 1 OR 2 DIGIT IC NUMBER AND PRESS ENTER. DISPLAY WILL SHOW BB-CC WHERE CC = PIN TO TEST. IF AN INVALID IC IS SPECIFIED AAA-- WILL BE DISPLAYED.
NO
VALID IC NUMBER ?
YES
PLACE PROBE TIP ON IC BB, PIN CC. TAPE TIMER DISPLAY SHOWS BB-CC1 IF TEST PASSES OR BB-CC2 IF TEST FAILS.
TEST PASSED ?
NO
CHECK SPECIFIED IC AND ASSOCIATED CIRCUITRY. REFER TO THE APPROPRIATE SECTION IN PART II OF THIS MANUAL.
YES
PROBE DIAGNOSTICS DISPLAYS NEXT PIN TO TEST OR TAPE TIMER DISPLAY SHOWS [--------] WHEN SPECIFIED TEST COMPLETE.
NO
IC TEST COMPLETE ?
YES
END

Figure 9-8. Probe Diagnostics Flowchart (Sheet 2 of 2)

Table 9-1. Diagnostic Fault Codes

Machine Faults	
100-03	AST PWA TIMER (U3)
100-22	AST PWA REF VERTICAL ABSENT
100-31	AST PWA REF FRAME ABSENT
100-47	AST PWA TIMER (U47)
100-56	AST PWA TIMER (U56)
101-02	AST DRIVER HIGH VOLTAGE REGULATOR
102-P2	CONTROL PWA PROBE FAULT
102-3-	CONTROL AND SERVO ROMs INCOMPATIBLE
102-05	CONTROL PWA ROM 4 FAULT
102-10	CONTROL PWA RAM 1 FAULT (U10)
102-11	CONTROL PWA ROM 3 FAULT
102-16	CONTROL PWA ROM 2 FAULT
102-20	CONTROL PWA ROM 1 FAULT
102-23	CONTROL PWA SYSTEM RESET
102-25	CONTROL PWA RAM 2 FAULT (U25)
102-27	CONTROL PWA TIMER 1 (U27)
102-32	CONTROL PWA TIMER 2 (U32)
102-44	CONTROL PWA INTERRUPTS
103- -	SERVO PWA DASH NUMBERS DON"T AGREE
103-01	SERVO PWA ARM OUT OF WINDOW
103-11	SERVO PWA TIMER FAULT (U11)
103-16	SERVO PWA TIMER FAULT (U16)
103-20	SERVO PWA COMM FAULT W/CTL PWA SEND
103-22	SERVO PWA CAPSTAN NOT LOCKED TO REF
103-23	SERVO PWA TIMER FAULT (U23)
103-24	SERVO PWA ROM 1 FAULT (U24)
103-26	SERVO PWA RAM FAULT (U26)
103-31	SERVO PWA ROM 2 FAULT (U31 and U32)
103-32	SERVO PWA INTERNAL RAM FAILURE
103-33	SERVO PWA COMM FAULT W/CTL PWA RECEIVE
103-35	SERVO PWA TIMER FAULT (U35)
103-36	SERVO PWA TIMER FAULT (U36)
103-41	SERVO PWA TIMER FAULT (U41)
103-49	SERVO PWA TIMER FAULT (U49)
103-50	SERVO PWA CAPSTAN RUNAWAY
103-56	SERVO WAS TIMER FAULT (U56)
103-63	SERVO PWA TIMER FAULT (U63)
103-64	SERVO PWA SUPPLY REEL FAULT
103-65	SERVO PWA TAKE UP REEL FAULT
103-70	SERVO PWA TIMER FAULT (U70)
103-73	SERVO PWA SCANNER TACH MISSING
103-77	SERVO PWA TIMER FAULT (U77)

(Continued next page)

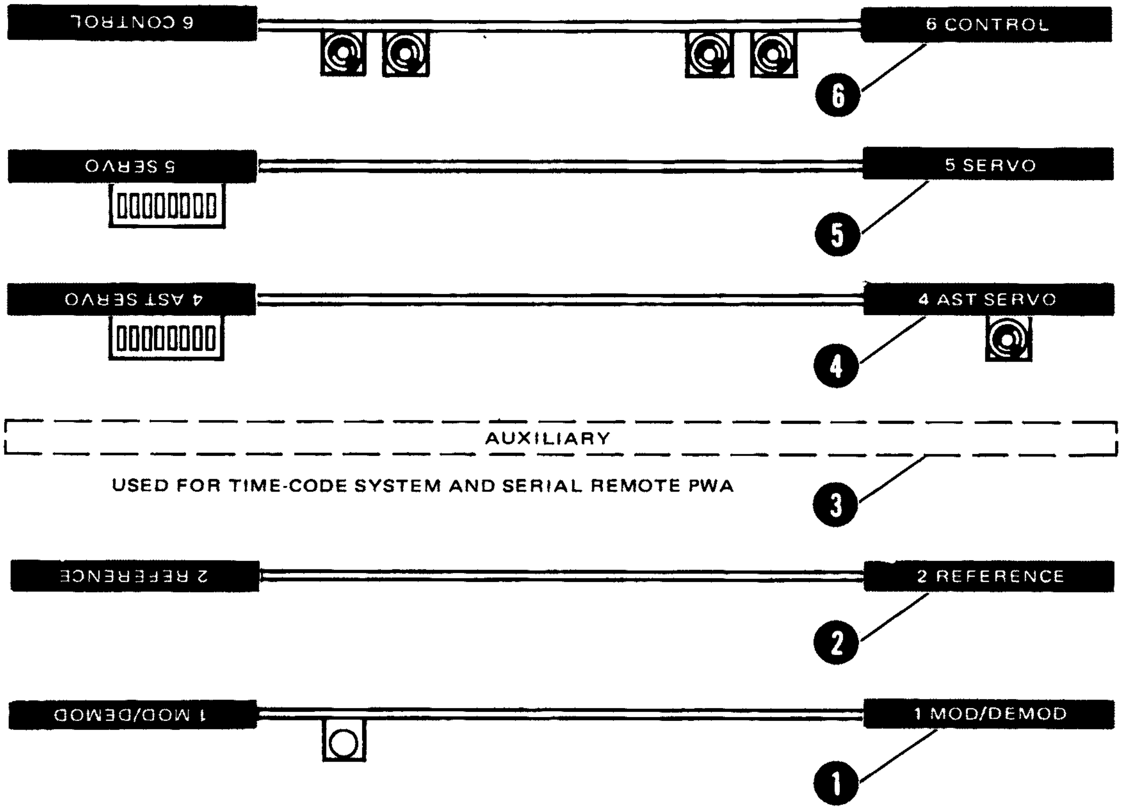
Table 9-1. Diagnostic Fault Codes (Continued)

Machine Faults	
104-23	REF PWA COMM FAULT (NTSC)
104-29	REF PWA COMM FAULT (PAL)
105-02	PARALLEL REMOTE PWA COMM FAULT W/CTL PWA
106-08	SERIAL REMOTE PWA COMM FAULT W/CTL PWA
107-30	TIMER CODE READER SEN/CG COMM FAULT

System Faults			
SYS_01	REF ABSENT	SYS_13	NOT CUED
SYS_02	VIDEO ABSENT	SYS_14	EXIT BEFORE ENTR
SYS_03	REF AND VIDEO ABSENT	SYS_15	UNABLE TO EDIT OPTIMIZE
SYS_04	RF ABSENT	SYS_16	MANUAL TRACKING DISABLED
SYS_05	CTL TRACK ABSENT	SYS_17	HI LINE
SYS_06	SERVOS NOT LOCKED	SYS_18	LO LINE
SYS_07	CTL TRACK NOT LOCKED	SYS_19	STORED DATA LOST
SYS_08	NOT FIELD MATCHED	SYS_20	PWR SUPPLY OVERTEMP
SYS_09	NOT COLOR FRAMED	SYS_21	TAPE OUT OF PATH
SYS_10	EDIT PHASE RANGE EXCEEDED	SYS_22	CUE POINT NOT FOUND
SYS_11	SCANNER STALLED		
SYS_12	AUTO RECORD—EDITOR OFF		

9-18 SUPPLEMENTAL INFORMATION

This section contains supplemental information that assists locating individual components tested with the diagnostic probe. Figure 9-9 shows the location of the individual PWA contained in the card rack assembly. Figures 9-10 through 9-18 show the location of the individual components under test.



Index No.	Reference Designator	Printed Wiring Assembly (PWA)	Part Number
1	PWA 6	Control	1450276
2	PWA 5	Servo	1450306
3	PWA 4	AST Servo	1450256
4	(PWA 3)	(Reserved for accessory PWAs)	
5	PWA 2	Reference (NTSC)	1450346
5	PWA 2	Reference (PAL-M)	1450363
5	PWA 2	Reference (PAL/SECAM)	1450356
6	PWA 1	MOD/DEMOD (525)	1450206
6	PWA 1	MOD/DEMOD (625)	1450216

Figure 9-9. Card Cage Assembly PWA Locations

AST Servo PWA (100-)

Board switches set as follows:

S1 (track jump timing)--all bits open (down)

U10 pins 2,3,4,5,6,7,8,9
U36 pins 2,3,4,5,6,7,8,9
U37 pins 2,5,6,7.9.12.15.16.19
U38 pins 2,5,6,12,15,16,19

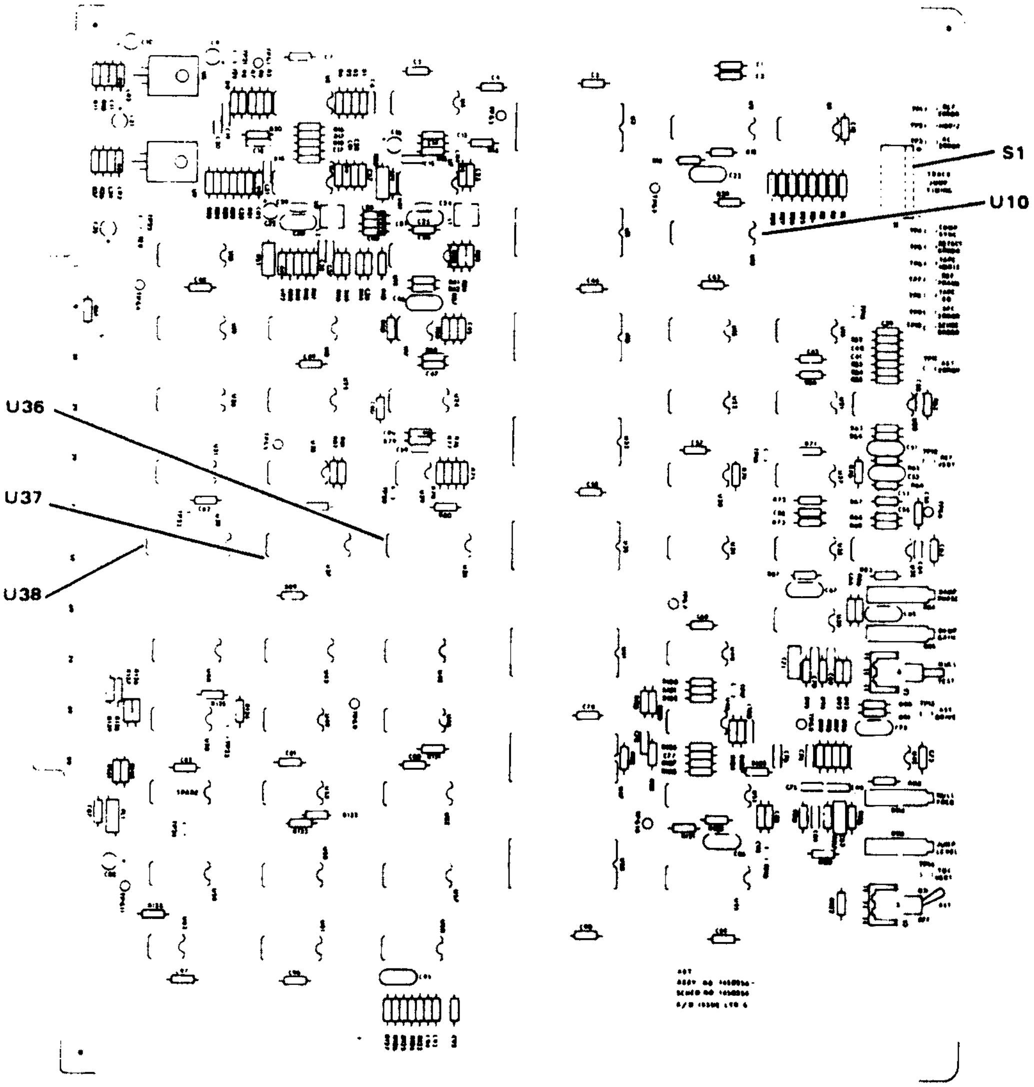


Figure 9-10. AST Servo PWA

Control PWA (102-)

Switches set as follows:
S3 (color framer)—(right position)
S4 (ff-df)—full frame (right position)
S5 (reference)—auto (center position)
S6 (preroll)—variable (center position)

Also: remove reference PWA from card cage with power off.
Defeat tape-in-path sensor.

U36 pins 2,5,6,9,12,15,16,19 (record relay clicks with each pin tested)
U39 pins 16,15,14
U40 pins 2,5,6,9,12,15
U41 pins 4,5,6,7,8,9

Note

Board edge switches must be set as stated above to test all pins on U41

U45 pins 5,6,9,12,15,16,19
U46 pins 7,8,9

Note

Tape must be in path to test pin 7. Reference board must be out to test pins 8 and 9 on U46.

U50 pins 2,3,6,7,8,9

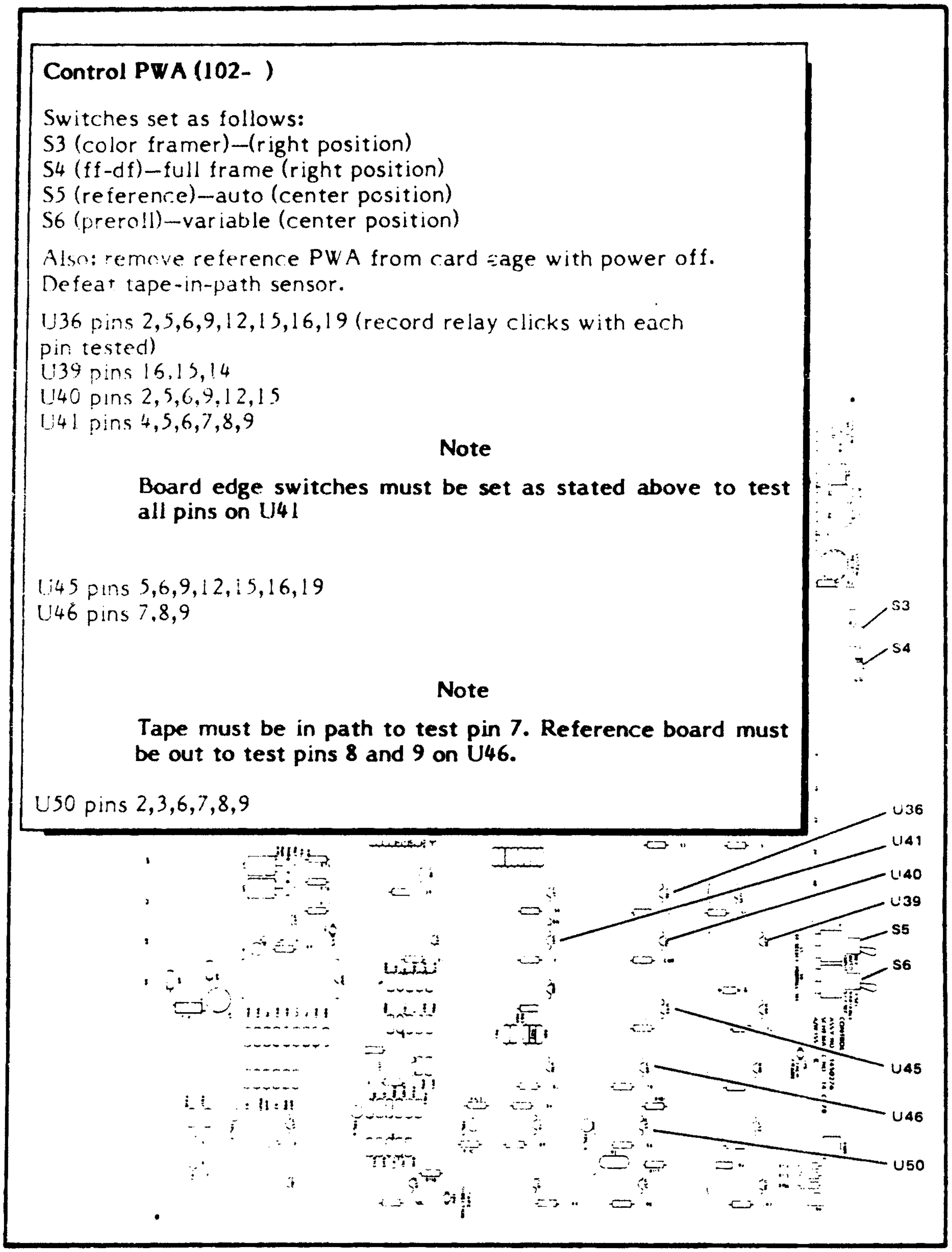


Figure 9-11. Control PWA

Servo PWA (103-   )

Switches set as follows:
S1 (scanner phase range)—all bits open (down)

U3 pins 2,5,6,9,12,15,16,19
U17 pins 2,3,4,5,6,7,8,9
U18 pins 3,4,5,6
U76 pins 2,3,4,5,6
U78 pins 2,5,16,19

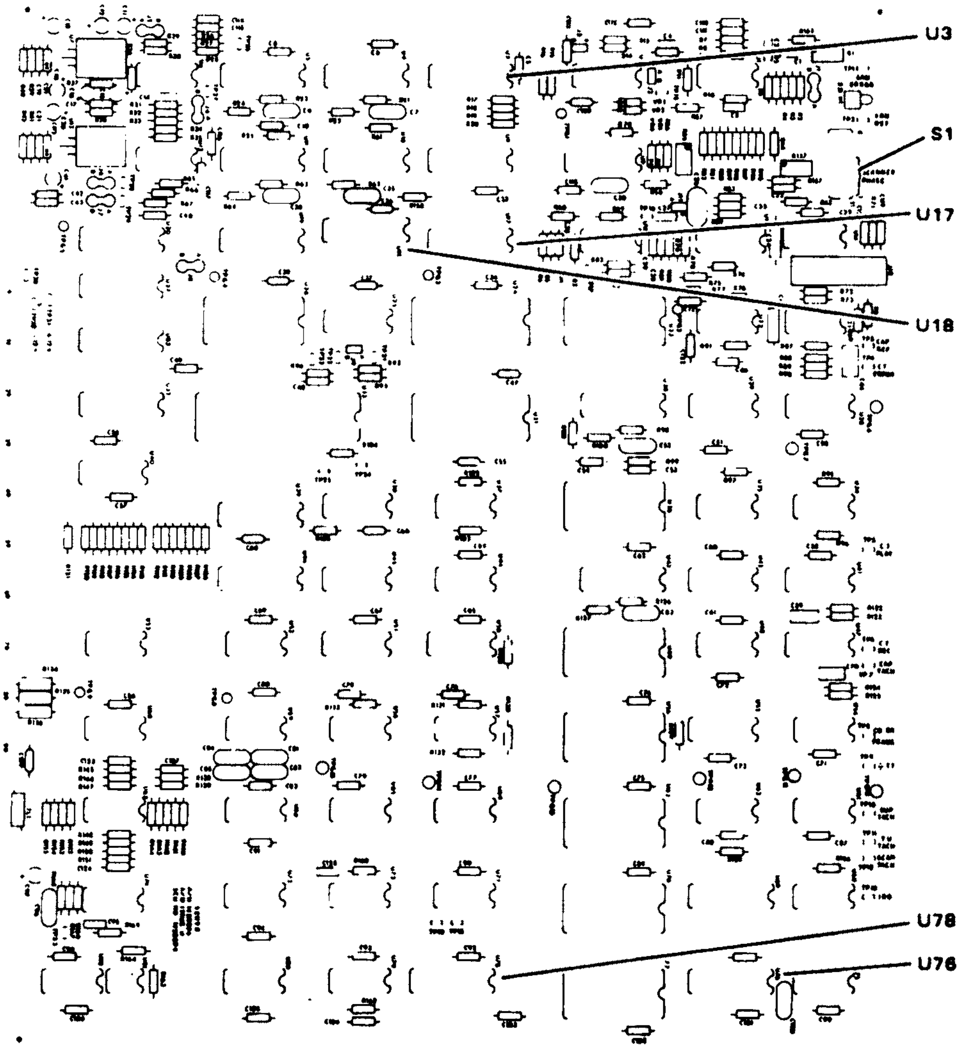


Figure 9-12. Servo PWA

Reference PWA (104-)

NTSC
U23 pins 2,5,6,9,12,15,16,19
U28 pin 9

Note
Not testable on board issues before E.

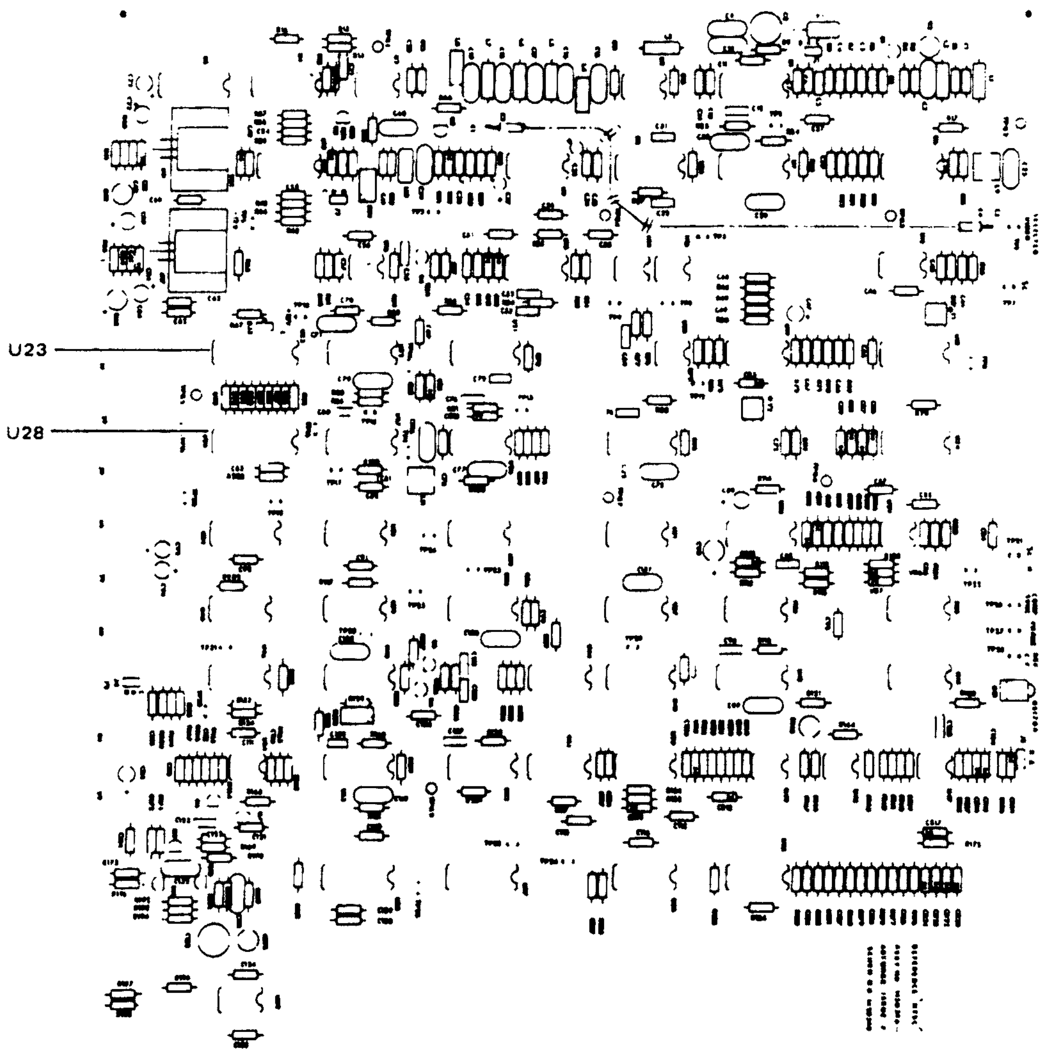


Figure 9-13. Reference PWA NTSC

Reference PWA (104-)

PAL
U29 pins 2,5,6,9,12,15,16,19
U37 pin 9

Note

Not testable on board issues before E.

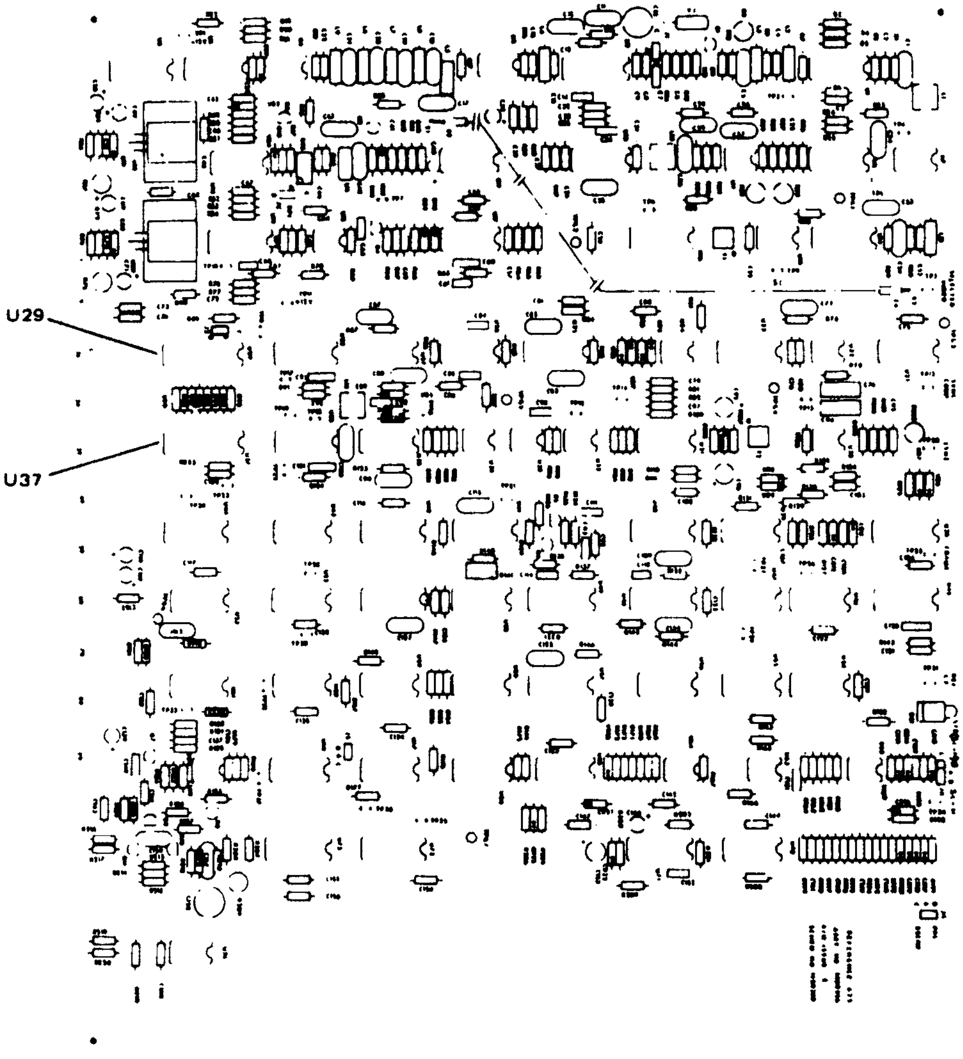


Figure 9-14. Reference PWA PAL/SECAM

Parallel Remote PWA (105-)

Switches set as follows:

S1 (normal-ACE-VPR2) -ACE (center position)

Also disconnect any remote panel or device.

U1 pins 3,4,5,8,9
U2 pins 2,5,6,9,19
U4 pins 2,3,4,5,8,9 (touching pin 5 clicks relay on board)
U5 pins 2,5,6,9,12,15
U8 pins 2,3,4,5,6,7,8,9
U9 pins 2,5,6,9,12,15,16
U12 pins 2,3,4,5,6,7,8,9

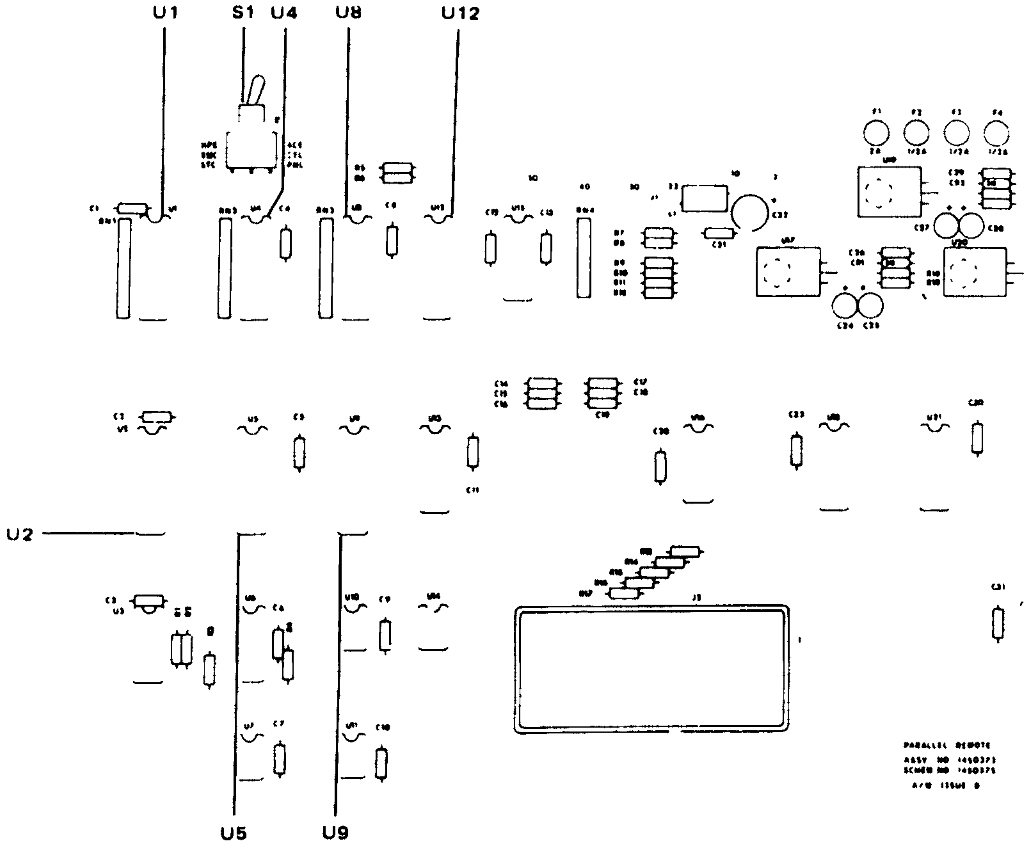


Figure 9-15. Parallel Remote PWA

Secondary Control Panel PWA (109-   )

CAUTION

When testing U1 and U3, remove the head hour meter drive (J2) to avoid having the tests increment the meter.

Note

Any tests of the control panel PWAs may turn on control panel lights at any time. The lights will turn off again when the program returns to the main selector.

U1 pins 16,15,14,13,12,11,10
U2 pins 16,15,12
U3 pins 5,6,9 12,15,16,19
U4 pins 2,5,6,9,12,15,16,19
U5 pins 3,4,5,6,7,8,9
U6 pins 2,3,4,5,6,7,8,9

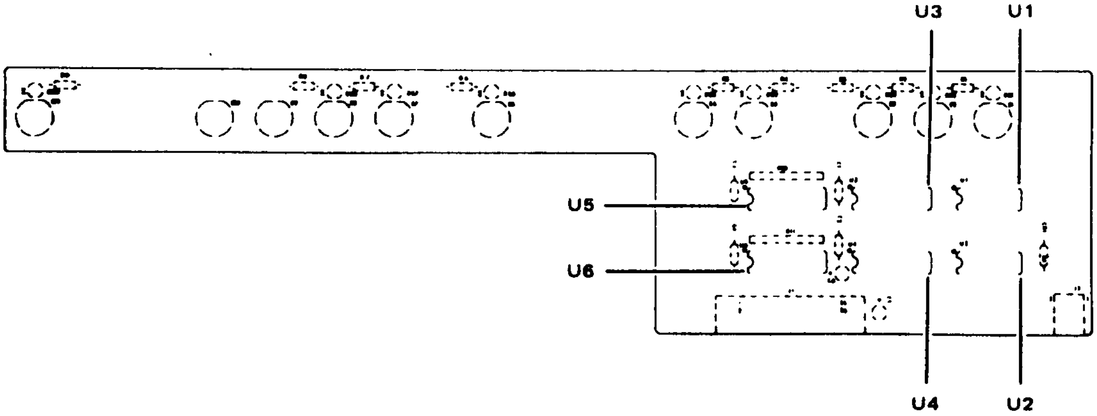


Figure 9-16. Secondary Control Panel PWA

Primary Control Panel PWA (110-)

Note

> **Any tests of the control panel PWAs may turn on control panel lights at any time. The lights will turn off again when the program returns to the main selector.**

U4 pins 2,3,4,5,6,7,8,9
U5 pins 2,5,6,9,12,15,16,19
U6 pins 16,15,14,13,12,11,10
U7 pins 2,3,4,5,6,7,8,9
U8 pins 2,5,6,9,12,15

Note

> **Touching pin 11 may make tape timer display go blank momentarily.**

U9 pins 16,15,14,13,12,11
U20 pins 2,3,4,5,6,7,8,9

Note

> **Touching pin 9 after an unsuccessful test may force the diagnostic program back to the main selector.**

U21 pins 2,5,6,9,12,15,16,19
U22 pins 16,15,14,13,12,11

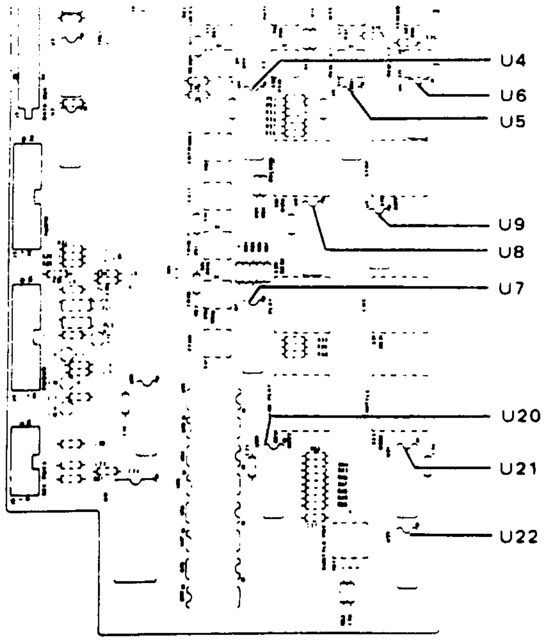


Figure 9-17. Primary Control Panel PWA

Audio PWA (111-)

U65 pins 2,5,6,9,12,15,16,19 (may cause relays to click)
U72 pins 2,5,6,9,12,15,16,19
U90 pins 2,5

Note

Sequencing to next chip test with probe still held on a pin may force the probe to be tested again.

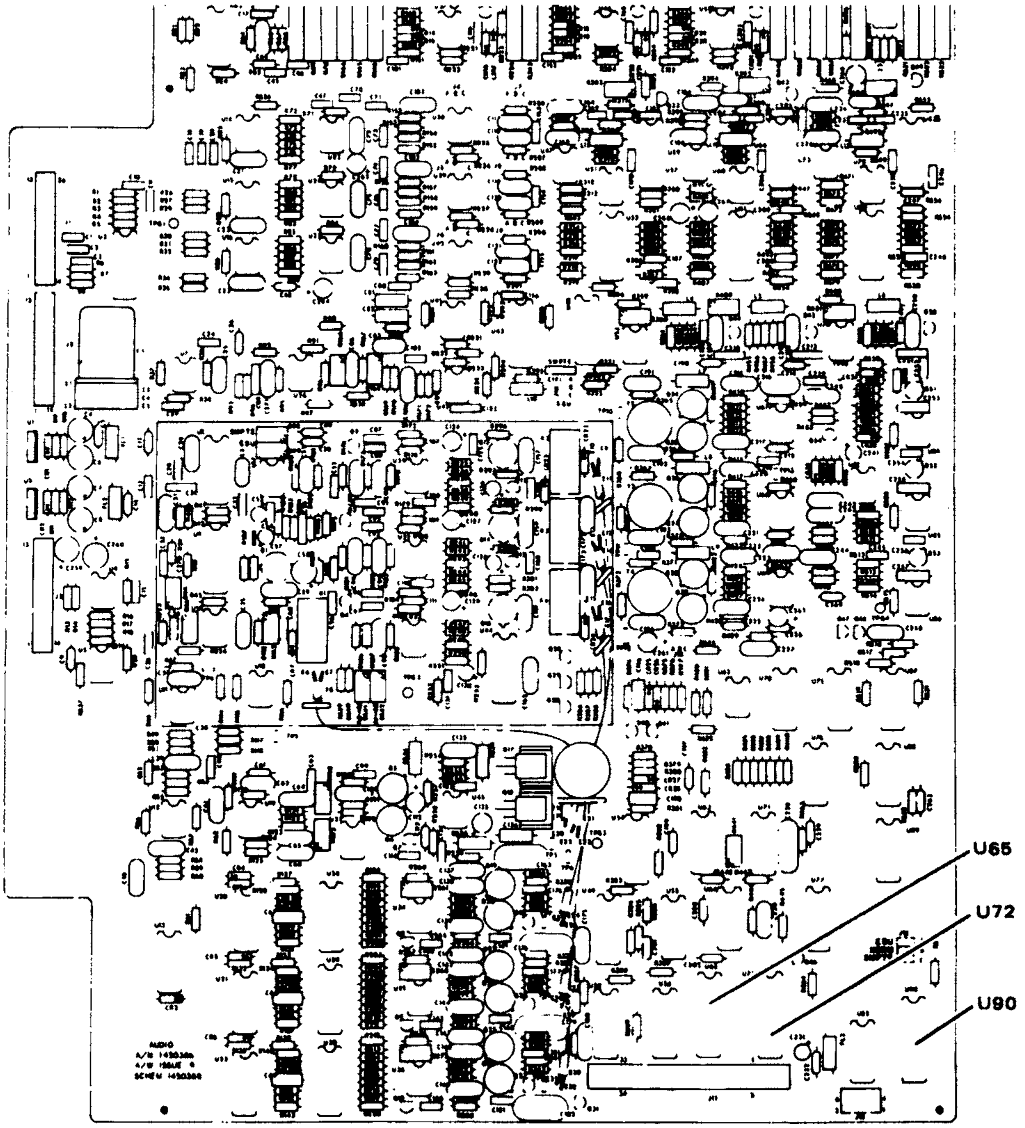


Figure 9-18. Audio PWA

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